HARRIS HI-201HS/883

High Speed Quad SPST CMOS Analog Switch

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low "ON" Resistance .....50Ω Max**
- **Wide Analog Signal Range ..... ±15V**
- **Turn-On Time..... 50ns**
- **Analog Current Range (Continuous)..... 25mA**
- **TTL/CMOS Compatible**
- **No Latch-Up**
- **Pin Compatible with Standard HI-201**

Applications

- **High Speed Multiplexing**
- **High Frequency Analog Switching**
- **Sample and Hold Circuits**
- **Digital Filters**
- **Op Amp Gain Switching Networks**
- **Integrator Reset Circuits**

Description

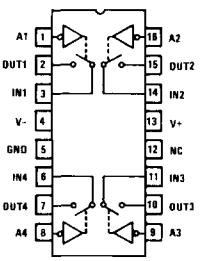
HI-201HS/883 is a monolithic CMOS Analog Switch featuring very fast switching speeds and low ON resistance. This integrated circuit consists of four independently selectable SPST switches and is pin compatible with the industry standard HI-201 switch.

Fabricated using silicon-gate technology and the Harris dielectric isolation process, this TTL compatible device offers improved performance over previously available CMOS analog switches while eliminating the problem of latch-up associated with other fabricated processes. Featuring maximum switching times of 50ns, low ON resistance of 50Ω maximum, and a wide analog signal range, the HI-201HS/883 is designed for any military application where improved switching performance, particularly switching speed, is required. (A more detailed discussion on the design and application of the HI-201HS/883 can be found in Application Note 543).

The HI-201HS/883 is available in a 16 pin Ceramic DIP package and a 20 pin LCC package. The HI-201HS/883 is specified over the temperature range of -55°C to +125°C.

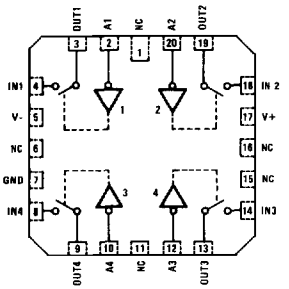
Pinouts

HI1-201HS/883 (CERAMIC DIP)
TOP VIEW

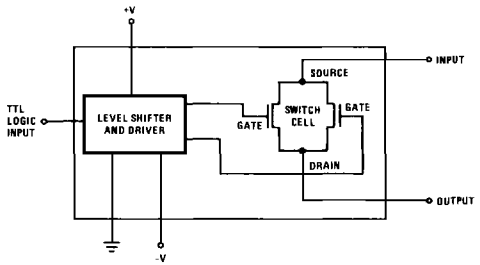


LOGIC	SWITCH
0	ON
1	OFF

HI4-201HS/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



4 CMOS ANALOG SWITCHES

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) ..... $\pm$18V
Analog Input Voltage $+V_S$ ..... $+V_{SUPPLY}$ +2V
$-V_S$ ..... $-V_{SUPPLY}$ -2V
Digital Input Voltage $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_A$ ..... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 50mA
Continuous Current Any Terminal (Except S or D) 25mA
Junction Temperature ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	75°C/W	16°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 0.99W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package ..... 13.36mW/°C
Ceramic LCC Package ..... 13.12mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) ..... $\pm$15V
Analog Input Voltage (V_S) ..... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) ..... 0V to 0.8V
Logic High Level (V_{AH}) ..... 3.0V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_{AL} = 0.8V, V_S = 10V, I_D = -1mA, All Unused Channels V_{AL} = 0.8V	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_{AL} = 0.8V, V_S = -10V, I_D = 1mA, All Unused Channels V_{AL} = 0.8V	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_{AH} = 3.0V, All Unused Channels V_{AH} = 3.0V, V_D = +14V, V_S = -14V	1	+25°C	-10	10	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_{AH} = 3.0V, All Unused Channels V_{AH} = 3.0V, V_D = -14V, V_S = +14V	1	+25°C	-10	10	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -14V, V_S = +14V, V_{AH} = 3.0V, All Unused Channels V_{AH} = 3.0V, V_D = +14V, V_S = -14V	1	+25°C	-10	10	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = +14V, V_S = -14V, V_{AH} = 3.0V, All Unused Channels V_{AH} = 3.0V, V_D = -14V, V_S = +14V	1	+25°C	-10	10	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_{AL} = 0.8V, All Unused Channels V_{AL} = 0.8V, V_D = V_S = -14V	1	+25°C	-10	10	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = -14V, V_{AL} = 0.8V, All Unused Channels V_{AL} = 0.8V, V_D = V_S = +14V	1	+25°C	-10	10	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	V_{AL} = 0.8V, All Unused Channels V_{AH} = 4.0V	1	+25°C	-	500	µA
			2, 3	-55°C to +125°C	-	500	µA
High Level Input Current	I_{AH}	V_{AH} = 4.0V, All Unused Channels V_{AL} = 0.8V	1	+25°C	-	40	µA
			2, 3	-55°C to +125°C	-	40	µA
Supply Current	$+I_{CC}$	All Channels V_{AL} = 0.8V	1, 2	+25°C, +125°C	-	10	mA
			3	-55°C	-	10	mA
		All Channels V_{AH} = 3.0V	1, 2	+25°C, +125°C	-	10	mA
			3	-55°C	-	10	mA
Supply Current	$-I_{CC}$	All Channels V_{AL} = 0.8V	1, 2	+25°C, +125°C	-	6	mA
			3	-55°C	-	6	mA
		All Channels V_{AH} = 3.0V	1, 2	+25°C, +125°C	-	6	mA
			3	-55°C	-	6	mA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	$t_{(ON)}$	C_L = 35pF, R_L = 1kΩ V_{AH} = 3.0V, V_{AL} = 0.8V	9	+25°C	-	50	ns
			10, 11	-55°C, +125°C	-	100	ns
Turn "OFF" Time	$t_{(OFF)}$	C_L = 35pF, R_L = 1kΩ V_{AH} = 3.0V, V_{AL} = 0.8V	9	+25°C	-	50	ns
			10, 11	-55°C, +125°C	-	100	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Capacitance	C_A	f= 1MHz, V_{AL} = 0V	1	+25°C	-	35	pF
Switch Input Capacitance	$C_{S(OFF)}$	f = 1MHz, V_{AH} = 5V Measure Input to Ground	1	+25°C	-	20	pF
Switch Output Capacitance	$C_{D(OFF)}$	f = 1MHz, V_{AH} = 5V Measure Output to Ground	1	+25°C	-	20	pF
	$C_{D(ON)}$	f = 1MHz, V_{AL} = 0V Measure Output to Ground	1	+25°C	-	50	pF
Drain to Source Capacitance	C_{DS}	f = 1MHz, V_{AH} = 5V	1	+25°C	-	2.0	pF
Off Isolation	V_{ISO}	f = 100kHz, V_A = 3.0, R_L = 1K V_{GEN} = $1V_{p-p}$, C_L = 10pF	1	+25°C	50	-	dB
Crosstalk	V_{CT}	f = 100kHz, V_A = 3.0, R_L = 1K V_{GEN} = $1V_{p-p}$, C_L = 10pF	1	+25°C	50	-	dB
Charge Transfer Error	V_{CTE}	R_L = 1K, C_L = 0.01µF	1	+25°C	-	10	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

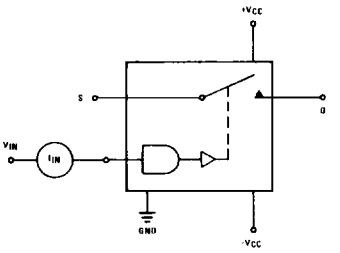
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

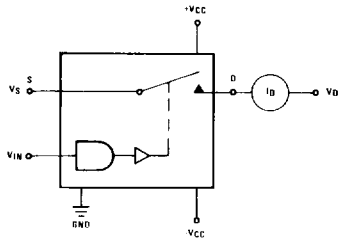
* PDA applies to Subgroup 1 only.

Test Circuits

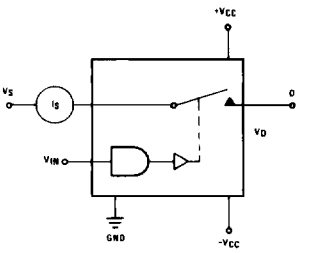
INPUT LEAKAGE CURRENT



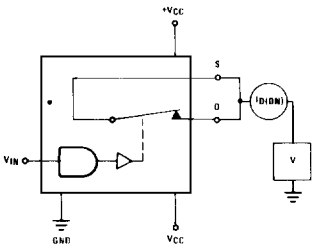
$I_{D(OFF)}$



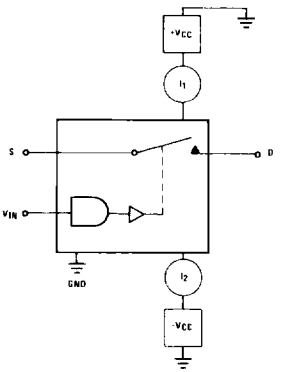
$I_{S(OFF)}$



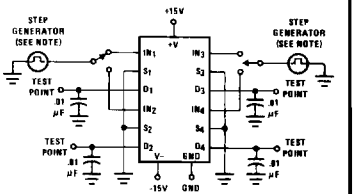
$I_{D(ON)}$



SUPPLY CURRENTS

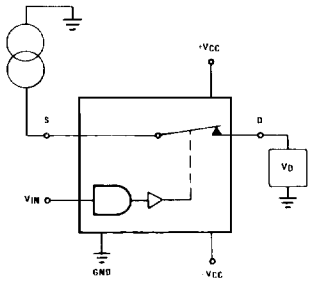


CHARGE TRANSFER ERROR

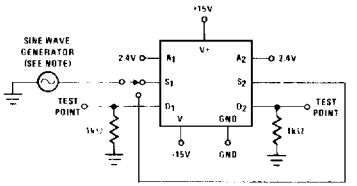


NOTE:
The pulse generator has the following characteristics: V_{GEN} = 0 to 3V, rise time ≤ 20ns, fall time ≤ 20ns, PRR = 100kHz.

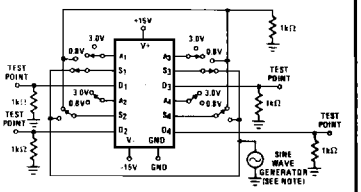
R_{DS}



OFF CHANNEL ISOLATION



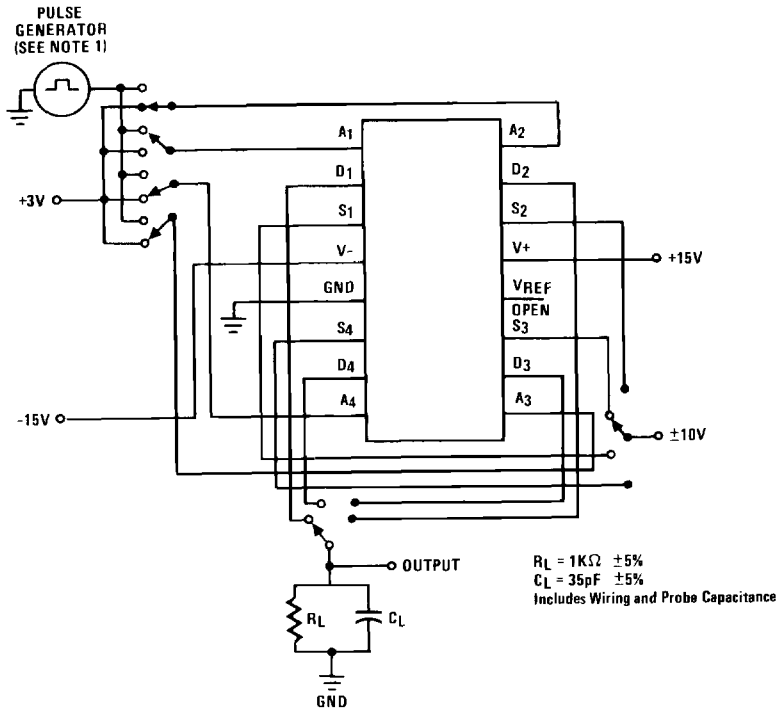
CROSSTALK BETWEEN CHANNELS



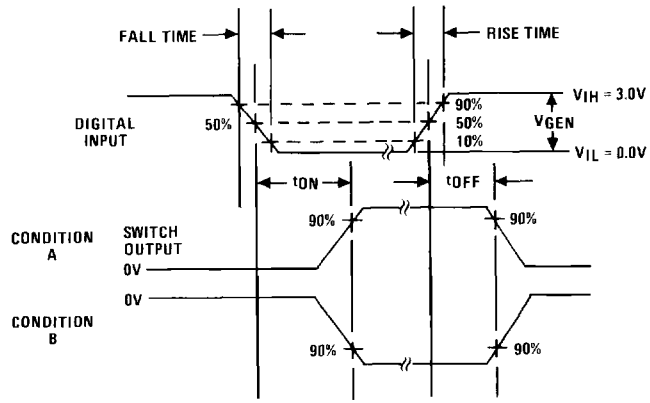
NOTE:
The pulse generator has the following characteristics: V_{GEN} = $1V_{p-p}$, frequency = 100kHz.

See Test Tech Brief For Additional Information

Switching Waveforms



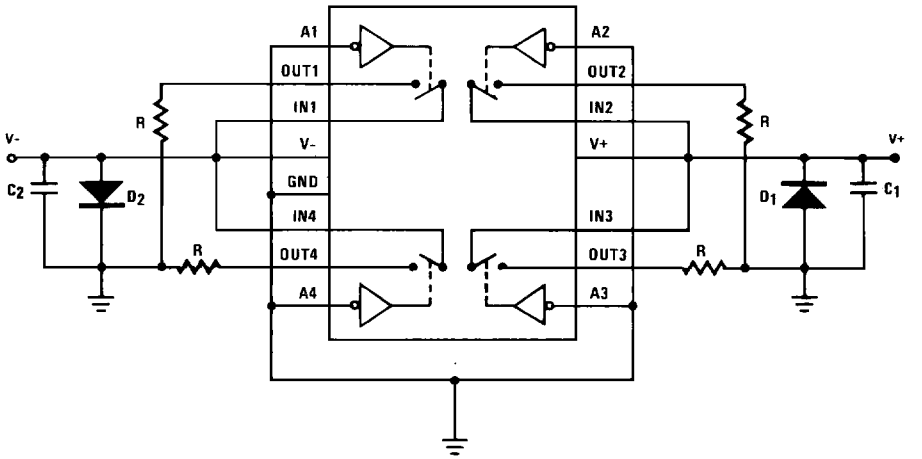
NOTES: 1. The pulse generator has the following characteristics: V_{GEN} = 3.0V, $t_{THL} \leq$ 20ns.
2. See Table 2 for complete terminal conditions.



NOTE: Rise time and fall time ≤ 20ns

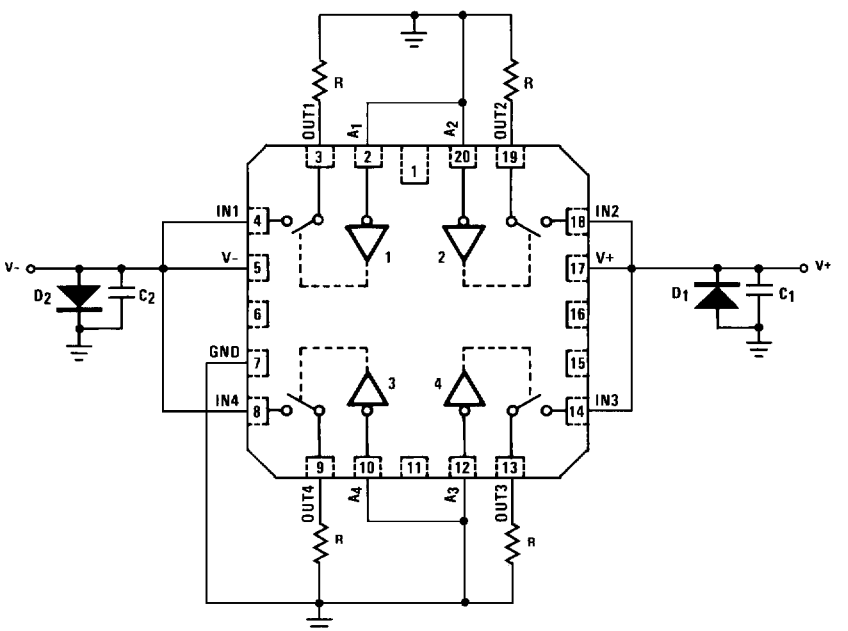
Burn-In Circuits

HI-201HS/883 CERAMIC DIP



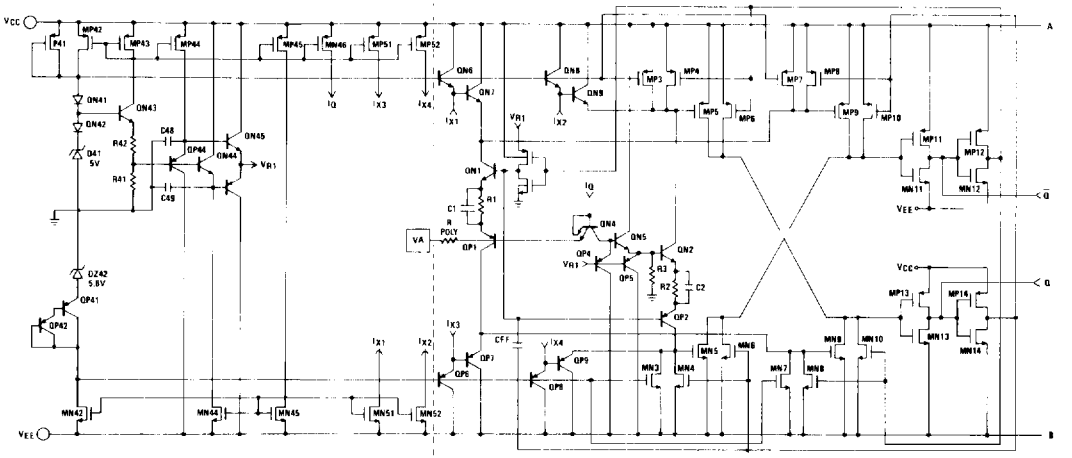
NOTES:
R = 10KΩ, 5%, 1/4 or 1/2W
$C_1 = C_2 = 0.1\mu F$ (one per row) or $.01\mu F$ (one per socket)
$D_1 = D_2$ = IN4002 or equivalent (one per board)
$|(V+) - (V-)| = 30V$

HI-201HS/883 CERAMIC LCC

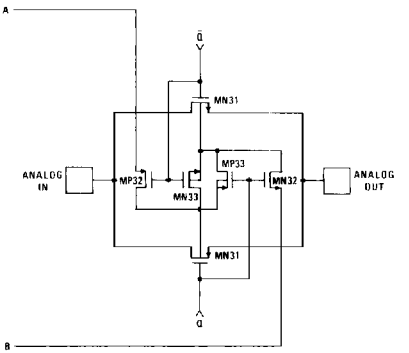


Schematic Diagrams

REFERENCE/LEVEL SHIFTER



SWITCH CELL



Die Characteristics

DIE DIMENSIONS:
92 x 111 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

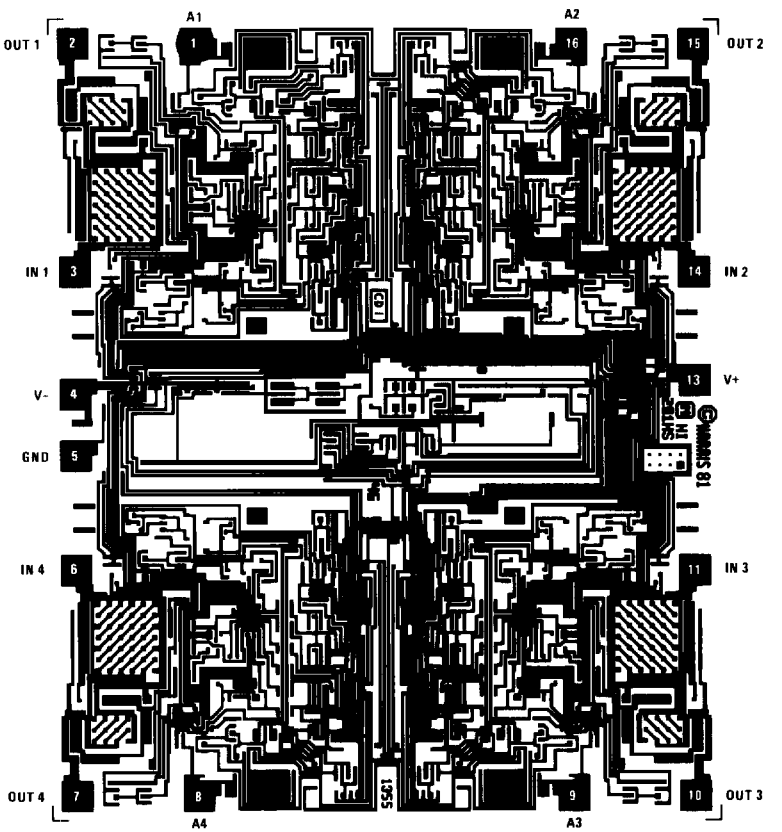
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
$4.5 \times 10^5 A/cm^2$ at 25mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

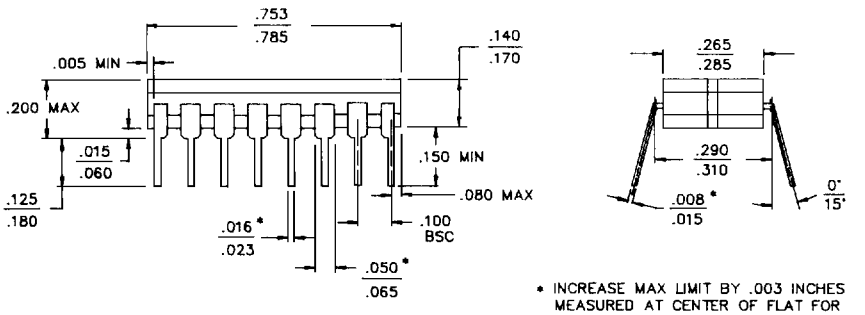
Metallization Mask Layout

HI-201HS/883



Packaging†

16 PIN CERAMIC DIP

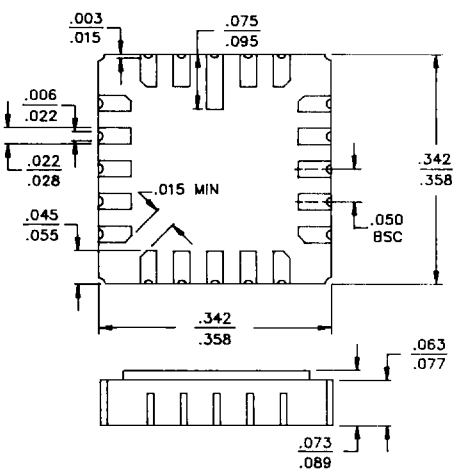


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

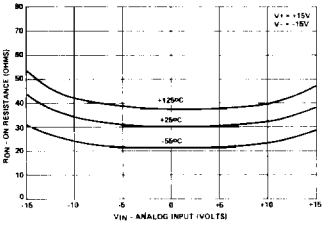
NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

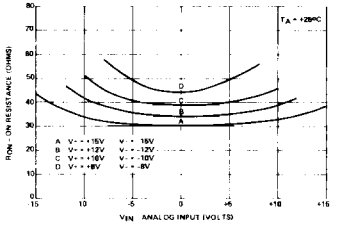
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$ $V_{AH} = 3.0V$, $V_{AL} = 0.8V$

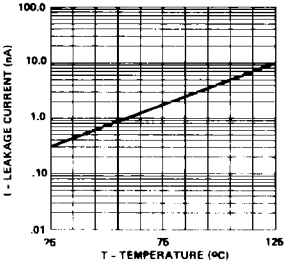
ON RESISTANCE vs. ANALOG SIGNAL LEVEL AND TEMPERATURE



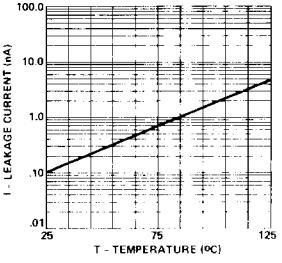
ON RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



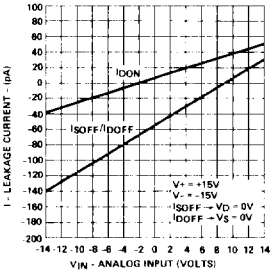
$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE



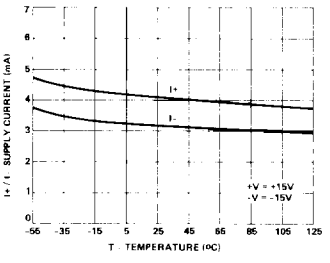
$I_{D(ON)}$ vs. TEMPERATURE



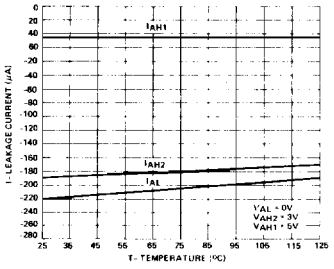
LEAKAGE CURRENT vs. ANALOG INPUT VOLTAGE



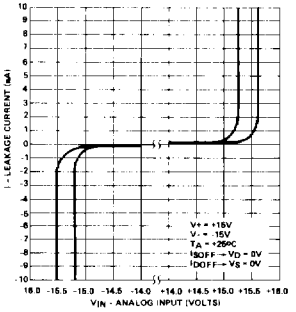
SUPPLY CURRENT vs. TEMPERATURE



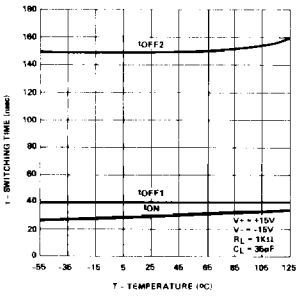
DIGITAL INPUT LEAKAGE CURRENT vs. TEMPERATURE



LEAKAGE CURRENT vs. ANALOG INPUT VOLTAGE ($V_{IN} \geq +14V$, $V_{IN} \geq -14V$)



SWITCHING TIME vs. TEMPERATURE

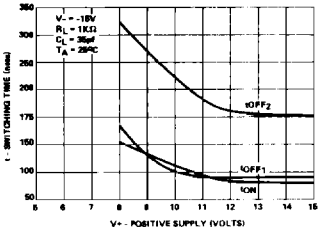


DESIGN INFORMATION (Continued)

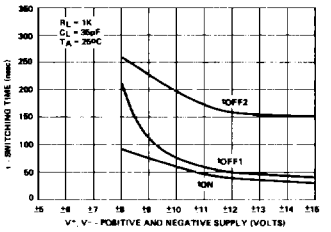
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$ $V_{AH} = 3.0V$, $V_{AL} = 0.8V$

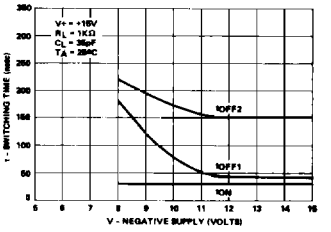
SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE



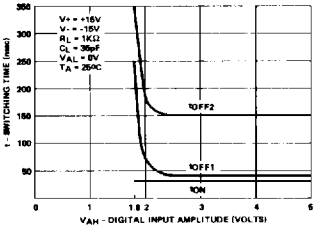
SWITCHING TIME vs. POSITIVE AND NEGATIVE SUPPLY VOLTAGE



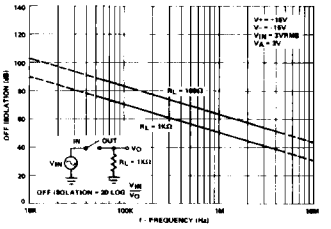
SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



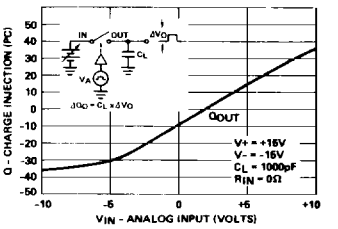
SWITCHING TIME vs. INPUT LOGIC AMPLITUDE



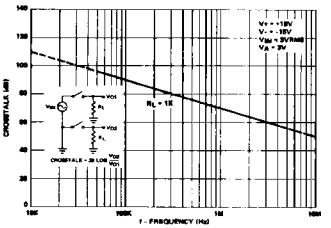
OFF ISOLATION vs. FREQUENCY



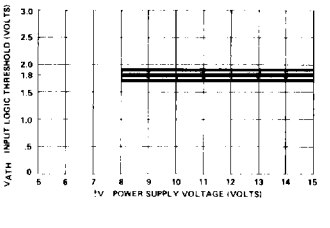
CHARGE INJECTION vs. ANALOG INPUT



CROSSTALK vs. FREQUENCY



INPUT SWITCHING THRESHOLD vs. POSITIVE AND NEGATIVE SUPPLY VOLTAGES



CAPACITANCE vs. ANALOG INPUT