# IS89LV51

# CMOS SINGLE CHIP LOW VOLTAGE 8-BIT MICROCONTROLLER with 4-Kbytes of FLASH

**ISSI®**

## FEATURES

- 80C51 based architecture
- 4-Kbytes of on-chip Reprogrammable Flash Memory
- 128 x 8 RAM
- Two 16-bit Timer/Counters
- Full duplex serial channel
- Boolean processor
- Four 8-bit I/O ports, 32 I/O lines
- Memory addressing capability
  - 64K ROM and 64K RAM
- Program memory lock
  - Lock bits (3)
- Power save modes:
  - Idle and power-down
- Six interrupt sources
- Most instructions execute in 0.3 µs
- CMOS and TTL compatible
- Maximum speed: 40 MHz @ Vcc = 3.3V
- Operating Range: 3.3V to 5V, ± 10%
- Industrial temperature available
- Packages available:
  - 40-pin DIP
  - 44-pin PLCC
  - 44-PIN PQFP

## GENERAL DESCRIPTION

The *ISSI* IS89LV51 is a high-performance microcontroller fabricated using high-density CMOS technology. The CMOS IS89LV51 is functionally compatible with the industry standard 80C51 microcontrollers.

The IS89LV51 is designed with 4-Kbytes of Flash memory, 128 x 8 RAM; 32 programmable I/O lines; a serial I/O port for either multiprocessor communications, I/O expansion or full duplex UART; two 16-bit timer/counters; an six-source, two-priority-level, nested interrupt structure; and an on-chip oscillator and clock circuit. The IS89LV51 can be expanded using standard TTL compatible memory.
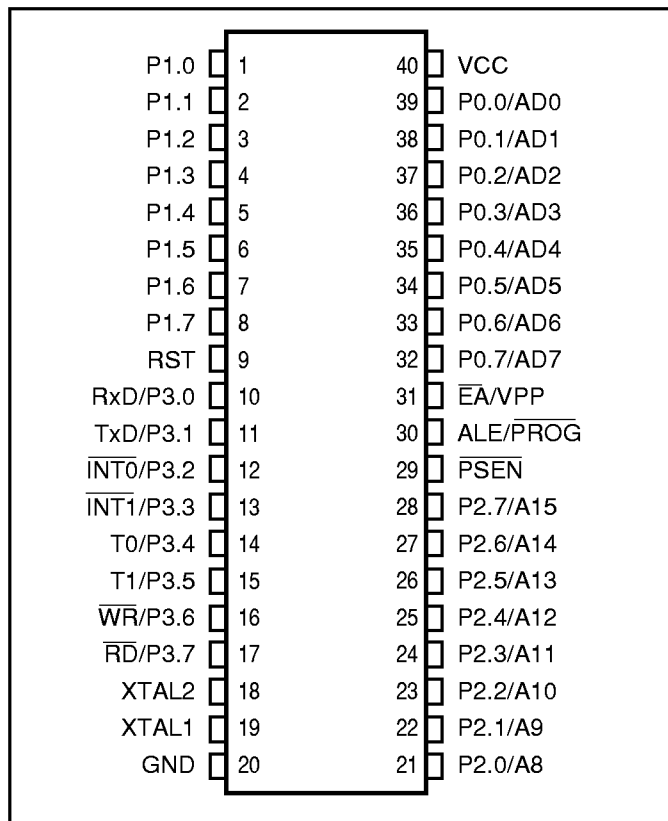
| | | | |
|---|---|---|---|
| P1.0 | 1 | 40 | VCC |
| P1.1 | 2 | 39 | P0.0/AD0 |
| P1.2 | 3 | 38 | P0.1/AD1 |
| P1.3 | 4 | 37 | P0.2/AD2 |
| P1.4 | 5 | 36 | P0.3/AD3 |
| P1.5 | 6 | 35 | P0.4/AD4 |
| P1.6 | 7 | 34 | P0.5/AD5 |
| P1.7 | 8 | 33 | P0.6/AD6 |
| RST | 9 | 32 | P0.7/AD7 |
| RxD/P3.0 | 10 | 31 | $\overline{EA}$/VPP |
| TxD/P3.1 | 11 | 30 | ALE/$\overline{PROG}$ |
| $\overline{INT0}$/P3.2 | 12 | 29 | $\overline{PSEN}$ |
| $\overline{INT1}$/P3.3 | 13 | 28 | P2.7/A15 |
| T0/P3.4 | 14 | 27 | P2.6/A14 |
| T1/P3.5 | 15 | 26 | P2.5/A13 |
| $\overline{WR}$/P3.6 | 16 | 25 | P2.4/A12 |
| $\overline{RD}$/P3.7 | 17 | 24 | P2.3/A11 |
| XTAL2 | 18 | 23 | P2.2/A10 |
| XTAL1 | 19 | 22 | P2.1/A9 |
| GND | 20 | 21 | P2.0/A8 |

**Figure 1. IS89LV51 Pin Configuration: 40-pin PDIP**

INDEX

| | P1.4 | P1.3 | P1.2 | P1.1 | P1.0 | NC | VCC | P0.0/AD0 | P0.1/AD1 | P0.2/AD2 | P0.3/AD3 |

P1.5 ☐ 7      39 ☐ P0.4/AD4

P1.6 ☐ 8      38 ☐ P0.5/AD5

P1.7 ☐ 9      37 ☐ P0.6/AD6

RST ☐ 10      36 ☐ P0.7/AD7

RxD/P3.0 ☐ 11      35 ☐ $\overline{EA}$/VPP

NC ☐ 12    TOP VIEW    34 ☐ NC

TxD/P3.1 ☐ 13      33 ☐ ALE/$\overline{PROG}$

$\overline{INT0}$/P3.2 ☐ 14      32 ☐ $\overline{PSEN}$

$\overline{INT1}$/P3.3 ☐ 15      31 ☐ P2.7/A15

T0/P3.4 ☐ 16      30 ☐ P2.6/A14

T1/P3.5 ☐ 17      29 ☐ P2.5/A13

| 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 |
| $\overline{WR}$/P3.6 | $\overline{RD}$/P3.7 | XTAL2 | XTAL1 | GND | NC | A8/P2.0 | A9/P2.1 | A10/P2.2 | A11/P2.3 | A12/P2.4 |
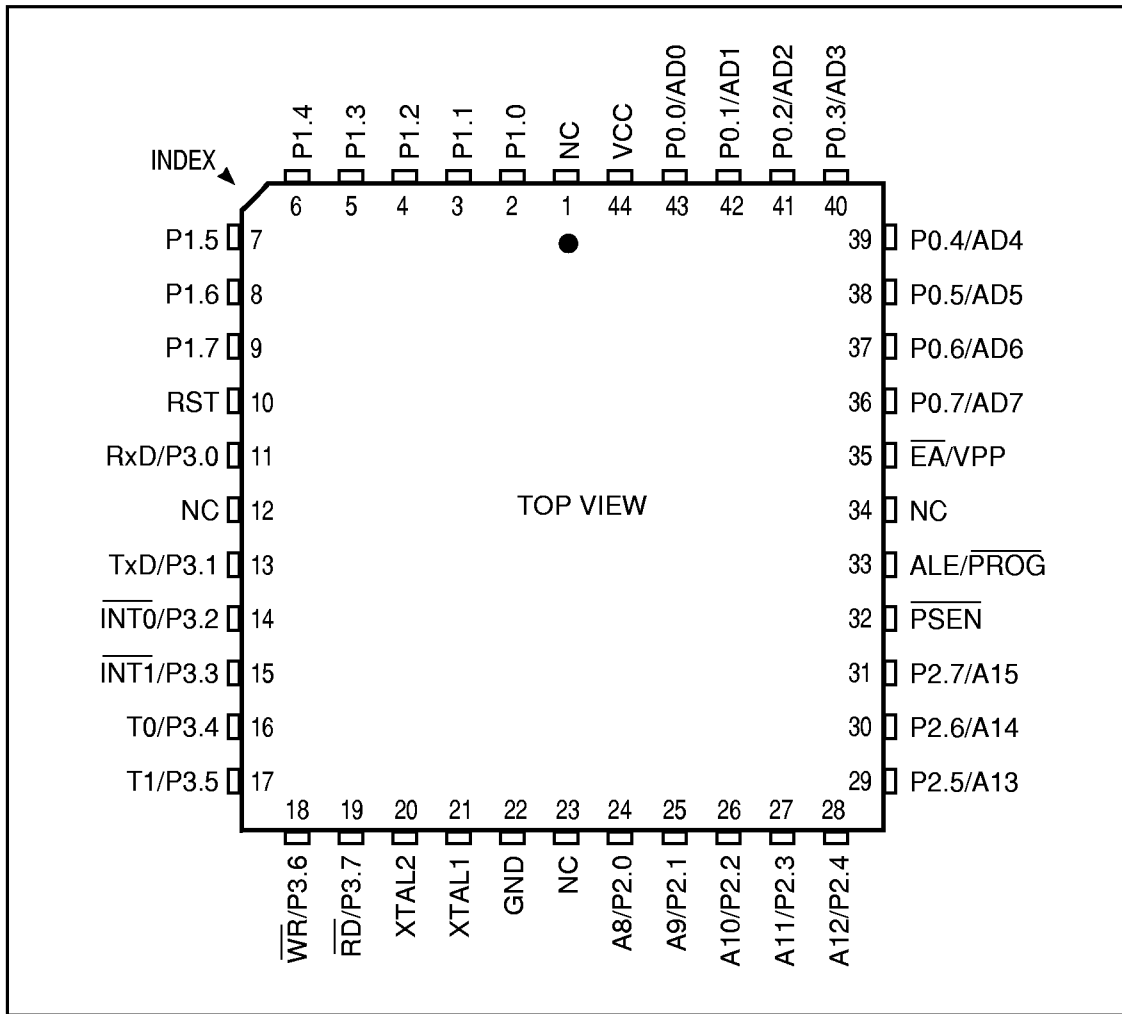
**Figure 2. IS89LV51 Pin Configuration: 44-pin PLCC**
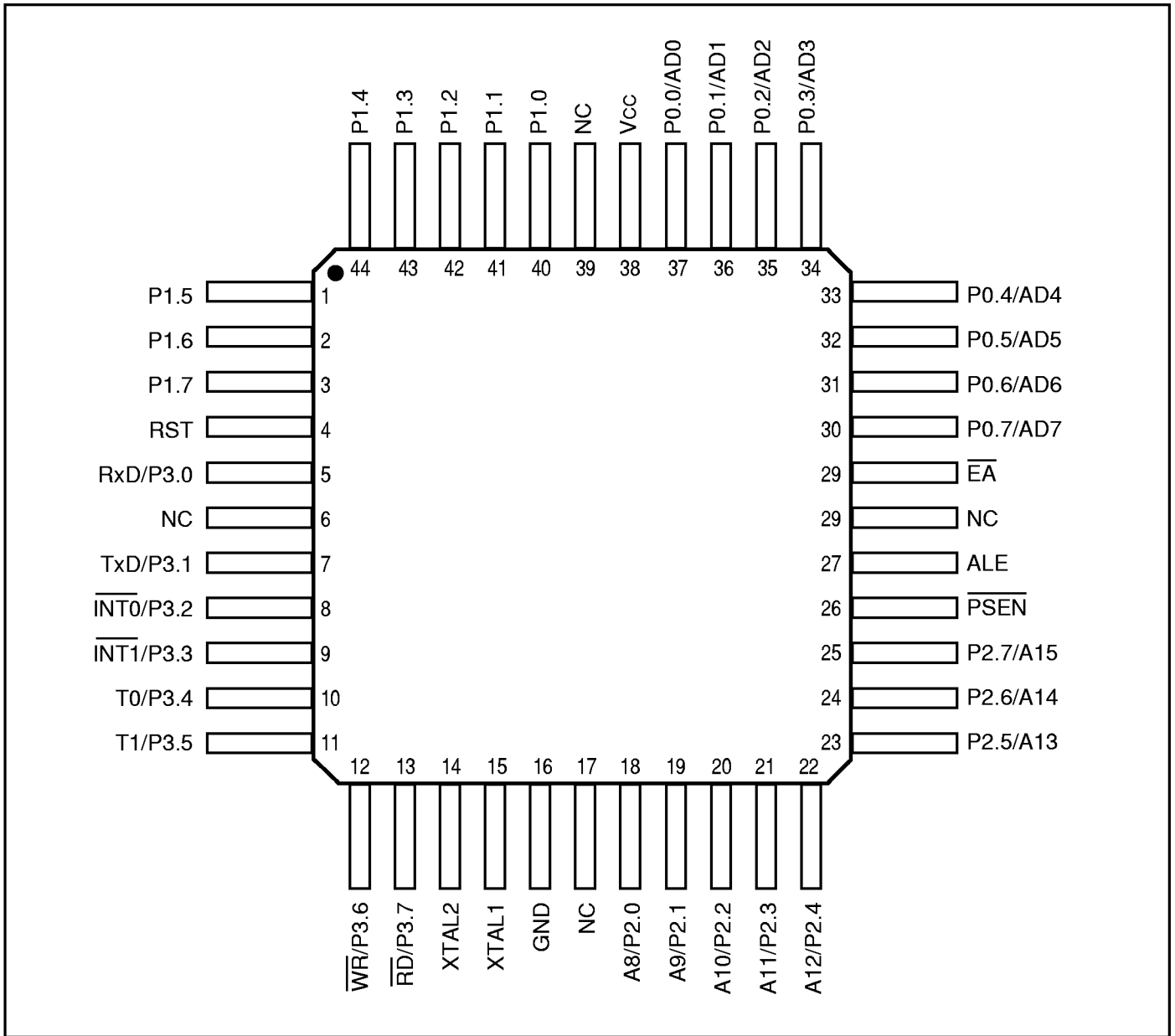
**Figure 3. IS89LV51 Pin Configuration: 44-pin PQFP**
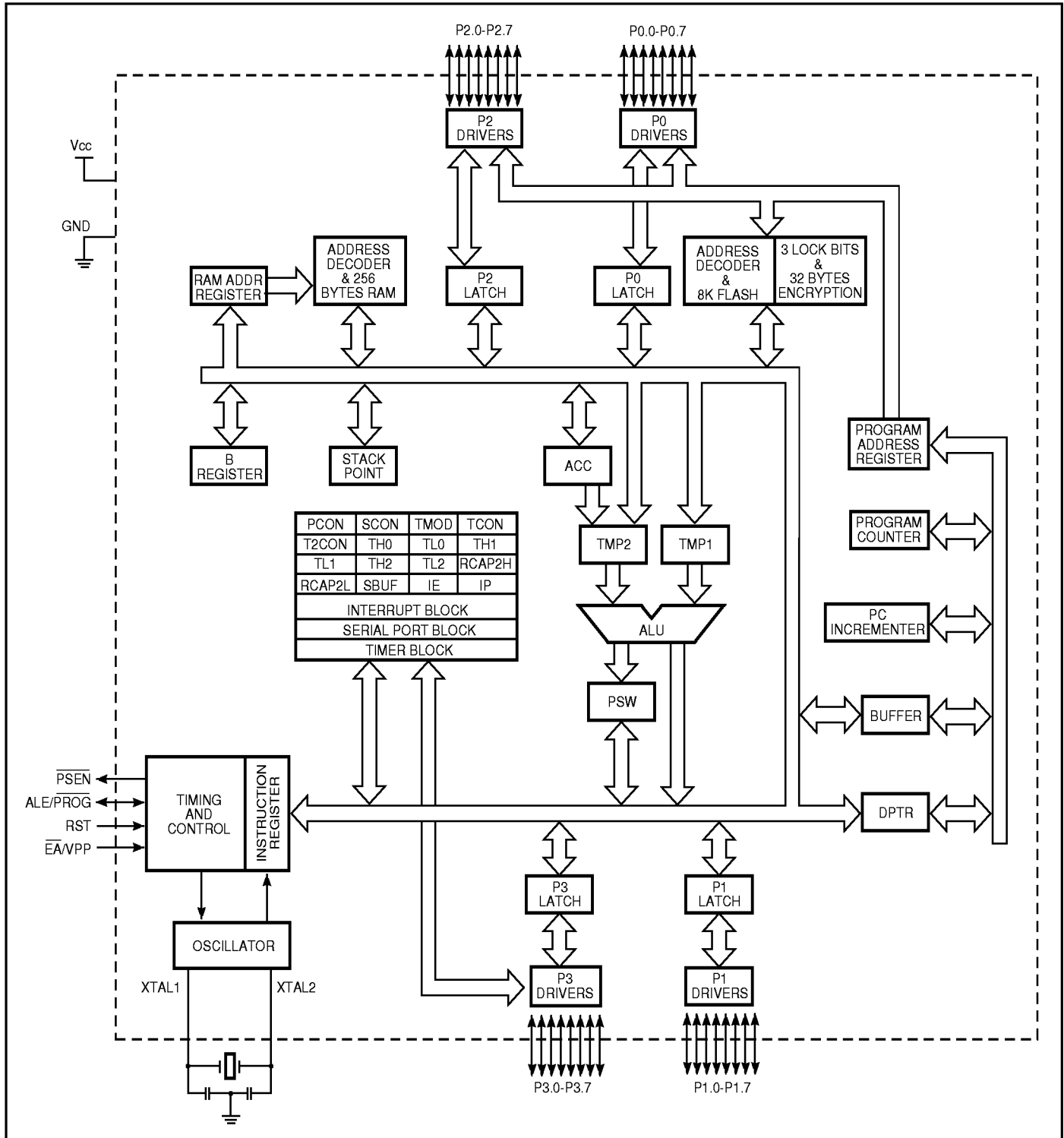
**Figure 4.  IS89LV51 Block Diagram**

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## Table 1. Detailed Pin Description

| Symbol | PDIP | PLCC | PQFP | I/O | Name and Function |
|---|---|---|---|---|---|
| ALE/$\overline{\text{PROG}}$ | 30 | 33 | 27 | I/O | **Address Latch Enable:** Output pulse for latching the low byte of the address during an address to the external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the Program Pulse input ($\overline{\text{PROG}}$) during Flash programming. |
| $\overline{\text{EA}}$/V$_{PP}$ | 31 | 35 | 29 | I | **External Access enable:** $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to FFFFH. If $\overline{\text{EA}}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 0FFFH. This also receives the 12V programming enable voltage (V$_{PP}$) during Flash programming. |
| P0.0-P0.7 | 39-32 | 43-36 | 37-30 | I/O | **Port 0:** Port 0 is an 8-bit open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pullups when emitting 1s.<br><br>Port 0 also receives the code bytes during programmable memory programming and outputs the code bytes during program verification. External pullups are required during program verification. |
| P1.0-P1.7 | 1-8 | 2-9 | 40-44<br>1-3 | I/O | **Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I$_{IL}$). The Port 1 output buffers can sink/source four TTL inputs.<br><br>Port 1 also receives the low-order address byte during Flash programming and verification. |
| P2.0-P2.7 | 21-28 | 24-31 | 18-25 | I/O | **Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I$_{IL}$). Port 2 emits the high order address byte during fetches from external program memory and during accesses to external data memory that used 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ Ri [i = 0, 1]), Port 2 emits the contents of the P2 Special Function Register.<br><br>Port 2 also receives the high-order bits and some control signals during Flash programming and verification. P2.6 and P2.7 are the control signals while the chip programs and erases. |

**Table 1. Detailed Pin Description** *(continued)*

| Symbol | PDIP | PLCC | PQFP | I/O | Name and Function |
|---|---|---|---|---|---|
| P3.0-P3.7 | 10-17 | 11, 13-19 | 5, 7-13 | I/O | **Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I<sub>IL</sub>).<br><br>Port 3 also serves the special features of the IS89LV51, as listed below: |
| | 10 | 11 | 5 | I | **RxD (P3.0):** Serial input port. |
| | 11 | 13 | 7 | O | **TxD (P3.1):** Serial output port. |
| | 12 | 14 | 8 | I | $\overline{\text{INT0}}$ **(P3.2):** External interrupt 0. |
| | 13 | 15 | 9 | I | $\overline{\text{INT1}}$ **(P3.3):** External interrupt 1. |
| | 14 | 16 | 10 | I | **T0 (P3.4):** Timer 0 external input. |
| | 15 | 17 | 11 | I | **T1 (P3.5):** Timer 1 external input. |
| | 16 | 18 | 12 | O | $\overline{\text{WR}}$ **(P3.6):** External data memory write strobe. |
| | 17 | 19 | 13 | O | $\overline{\text{RD}}$ **(P3.7):** External data memory read strobe. |
| $\overline{\text{PSEN}}$ | 29 | 32 | 26 | O | **Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory. |
| RST | 9 | 10 | 4 | I | **Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal MOS resistor to GND permits a power-on reset using only an external capacitor connected to Vcc. |
| XTAL 1 | 19 | 21 | 15 | I | **Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. |
| XTAL 2 | 18 | 20 | 14 | O | **Crystal 2:** Output from the inverting oscillator amplifier. |
| GND | 20 | 22 | 16 | I | **Ground:** 0V reference. |
| Vcc | 40 | 44 | 38 | I | **Power Supply:** This is the power supply voltage for operation. |

## OPERATING DESCRIPTION

The detail description of the IS89LV51 included in this description are:

• **Memory Map and Registers**

• **Timer/Counters**

• **Serial Interface**

• **Interrupt System**

• **Other Information**

• **Flash Memory**

## MEMORY MAP AND REGISTERS

### Memory

The IS89LV51 has separate address spaces for program and data memory. The program and data memory can be up to 64K bytes long. The lower 4K program memory can reside on-chip. Figure 5 shows a map of the IS89LV51 program and data memory.

The IS89LV51 has 128 bytes of on-chip RAM, plus numbers of special function registers. The lower 128 bytes can be accessed either by direct addressing or by indirect addressing. Figure 6 shows internal data memory organization and SFR Memory Map.

The lower 128 bytes of RAM can be divided into three segments as listed below and shown in Figure 7.

1. **Register Banks 0-3:** locations 00H through 1FH (32 bytes). The device after reset defaults to register bank 0. To use the other register banks, the user must select them in software. Each register bank contains eight 1-byte registers R0-R7. Reset initializes the stack point to location 07H, and is incremented once to start from 08H, which is the first register of the second register bank.

2. **Bit Addressable Area:** 16 bytes have been assigned for this segment 20H-2FH. Each one of the 128 bits of this segment can be directly addressed (0-7FH). Each of the 16 bytes in this segment can also be addressed as a byte.

3. **Scratch Pad Area:** 30H-7FH are available to the user as data RAM. However, if the data pointer has been initialized to this area, enough bytes should be left aside to prevent SP data destruction.
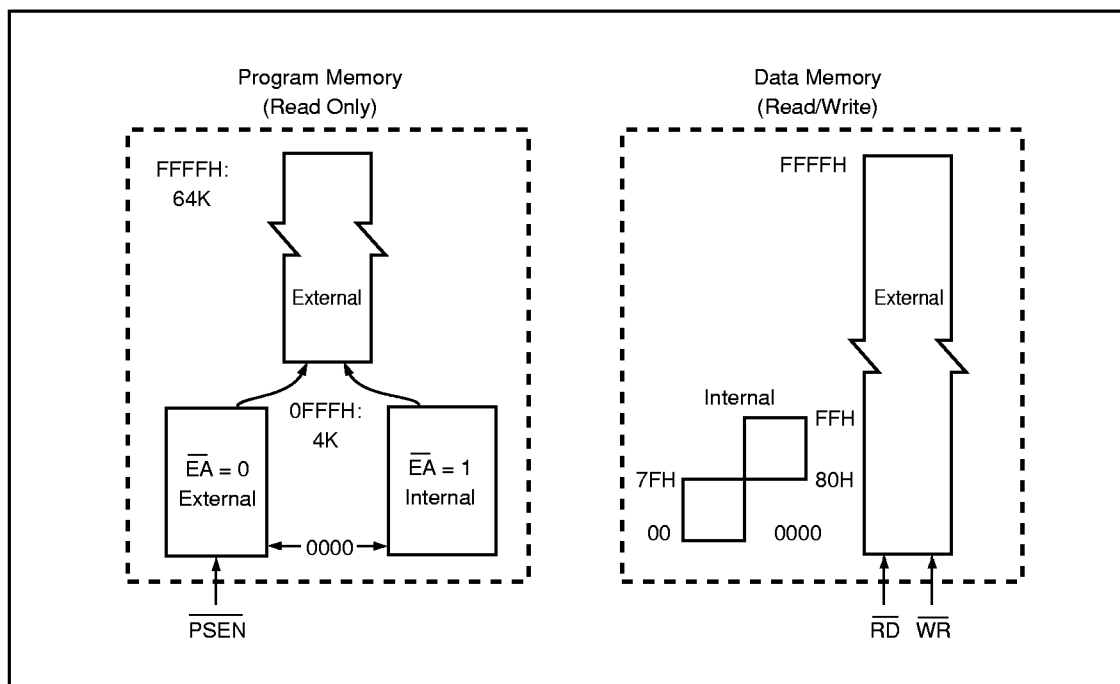


Figure 5. IS89LV51 Program and Data Memory Structure

## SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFR's) are located in upper 128 Bytes direct addressing area. The SFR Memory Map in Figure 6 shows that.

Not all of the addresses are occupied. Unoccupied addresses are not implemented on the chip. Read accesses to these addresses in general return random data, and write accesses have no effect.

User software should not write 1s to these unimplemented locations, since they may be used in future microcontrollers to invoke new features. In that case, the reset or inactive values of the new bits will always be 0, and their active values will be 1.

The functions of the SFRs are outlined in the following sections, and detailed in Table 2.

### Accumulator (ACC)
ACC is the Accumulator register. The mnemonics for Accumulator-specific instructions, however, refer to the Accumulator simply as A.

### B Register (B)
The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

**Program Status Word (PSW).** The PSW register contains program status information.
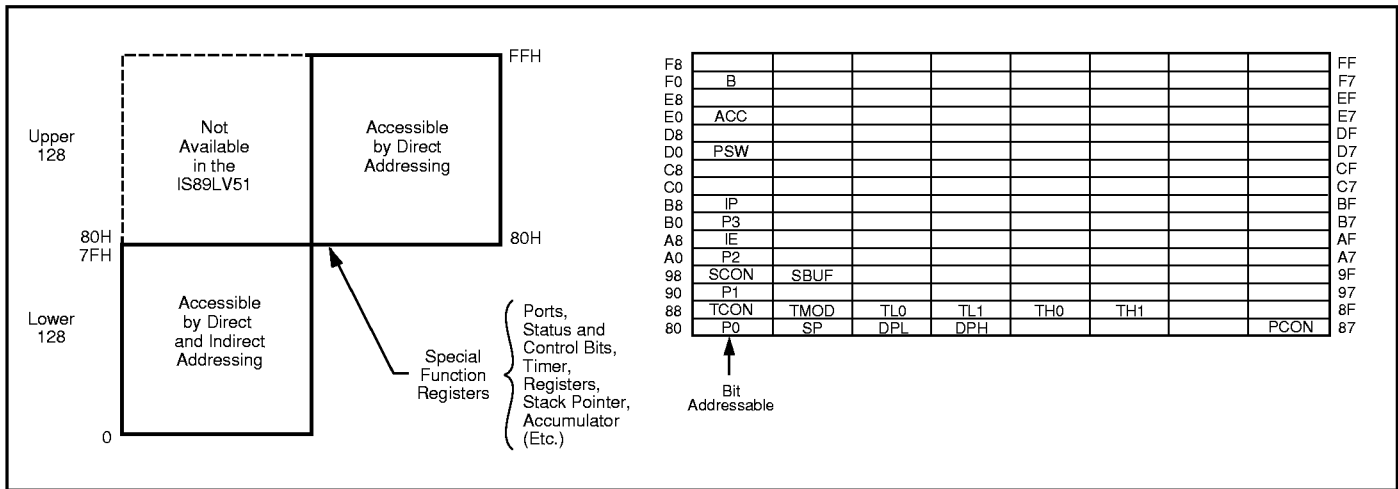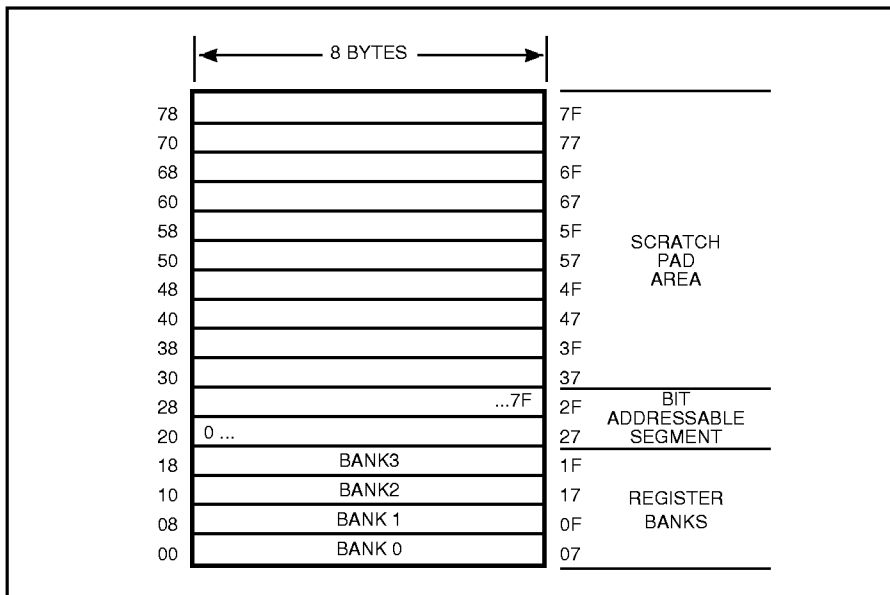


**Figure 6. Internal Data Memory and SFR Memory Map**



**Figure 7. Lower 128 Bytes of Internal RAM**

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## SPECIAL FUNCTION REGISTERS

*(Continued)*

### Stack Pointer (SP)
The Stack Pointer Register is eight bits wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at location 08H.

### Data Pointer (DPTR)
The Data Pointer consists of a high byte (DPH) and a low byte (DPL). Its function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

### Ports 0 To 3
P0, P1, P2, and P3 are the SFR latches of Ports 0, 1, 2, and 3, respectively.

### Serial Data Buffer (SBUF)
The Serial Data Buffer is actually two separate registers, a transmit buffer and a receive buffer register. When data is moved to SBUF, it goes to the transmit buffer, where it is held for serial transmission. (Moving a byte to SBUF initiates the transmission.) When data is moved from SBUF, it comes from the receive buffer.

### Timer Registers
Register pairs (TH0, TL0) and (TH1, TL1) are the 16-bit Counter registers for Timer/Counters 0 and 1, respectively.

### Control Registers
Special Function Registers IP, IE, TMOD, TCON, SCON, and PCON contain control and status bits for the interrupt system, the Timer/Counters, and the serial port. They are described in later sections of this chapter.

## Table 2. Special Function Registers

| Symbol | Description | Direct Address | Bit Address, Symbol, or Alternative Port Function | | | | | | | | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ACC[1] | Accumulator | E0H | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 | 00H |
| B[1] | B register | F0H | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | 00H |
| DPH | Data pointer (DPTR) high | 83H | | | | | | | | | 00H |
| DPL | Data pointer (DPTR) low | 82H | | | | | | | | | 00H |
| IE[1] | Interrupt enable | A8H | **AF**<br>EA | **AE**<br>— | **AD**<br>— | **AC**<br>ES | **AB**<br>ET1 | **AA**<br>EX1 | **A9**<br>ET0 | **A8**<br>EX0 | 0XX00000B |
| IP[1] | Interrupt priority | B8H | **BF**<br>— | **BE**<br>— | **BD**<br>— | **BC**<br>PS | **BB**<br>PT1 | **BA**<br>PX1 | **B9**<br>PT0 | **B8**<br>PX0 | XXX00000B |
| P0[1] | Port 0 | 80H | **87**<br>P0.7<br>AD7 | **86**<br>P0.6<br>AD6 | **85**<br>P0.5<br>AD5 | **84**<br>P0.4<br>AD4 | **83**<br>P0.3<br>AD3 | **82**<br>P0.2<br>AD2 | **81**<br>P0.1<br>AD1 | **80**<br>P0.0<br>AD0 | FFH |
| P1[1] | Port 1 | 90H | **97**<br>P1.7 | **96**<br>P1.6 | **95**<br>P1.5 | **94**<br>P1.4 | **93**<br>P1.3 | **92**<br>P1.2 | **91**<br>P1.1 | **90**<br>P1.0 | FFH |
| P2[1] | Port 2 | A0H | **A7**<br>P2.7<br>AD15 | **A6**<br>P2.6<br>AD14 | **A5**<br>P2.5<br>AD13 | **A4**<br>P2.4<br>AD12 | **A3**<br>P2.3<br>AD11 | **A2**<br>P2.2<br>AD10 | **A1**<br>P2.1<br>AD9 | **A0**<br>P2.0<br>AD8 | FFH |
| P3[1] | Port 3 | B0H | **B7**<br>P3.7<br>$\overline{RD}$ | **B6**<br>P3.6<br>$\overline{WR}$ | **B5**<br>P3.5<br>T1 | **B4**<br>P3.4<br>T0 | **B3**<br>P3.3<br>$\overline{INT1}$ | **B2**<br>P3.2<br>$\overline{INT0}$ | **B1**<br>P3.1<br>TXD | **B0**<br>P3.0<br>RXD | FFH |
| PCON | Power control | 87H | SMOD | — | — | — | GF1 | GF0 | PD | IDL | 0XXX0000B |
| PSW[1] | Program status word | D0H | **D7**<br>CY | **D6**<br>AC | **D5**<br>F0 | **D4**<br>RS1 | **D3**<br>RS0 | **D2**<br>OV | **D1**<br>— | **D0**<br>P | 00H |
| SBUF | Serial data buffer | 99H | | | | | | | | | XXXXXXXXB |
| SCON[1] | Serial controller | 98H | **9F**<br>SM0 | **9E**<br>SM1 | **9D**<br>SM2 | **9C**<br>REN | **9B**<br>TB8 | **9A**<br>RB8 | **99**<br>TI | **98**<br>RI | 00H |
| SP | Stack pointer | 81H | | | | | | | | | 07H |
| TCON[1] | Timer control | 88H | **8F**<br>TF1 | **8E**<br>TR1 | **8D**<br>TF0 | **8C**<br>TR0 | **8B**<br>IE1 | **8A**<br>IT1 | **89**<br>IE0 | **88**<br>IT0 | 00H |
| TMOD | Timer mode | 89H | GATE | C/$\overline{T}$ | M1 | M0 | GATE | C/$\overline{T}$ | M1 | M0 | 00H |
| TH0 | Timer high 0 | 8CH | | | | | | | | | 00H |
| TH1 | Timer high 1 | 8DH | | | | | | | | | 00H |
| TL0 | Timer low 0 | 8AH | | | | | | | | | 00H |
| TL1 | Timer low 1 | 8BH | | | | | | | | | 00H |

**Notes:**
1. Denotes bit addressable.

The detail description of each bit is as follows:

## PSW:

**Program Status Word. Bit Addressable.**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CY | AC | F0 | RS1 | RS0 | OV | — | P |

**Register Description:**

| | | |
|---|---|---|
| CY | PSW.7 | Carry flag. |
| AC | PSW.6 | Auxiliary carry flag. |
| F0 | PSW.5 | Flag 0 available to the user for general purpose. |
| RS1 | PSW.4 | Register bank selector bit 1.[1] |
| RS0 | PSW.3 | Register bank selector bit 0.[1] |
| OV | PSW.2 | Overflow flag. |
| — | PSW.1 | Usable as a general purpose flag |
| P | PSW.0 | Parity flag. Set/Clear by hardware each instruction cycle to indicate an odd/even number of "1" bits in the accumulator. |

**Note:**
1. The value presented by RS0 and RS1 selects the corresponding register bank.

| RS1 | RS0 | Register Bank | Address |
|---|---|---|---|
| 0 | 0 | 0 | 00H-07H |
| 0 | 1 | 1 | 08H-0FH |
| 1 | 0 | 2 | 10H-17H |
| 1 | 1 | 3 | 18H-1FH |

## PCON:

**Power Control Register. Not Bit Addressable.**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SMOD | — | — | — | GF1 | GF0 | PD | IDL |

**Register Description:**

| | |
|---|---|
| SMOD | Double baud rate bit. If Timer 1 is used to generate baud rate and SMOD=1, the baud rate is doubled when the serial port is used in modes 1, 2, or 3. |
| — | Not implemented, reserve for future use.[1] |
| — | Not implemented, reserve for future use.[1] |
| — | Not implemented, reserve for future use.[1] |
| GF1 | General purpose flag bit. |
| GF0 | General purpose flag bit. |
| PD | Power-down bit. Setting this bit activates power-down mode. |
| IDL | Idle mode bit. Setting this bit activates idle mode. If 1s are written to PD and IDL at the same time, PD takes precedence. |

**Note:**
1. User software should not write 1s to reserved bits. These bits may be used in future products to invoke new features.

## IE:

**Interrupt Enable Register. Bit Addressable.**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EA | — | — | ES | ET1 | EX1 | ET0 | EX0 |

**Register Description:**

| | | |
|---|---|---|
| EA | IE.7 | Disable all interrupts. If EA=0, no interrupt will be acknowledged. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit. |
| — | IE.6 | Not implemented, reserve for future use.[5] |
| — | IE.5 | Not implemented, reserve for future use.[5] |
| ES | IE.4 | Enable or disable the serial port interrupt. |
| ET1 | IE.3 | Enable or disable the Timer 1 overflow interrupt. |
| EX1 | IE.2 | Enable or disable External Interrupt 1. |
| ET0 | IE.1 | Enable or disable the Timer 0 overflow interrupt. |
| EX0 | IE.0 | Enable or disable External Interrupt 0. |

**Note:** To use any of the interrupts in the 80C51 Family, the following three steps must be taken:
1. Set the EA (enable all) bit in the IE register to 1.
2. Set the coresponding individual interrupt enable bit in the IE register to 1.
3. Begin the interrupt service routine at the corresponding Vector Address of that interrupt (see below).

| Interrupt Source | Vector Address |
|---|---|
| IE0 | 0003H |
| TF0 | 000BH |
| IE1 | 0013H |
| TF1 | 001BH |
| RI & TI | 0023H |

4. In addition, for external interrupts, pins $\overline{INT0}$ and $\overline{INT1}$ (P3.2 and P3.3) must be set to 1, and depending on whether the interrupt is to be level or transition activated, bits IT0 or IT1 in the TCON register may need to be set to 0 or 1.
   ITX = 0 level activated (X = 0, 1)
   ITX = 1 transition activated
5. User software should not write 1s to reserved bits. These bits may be used in future products to invoke new features.

## IP:
**Interrupt Priority Register. Bit Addressable.**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| — | — | — | PS | PT1 | PX1 | PT0 | PX0 |

**Register Description:**

| | | |
|---|---|---|
| — | IP.7 | Not implemented, reserve for future use[3] |
| — | IP.6 | Not implemented, reserve for future use[3] |
| — | IP.5 | Not implemented, reserve for future use[3] |
| PS | IP.4 | Defines Serial Port interrupt priority level |
| PT1 | IP.3 | Defines Timer 1 interrupt priority level |
| PX1 | IP.2 | Defines External Interrupt 1 priority level |
| PT0 | IP.1 | Defines Timer 0 interrupt priority level |
| PX0 | IP.0 | Defines External Interrupt 0 priority level |

**Notes:**
1. In order to assign higher priority to an interrupt the coresponding bit in the IP register must be set to 1. While an interrupt service is in progress, it cannot be interrupted by a lower or same level interrupt.
2. Priority within level is only to resolve simultaneous requests of the same priority level. From high-to-low, interrupt sources are listed below:
   IE0
   TF0
   IE1
   TF1
   RI or TI
3. User software should not write 1s to reserved bits. These bits may be used in future products to invoke new features.

## TCON:
**Timer/Counter Control Register. Bit Addressable**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |

**Register Description:**

| | | |
|---|---|---|
| TF1 | TCON.7 | Timer 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as processor vectors to the interrupt service routine. |
| TR1 | TCON.6 | Timer 1 run control bit. Set/Cleared by software to turn Timer/Counter 1 ON/OFF. |
| TF0 | TCON.5 | Timer 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as processor vectors to the interrupt service routine. |
| TR0 | TCON.4 | Timer 0 run control bit. Set/Cleared by software to turn Timer/Counter 0 ON/OFF. |
| IE1 | TCON.3 | External Interrupt 1 edge flag. Set by hardware when the External Interrupt edge is detected. Cleared by hardware when interrupt is processed. |
| IT1 | TCON.2 | Interrupt 1 type control bit. Set/Cleared by software specify falling edge/low level triggered External Interrupt. |
| IE0 | TCON.1 | External Interrupt 0 edge flag. Set by hardware when the External Interrupt edge is detected. Cleared by hardware when interrupt is processed. |
| IT0 | TCON.0 | Interrupt 0 type control bit. Set/Cleared by software specify falling edge/low level triggered External Interrupt. |

## TMOD:
**Timer/Counter Mode Control Register.**
**Not Bit Addressable.**

| Timer 1 | | | | Timer 0 | | | |
|---------|---|---|---|---------|---|---|---|
| GATE | C/T̄ | M1 | M0 | GATE | C/T̄ | M1 | M0 |

| | |
|------|-----|
| GATE | When TRx (in TCON) is set and GATE=1, TIMER/COUNTERx will run only while $\overline{INTx}$ pin is high (hardware control). When GATE=0, TIMER/COUNTERx will run only while TRx=1 (software control). |
| C/T̄ | Timer or Counter selector. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin). |
| M1 | Mode selector bit.[1] |
| M0 | Mode selector bit.[1] |

**Note 1:**

| M1 | M0 | Operating Mode |
|----|----|----------------|
| 0 | 0 | Mode 0. (13-bit Timer) |
| 0 | 1 | Mode 1. (16-bit Timer/Counter) |
| 1 | 0 | Mode 2. (8-bit auto-load Timer/Counter) |
| 1 | 1 | Mode 3. (Splits Timer 0 into TL0 and TH0. TL0 is an 8-bit Timer/Counter controller by the standard Timer 0 control bits. TH0 is an 8-bit Timer and is controlled by Timer 1 control bits.) |
| 1 | 1 | Mode 3. (Timer/Counter 1 stopped). |

## SCON:
**Serial Port Control Register. Bit Addressable.**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI |

**Register Description:**

| | | |
|-----|--------|---|
| SM0 | SCON.7 | Serial port mode specifier.[1] |
| SM1 | SCON.6 | Serial port mode specifier.[1] |
| SM2 | SCON.5 | Enable the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1 then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2=1 then RI will not be activated if valid stop bit was not received. In mode 0, SM2 should be 0. |
| REN | SCON.4 | Set/Cleared by software to Enable/Disable reception. |
| TB8 | SCON.3 | The 9th bit that will be transmitted in mode 2 and 3. Set/Cleared by software. |
| RB8 | SCON.2 | In modes 2 and 3, RB8 is the 9th data bit that was received. In mode 1, if SM2=0, RB8 is the stop bit that was received. In mode 0, RB8 is not used. |
| TI | SCON.1 | Transmit interrupt flag. Set by hardware at the end of the eighth bit time in mode 0, or at the beginning of the stop bit in the other modes. Must be cleared by software. |
| RI | SCON.0 | Receive interrupt flag. Set by hardware at the end of the eighth bit time in mode 0, or halfway through the stop bit time in the other modes (except see SM2). Must be cleared by software. |

**Note 1:**

| SM0 | SM1 | MODE | Description | Baud Rate |
|-----|-----|------|-------------|-----------|
| 0 | 0 | 0 | Shift register | Fosc/12 |
| 0 | 1 | 1 | 8-bit UART | Variable |
| 1 | 0 | 2 | 9-bit UART | Fosc/64 or Fosc/32 |
| 1 | 1 | 3 | 9-bit UART | Variable |

## TIMER/COUNTERS

The IS89LV51 has two 16-bit Timer/Counter registers: Timer 0 and Timer 1. All two can be configured to operate either as Timers or event Counters.

As a Timer, the register is incremented every machine cycle. Thus, the register counts machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

As a Counter, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 and T1. The external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but it should be held for at least one full machine cycle to ensure that a given level is sampled at least once before it changes.

In addition to the Timer or Counter functions, Timer 0 and Timer 1 have four operating modes: 13-bit timer, 16-bit timer, 8-bit auto-reload, split timer.

## Timer 0 and Timer 1

The Timer or Counter function is selected by control bits C/$\overline{T}$ in the Special Function Regiser TMOD. These two Timer/Counters have four operating modes, which are selected by bit pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timer/Counters, but Mode 3 is different. The four modes are described in the following sections.

**Mode 0:**
Both Timers in Mode 0 are 8-bit Counters with a divide-by-32 prescaler. Figure 8 shows the Mode 0 operation as it applies to Timer 1.

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TF1. The counted input is enabled to the Timer when TR1 = 1 and either GATE = 0 or $\overline{INT1}$ = 1. Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INT1}$, to facilitate pulse width measurements. TR1 is a control bit in the Special Function Register TCON. Gate is in TMOD.

The 13-bit register consists of all eight bits of TH1 and the lower five bits of TL1. The upper three bits of TL1 are indeterminate and should be ignored. Setting the run flag (TR1) does not clear the registers.

Mode 0 operation is the same for Timer 0 as for Timer 1, except that TR0, TF0 and $\overline{INT0}$ replace the corresponding Timer 1 signals in Figure 8. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).
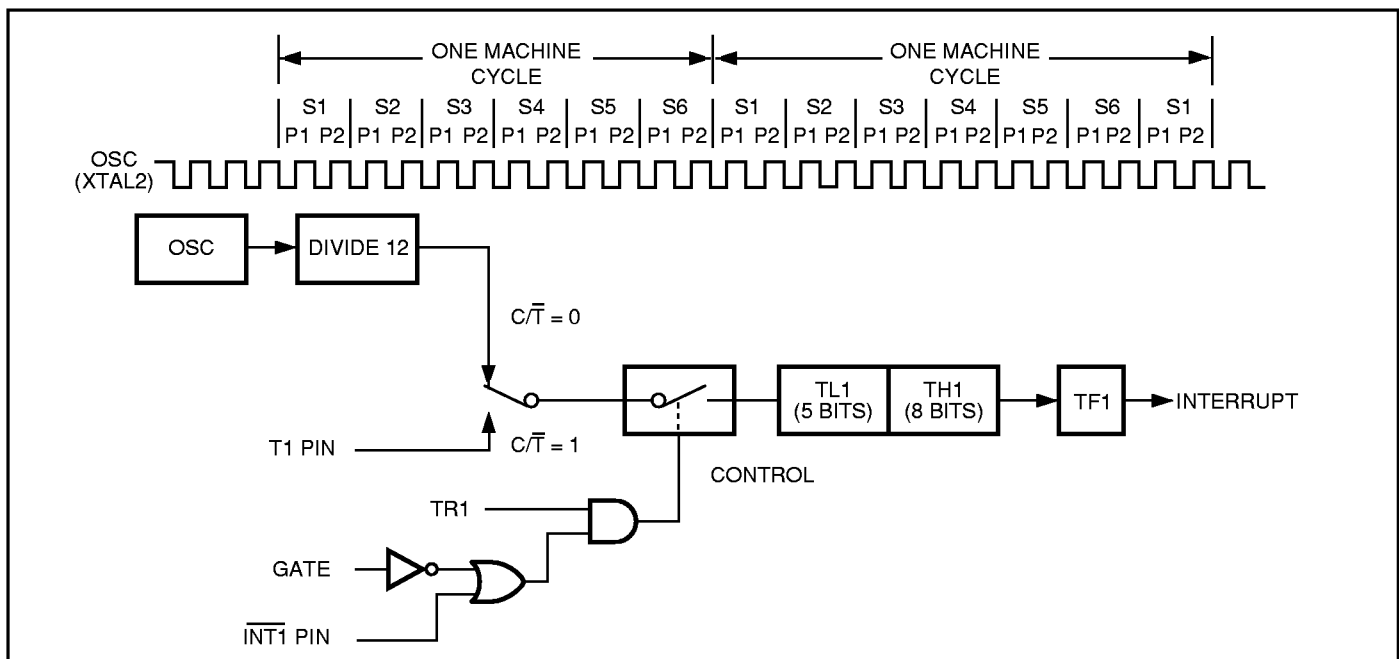


**Figure 8. Timer/Counter 1 Mode 0: 13-Bit Counter**

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**Mode 1:**

Mode 1 is the same as Mode 0, except that the Timer register is run with all 16 bits. The clock is applied to the combined high and low timer registers (TL1/TH1). As clock pulses are received, the timer counts up: 0000H, 0001H, 0002H, etc. An overflow occurs on the FFFFH-to-0000H overflow flag. The timer continues to count. The overflow flag is the TF1 bit in TCON that is read or written by software (see Figure 9).

**Mode 2:**

Mode 2 configures the Timer register as an 8-bit Counter (TL1) with automatic reload, as shown in Figure 10. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is preset by software. The reload leaves the TH1 unchanged. Mode 2 operation is the same for Timer/Counter 0.

**Mode 3:**

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 11. TL0 uses the Timer 0 control bits: C/T̄, GATE, TR0, INT0̄, and TF0. TH0 is locked into a timer function (counting machine cycles) and over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the Timer 1 interrupt.

Mode 3 is for applications requiring an extra 8-bit timer or counter. With Timer 0 in Mode 3, the IS89LV51 can appear to have three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3. In this case, Timer 1 can still be used by the serial port as a baud rate generator or in any application not requiring an interrupt.
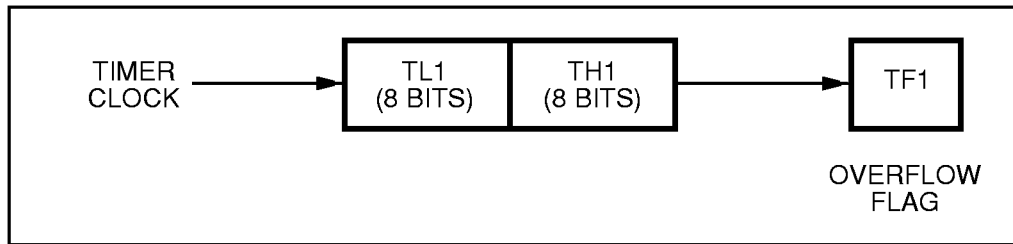


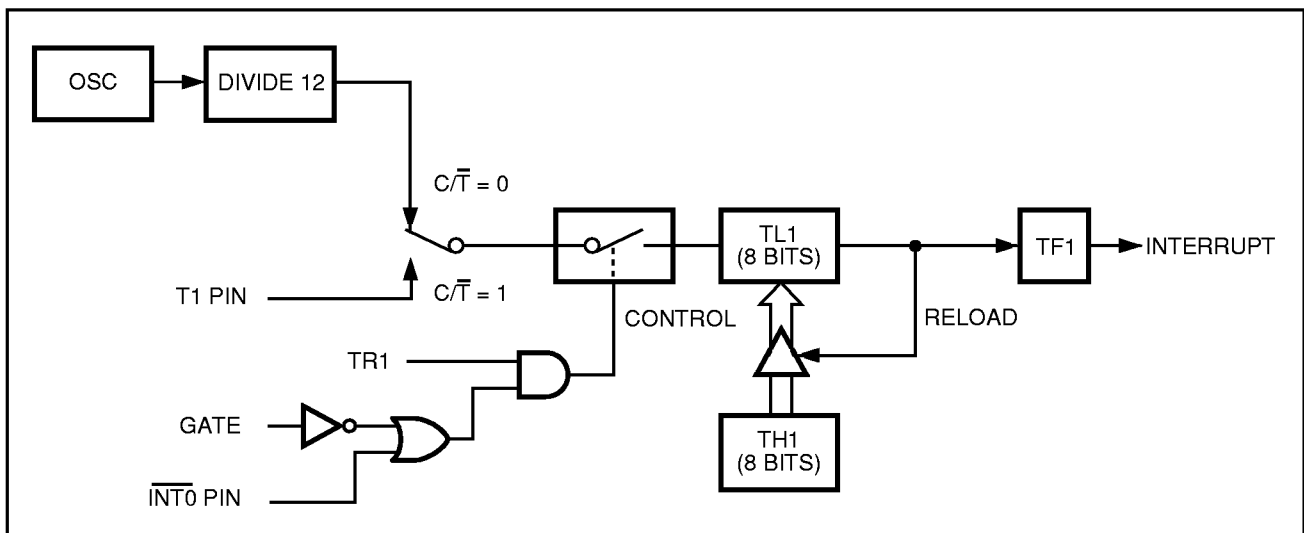**Figure 9.  Timer/Counter 1 Mode 1: 16-Bit Counter**



**Figure 10.  Timer/Counter 1 Mode 2: 8-Bit Auto-Reload**
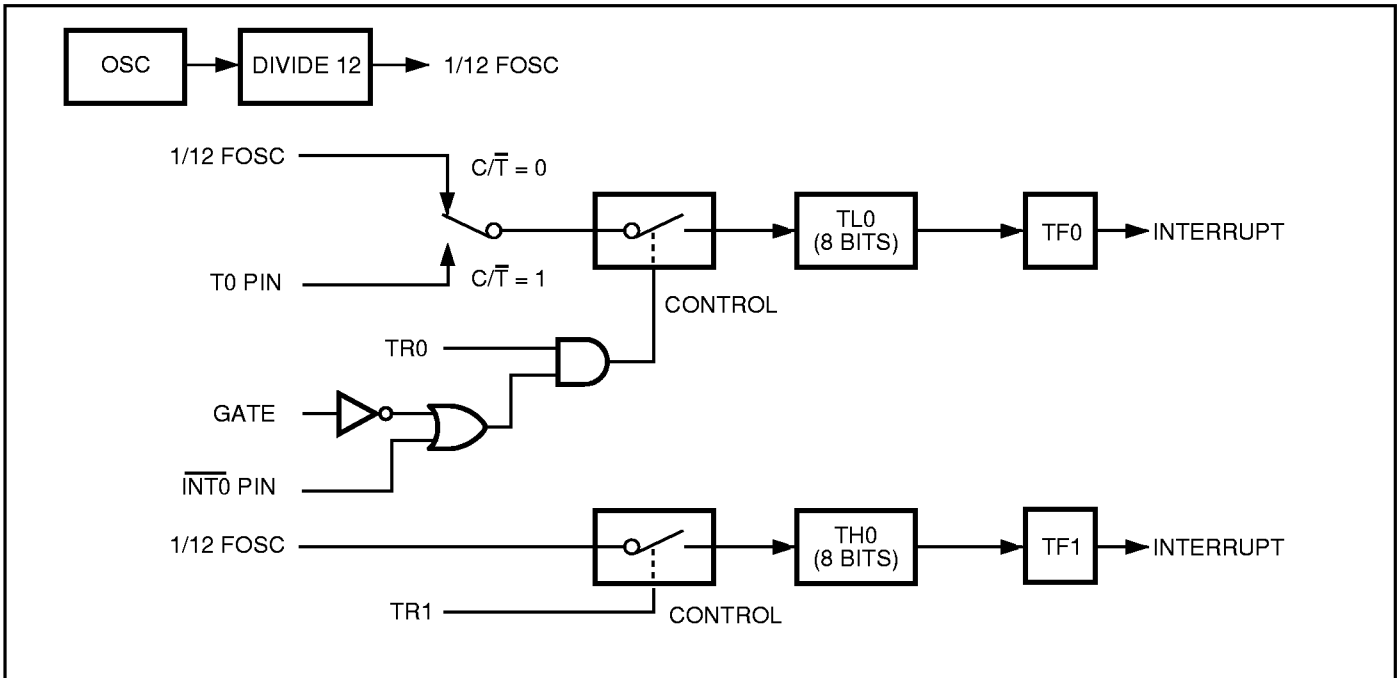
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**Figure 11. Timer/Counter 0 Mode 3: Two 8-Bit Counters**

## Timer Setup

Tables 3 through 6 give TMOD values that can be used to set up Timers in different modes.

It assumes that only one timer is used at a time. If Timers 0 and 1 must run simultaneously in any mode, the value in TMOD for Timer 0 must be ORed with the value shown for Timer 1 (Tables 5 and 6).

For example, if Timer 0 must run in Mode 1 GATE (external control), and Timer 1 must run in Mode 2 COUNTER, then the value that must be loaded into TMOD is 69H (09H from Table 3 ORed with 60H from Table 6).

Moreover, it is assumed that the user is not ready at this point to turn the timers on and will do so at another point in the program by setting bit TRx (in TCON) to 1.

### Table 3. Timer/Counter 0 Used as a Timer

| Mode | Timer 0 Function | TMOD Internal Control[1] | External Control[2] |
|------|------------------|--------------------------|---------------------|
| 0 | 13-Bit Timer | 00H | 08H |
| 1 | 16-Bit Timer | 01H | 09H |
| 2 | 8-Bit Auto-Reload | 02H | 0AH |
| 3 | Two 8-Bit Timers | 03H | 0BH |

### Table 4. Timer/Counter 0 Used as a Counter

| Mode | Timer 0 Function | TMOD Internal Control[1] | External Control[2] |
|------|------------------|--------------------------|---------------------|
| 0 | 13-Bit Timer | 04H | 0CH |
| 1 | 16-Bit Timer | 05H | 0DH |
| 2 | 8-Bit Auto-Reload | 06H | 0EH |
| 3 | One 8-Bit Counter | 07H | 0FH |

**Notes:**
1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on $\overline{\text{INT0}}$ (P3.2) when TR0 = 1 (hardware control).

### Table 5. Timer/Counter 1 Used as a Timer

| Mode | Timer 1 Function | TMOD Internal Control[1] | External Control[2] |
|------|------------------|--------------------------|---------------------|
| 0 | 13-Bit Timer | 00H | 80H |
| 1 | 16-Bit Timer | 10H | 90H |
| 2 | 8-Bit Auto-Reload | 20H | A0H |
| 3 | Does Not Run | 30H | B0H |

### Table 6. Timer/Counter 1 Used as a Counter

| Mode | Timer 1 Function | TMOD Internal Control[1] | External Control[2] |
|------|------------------|--------------------------|---------------------|
| 0 | 13-Bit Timer | 40H | C0H |
| 1 | 16-Bit Timer | 50H | D0H |
| 2 | 8-Bit Auto-Reload | 60H | E0H |
| 3 | Not Available | — | — |

**Notes:**
1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1-to-0 transition on $\overline{\text{INT1}}$ (P3.3) when TR1 = 1 (hardware control).

## SERIAL INTERFACE

The Serial port is full duplex, which means it can transmit and receive simultaneously. It is also receive-buffered, which means it can begin receiving a second byte before a previously received byte has been read from the receive register. (However, if the first byte still has not been read when reception of the second byte is complete, one of the bytes will be lost.) The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can operate in the following four modes:

**Mode 0:**
Serial data enters and exits through RXD. TXD outputs the shift clock. Eight data bits are transmitted/received, with the LSB first. The baud rate is fixed at 1/12 the oscillator frequency (see Figure 12).

**Mode 1:**
Ten bits are transmitted (through TXD) or received (through RXD): a start bit (0), eight data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable (see Figure 13).

**Mode 2:**
Eleven bits are transmitted (through TXD) or received (through RXD): a start bit (0), eight data bits (LSB first), a programmable ninth data bit, and a stop bit (1). On transmit, the ninth data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) can be moved into TB8. On receive, the ninth data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency (see Figure 14).

**Mode 3:**
Eleven bits are transmitted (through TXD) or received (through RXD): a start bit (0), eight data bits (LSB first), a programmable ninth data bit, and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except the baud rate, which is variable in Mode 3 (see Figure 15).

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

## Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, nine data bits are received, followed by a stop bit. The ninth bit goes into RB8; then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt is activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON.

The following example shows how to use the serial interrupt for multiprocessor communications. When the master processor must transmit a block of data to one of several slaves, it first sends out an address byte that identifies the target slave. An address byte differs from a data byte in that the ninth bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave is interrupted by a data byte. An address byte, however, interrupts all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave clears its SM2 bit and prepares to receive the data bytes that follows. The slaves that are not addressed set their SM2 bits and ignore the data bytes.

SM2 has no effect in Mode 0 but can be used to check the validity of the stop bit in Mode 1. In a Mode 1 reception, if SM2 = 1, the receive interrupt is not activated unless a valid stop bit is received.

## Baud Rates

The baud rate in Mode 0 is fixed as shown in the following equation.

$$\text{Mode 0 Baud Rate} = \frac{\text{Oscillator Frequency}}{12}$$

The baud rate in Mode 2 depends on the value of the SMOD bit in Special Function Register PCON. If SMOD = 0 (the value on reset), the baud rate is 1/64 of the oscillator frequency. If SMOD = 1, the baud rate is 1/32 of the oscillator frequency, as shown in the following equation.

$$\text{Mode 2 Baud Rate} = \frac{2^{SMOD}}{64} \times (\text{Oscillator Frequency})$$

In the IS89LV51, the Timer 1 overflow rate determines the baud rates in Modes 1 and 3.

## Using the Timer 1 to Generate Baud Rates

When Timer 1 is the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD according to the following equation.

$$\frac{\text{Mode 1, 3}}{\text{Baud Rate}} = \frac{2^{SMOD}}{32} \times (\text{Timer 1 Overflow Rate})$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either timer or counter operation in any of its three running modes. In the most typical applications, it is configured for timer operation in auto-reload mode (high nibble of TMOD = 0010B). In this case, the baud rate is given by the following formula.

$$\frac{\text{Mode 1,3}}{\text{Baud Rate}} = \frac{2^{SMOD}}{32} \times \frac{\text{Oscillator Frequency}}{12x\,[256 - (TH1)]}$$

Programmers can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload.

Table 7 lists commonly used baud rates and how they can be obtained from Timer 1.

## Table 7. Commonly Used Baud Rates Generated by Timer 1

| | | | Timer 1 | | |
|---|---|---|---|---|---|
| Baud Rate | fosc | SMOD | C/$\overline{T}$ | Mode | Reload Value |
| Mode 0 Max: 1 MHz | 12 MHz | X | X | X | X |
| Mode 2 Max: 375K | 12 MHz | 1 | X | X | X |
| Modes 1, 3: 62.5K | 12 MHz | 1 | 0 | 2 | FFH |
| 19.2K | 11.059 MHz | 1 | 0 | 2 | FDH |
| 9.6K | 11.059 MHz | 0 | 0 | 2 | FDH |
| 4.8K | 11.059 MHz | 0 | 0 | 2 | FAH |
| 2.4K | 11.059 MHz | 0 | 0 | 2 | F4H |
| 1.2K | 11.059 MHz | 0 | 0 | 2 | E8H |
| 137.5 | 11.986 MHz | 0 | 0 | 2 | 1DH |
| 110 | 6 MHz | 0 | 0 | 2 | 72H |
| 110 | 12 MHz | 0 | 0 | 1 | FEEBH |

**More About Mode 0**

Serial data enters and exits through RXD. TXD outputs the shift clock. Eight data bits are transmitted/received, with the LSB first. The baud rate is fixed at 1/12 the oscillator frequency.

Figure 12 shows a simplified functional diagram of the serial port in Mode 0 and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal at S6P2 also loads a 1 into the ninth position of the transmit shift register and tells the TX Control block to begin a transmission. The internal timing is such that one full machine cycle will elapse between "write to SBUF" and activation of SEND.

SEND transfer the output of the shift register to the alternate output function line of P3.0, and also transfers SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1, and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift register are shifted one position to the right.

As data bits shift out to the right, 0s come in from the left. When the MSB of the data byte is at the output position of the shift register, the 1 that was initially loaded into the ninth position is just to the left of the MSB, and all positions to the left of that contain 0s. This condition flags the TX Control block to do one last shift, then deactivate SEND and set TI. Both of these actions occur at S1P1 of the tenth machine cycle after "write to SBUF."

Reception is initiated by the condition REN = 1 and RI = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 to the receive shift register and activates RECEIVE in the next clock phase.

RECEIVE enables SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are shifted on position to the left. The value that comes in from the right is the value that was sampled at the P3.0 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the right-most position arrives at the left-most position in the shift register, it flags the RX Control block to do one last shift and load SBUF. At S1P1 of the tenth machine cycle after the write to SCON that cleared RI, RECEIVE is cleared and RI is set.

**More About Mode 1**

Ten bits are transmitted (through TXD), or received (through RXD): a start bit (0), eight data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the IS89LV51 the baud rate is determined by the Timer 1 overflow rate.

Figure 13 shows a simplified functional diagram of the serial port in Mode 1 and associated timings for transmit and receive.

Transmission is initiated by any instruction that uses SBUF as a destination register.

The "write to SBUF" signal also loads a 1 into the ninth bit position of the transmit shift register and flags the TX control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. Thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.

The transmission begins when SEND is activated, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, 0s are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, the 1 that was initially loaded into the ninth position is just to the left of the MSB, and all positions to the left of that contain 0s. This condition flags the TX Control unit to do one last shift, then deactivate SEND and set TI. This occurs at the tenth divide-by-16 rollover after "write to SBUF".

Reception is initiated by a 1-to-0 transition detected at RXD. For this purpose, RXD is sampled at a rate of 16 times the established baud rate. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16th. At the seventh, eighth, and ninth counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least two of the three samples. This is done to reject noise. In order to reject false bits, if the value accepted during the first bit time is not 0, the receive circuits are reset and the unit continues looking for another 1-to-0 transition. If the start bit is valid, it is shifted into the input shift register, and reception of the rest of the frame proceeds.

As data bits come in from the right, 1s shift to the left. When the start bit arrives at the leftmost position in the shift register, (which is a 9-bit register in Mode 1), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8 and to set RI is generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

1) RI = 0 and

2) Either SM2 = 0, or the received stop bit =1

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the eight data bits go into SBUF, and RI is activated. At this time, whether or not the above conditions are met, the unit continues looking for a 1-to-0 transition in RXD.

### More About Modes 2 and 3

Eleven bits are transmitted (through TXD), or received (through RXD): a start bit (0), eight data bits (LSB first), a programmable ninth data bit, and a stop bit (1). On transmit, the ninth data bit (TB8) can be assigned the value of 0 or 1. On receive, the ninth data bit goes into RB8 in SCON. The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1.

Figures 14 and 15 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the ninth bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads TB8 into the ninth bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. Thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.

The transmission begins when SEND is activated, which puts the start bit at TXD. One bit timer later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the ninth bit position of the shift register. Thereafter, only 0s are clocked in. Thus, as data bits shift out to the right, 0s are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain 0s. This condition flags the TX Control unit to do one last shift, then deactivate SEND and set TI. This occurs at the eleventh divide-by-16 rollover after "write to SBUF".

Reception is initiated by a 1-to-0 transition detected at RXD. For this purpose, RXD is sampled at a rate of 16 times the established baud rate. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

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At the seventh, eighth, and ninth counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least two of the three samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit continues looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame proceeds.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8 and to set RI is generated if, and only if, the following conditions are met at the time the final shift pulse is generated:

1) RI = 0, and

2) Either SM2 = 0 or the received ninth data bit = 1

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received ninth data bit goes into RB8, and the first eight data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit continues looking for a 1-to-0 transition at the RXD input.

Note that the value of the received stop bit is irrelevant to SBUF, RB8, or RI.

**Table 8. Serial Port Setup**

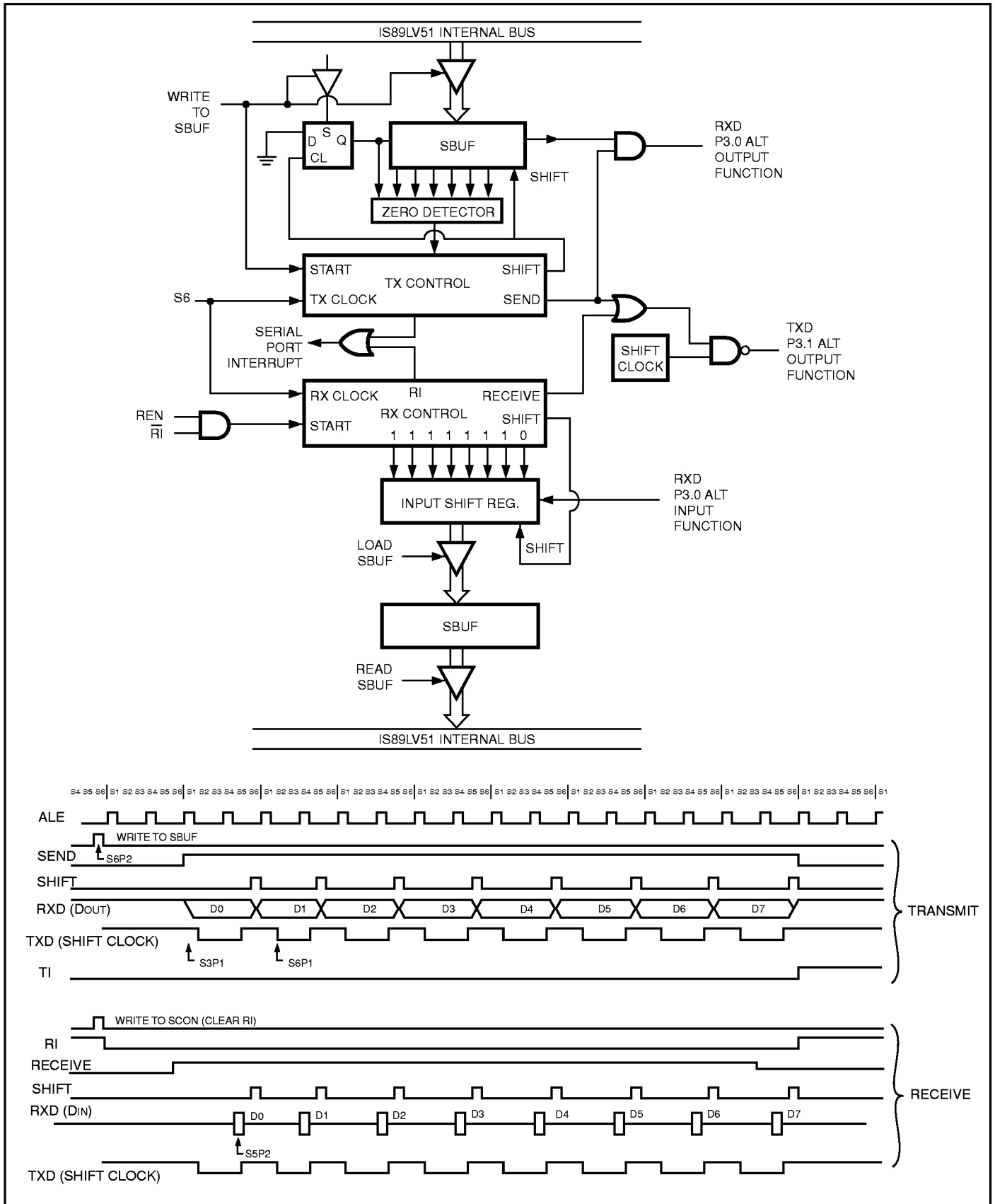| Mode | SCON | SM2 Variation |
|------|------|---------------|
| 0 | 10H | Single Processor Environment (SM2 = 0) |
| 1 | 50H | |
| 2 | 90H | |
| 3 | D0H | |
| 0 | NA | Multiprocessor Environment (SM2 = 1) |
| 1 | 70H | |
| 2 | B0H | |
| 3 | F0H | |

**Figure 12. Serial Port Mode 0**