IMS1630L CMOS High Performance 8K x 8 Static RAM

inmos®

FEATURES

- INMOS' high performance CMOS
- Advanced Process - 1.6 Micron Design Rules
- 8K x 8 Bit Organization
- 45, 55, 70, 100 and 120 ns Address Access Times
- 45, 55, 70, 100 and 120 ns Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- Standard 28 Pin 600-mil DIP, 28-Lead SOIC and Skinny DIP Package
- Battery Backup Operation - 2V Data Retention

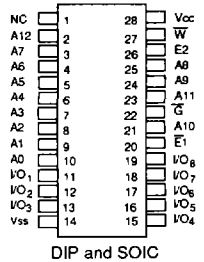
DESCRIPTION

The INMOS IMS1630L is a high performance 8Kx8 CMOS Static RAM.

The IMS1630L features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. The IMS1630L provides two Chip Enable functions ($\overline{E1}$, E2) to place the device into a reduced power standby mode.

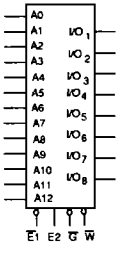
In the low power battery backup data retention mode, the IMS1630L consumes typically 10µA at 2 volts supply.

PIN CONFIGURATION

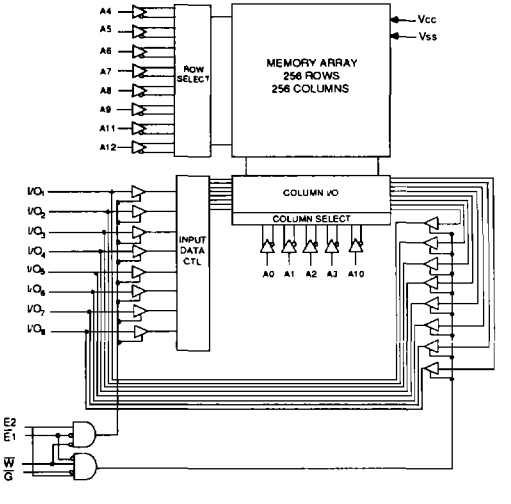


DIP and SOIC

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{12}	ADDRESS INPUTS	Vcc	POWER (+5V)
$\overline{W}$	WRITE ENABLE	Vcc	GROUND
I/O1-I/O8	DATA IN/OUT		
$\overline{E1}$, E2	CHIP ENABLE		
$\overline{G}$	OUTPUT ENABLE		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect reliability

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	400 linear ft/min air flow

*V_{IL} min = -3.0 volts for pulse width <20ns, note b

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		90	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		20	mA	$\bar{E}1 \ge V_{IH}$ or $E2 \le V_{IL}$. All other inputs at $V_{IN} \le V_{IL}$ or $\ge V_{IH}$
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		8	mA	$\bar{E}1 \ge$ (Vcc - 0.2V) or $E2 \le 0.2V$. All other inputs at $V_{IN} \le 0.2$ or $\ge$ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	$\bar{E}1 \ge$ (Vcc - 0.2V) or $E2 \le 0.2V$. Inputs cycling at $V_{IN} \le 0.2$ or $\ge$ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±5	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the outputs unloaded.

AC TEST CONDITIONS

Input Pulse Levels ..... Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load ..... See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0 MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b This parameter is sampled and not 100% tested

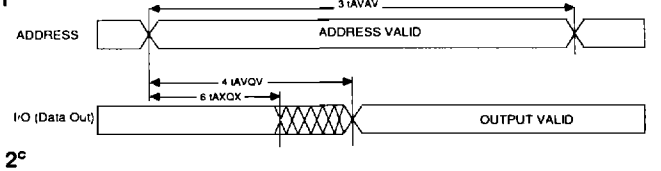
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

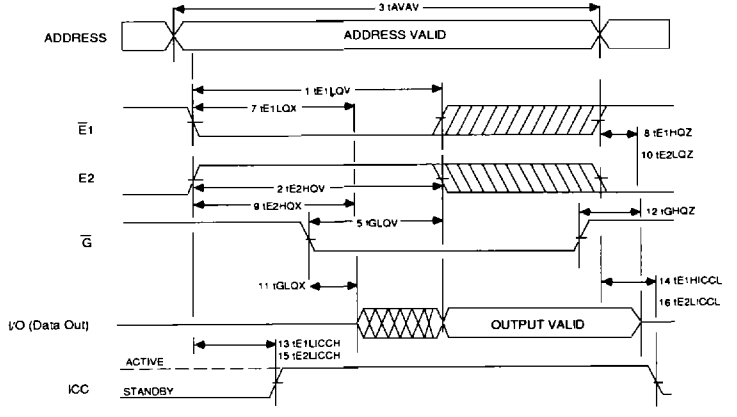
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630L-45 MIN	IMS 1630L-45 MAX	IMS 1630L-55 MIN	IMS 1630L-55 MAX	IMS 1630L-70 MIN	IMS 1630L-70 MAX	IMS 1630L-100 MIN	IMS 1630L-100 MAX	IMS 1630L-120 MIN	IMS 1630L-120 MAX	UNITS	NOTES
1	tE1LQV	tACS	Chip Enable Access Time		45		55		70		100		120	ns	
2	tE2HQV	tACS	Chip Enable Access Time		45		55		70		100		120	ns	
3	tAVAV	tRC	Read Cycle Time	45		55		70		100		120		ns	c
4	tAVQV	tAA	Address Access Time		45		55		70		100		120	ns	d
5	tGLQV	tOE	O/P Enable to Data Valid		20		20		35		40		50	ns	
6	tAXQX	tOH	O/P Hold After Addr's Ch'ge	5		5		10		10		10		ns	
7	tE1LQZ	tLZ	Chip Enable to O/P Active	5		5		10		10		10		ns	
8	tE1HQZ	tHZ	Chip Disable to O/P Inactive	0	20	0	25	0	25	0	35	0	40	ns	f, j
9	tE2HQZ	tLZ	Chip Enable to O/P Active	5		5		10		10		10		ns	
10	tE2LQZ	tHZ	Chip Disable to O/P Inactive	0	20	0	25	0	25	0	35	0	40	ns	f, j
11	tGLQX	tLZ	O/P Enable to O/P Active	5		5		5		5		5		ns	
12	tGHQZ	tHZ	O/P Disable to O/P Inactive	0	20	0	25	0	25	0	35	0	40	ns	f, j
13	tE1HICCH	tPU	Chip Enable to Power Up	0		0		0		0		0		ns	j
14	tE1LICCL	tPD	Chip Enable to Power Down		20		20		20		25		30	ns	j
15	tE2HICCH	tPU	Chip Enable to Power Up	0		0		0		0		0		ns	j
16	tE2LICCL	tPD	Chip Disable to Power Down		20		20		20		25		30	ns	j
17		tT	I/P Rise and Fall Times		50		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}1$ low, $\overline{G}$ low and E2 high.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}1$, E2, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

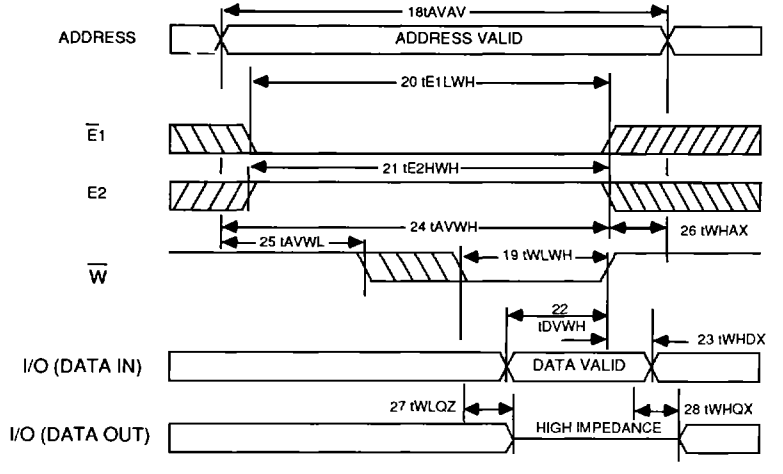
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630L-45 MIN	IMS 1630L-45 MAX	IMS 1630L-55 MIN	IMS 1630L-55 MAX	IMS 1630L-70 MIN	IMS 1630L-70 MAX	IMS 1630L-100 MIN	IMS 1630L-100 MAX	IMS 1630L-120 MIN	IMS 1630L-120 MAX	UNITS	NOTES
18	tAVAV	tWC	Write Cycle Time	45		55		70		100		120		ns	
19	tWLWH	tWP	Write Pulse Width	35		40		40		60		70		ns	
20	tE1LWH	tCW	Chip Enable 1 to End of Write	35		40		40		60		70		ns	
21	tE2HWH	tCW	Chip Enable 2 to End of Write	35		40		40		60		70		ns	
22	tDVWH	tDW	Data Setup to End of Write	20		20		20		40		40		ns	
23	tWHDX	tDH	Data Hold after End of Write	0		0		0		0		0		ns	
24	tAVWH	tAW	Address Setup to End of Write	35		40		40		80		85		ns	
25	tAVWL	tAS	Address Setup to Start of Write	0		0		0		0		0		ns	
26	tWHAX	tWR	Address Hold after End of Write	0		0		0		0		0		ns	
27	tWLQZ	tWZ	Write Enable to Output Disable	0	20	0	20	0	20	0	35	0	40	ns	f,j
28	tWHQX	tOW	Output Active After End of Write	5		5		5		5		5		ns	i,j

WRITE CYCLE 2: $\overline{E}1$ OR E2 CONTROLLED[g,h]

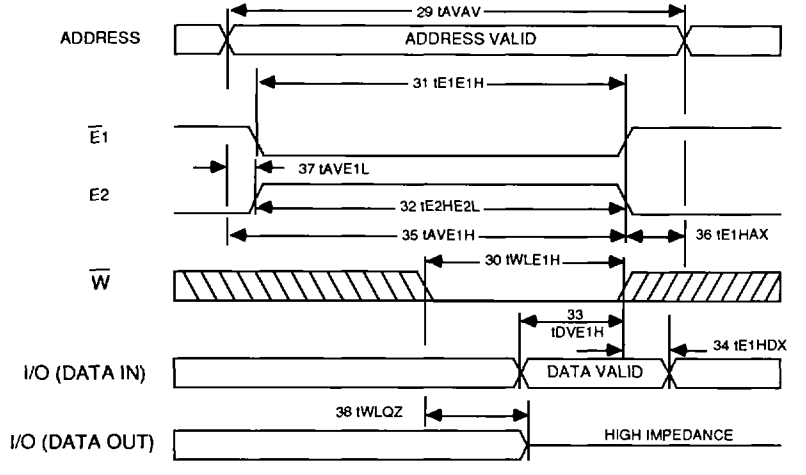
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630L-45 MIN	IMS 1630L-45 MAX	IMS 1630L-55 MIN	IMS 1630L-55 MAX	IMS 1630L-70 MIN	IMS 1630L-70 MAX	IMS 1630L-100 MIN	IMS 1630L-100 MAX	IMS 1630L-120 MIN	IMS 1630L-120 MAX	UNITS	NOTES
29	tAVAV	tWC	Write Cycle Time	45		55		70		100		120		ns	
30	tWLE1H	tWP	Write Pulse Width	35		40		40		60		70		ns	
31	tE1LE1H	tCW	Chip Enable 1 to End of Write	35		40		40		60		70		ns	
32	tE2HE2L	tCW	Chip Enable 2 to End of Write	35		40		40		60		70		ns	
33	tDVE1H	tDW	Data Setup to End of Write	20		20		20		40		40		ns	
34	tE1HDX	tDH	Data Hold after End of Write	0		0		0		0		0		ns	
35	tAVE1H	tAW	Address Setup to End of Write	35		40		40		80		85		ns	
36	tE1HAX	tWR	Address Hold after End of Write	0		0		0		0		0		ns	
37	tAVE1L	tAS	Address Setup to Start of Write	0		0		0		0		0		ns	
38	tWLQZ	tWZ	Write Enable to Output Disable	0	20	0	20	0	20	0	30	0	35	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}1$, E2, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}1$, or $\overline{W}$ must be $\geq V_{IH}$ or E2 must be $\leq V_{IL}$ during address transitions.
Note i: If $\overline{W}$ is low when the later of $\overline{E}1$ goes low or E2 goes high, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



WRITE CYCLE 2



DEVICE OPERATION

The IMS1630L has four control inputs, Chip Enable1 ($\overline{E1}$), Chip Enable 2 (E2), Write Enable ($\overline{W}$) and Output Enable ($\overline{G}$). There are also13 address inputs (A0 -A12) and eight Data I/O lines (I/O 1 to I/O 8). The Enable inputs control device selection as well as active and standby modes. The $\overline{W}$ input controls the mode of operation (Read or Write). The $\overline{G}$ input controls only the state of the eight output drivers.

With both $\overline{E1}$ low and E2 high, the device is selected and the 13 address inputs are decoded to select one 8-bit word out of 8K words. Read and Write operations on the memory cells are controlled by the $\overline{W}$ input. With either $\overline{E1}$ high or E2 low, the device is deselected, the outputs disabled and the power consumption is reduced to less than one-fourth of the active mode power. $\overline{G}$ serves only to control the operation of the output drivers. When $\overline{G}$ is high, the output drivers are in a high impedance state, independant of the $\overline{E1}$, E2 and $\overline{W}$ inputs.

READ CYCLE

A read cycle is defined as $W \geq V_{IH}$ min with $\overline{E1} \leq V_{IL}$ max, $E2 \geq V_{IH}$ min and $\overline{G} \leq V_{IL}$ max. Read access time is measured from the later of either $\overline{E1}$ going low, E2 going high, valid address, or $\overline{G}$ going low.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E1}$ is low and E2 is high (with $\overline{G}$ low). The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of tAXQX. As long as $\overline{E1}$ remains low and E2 is high, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by the later of $\overline{E1}$ going low, E2 going high or $\overline{G}$ going low. As long as address is stable when the later of $\overline{E1}$ goes low or E2 goes high, valid data is at the output at the later of tE1LQV, tE2HQV or tGLQV. If address is not valid when the later of $\overline{E1}$ goes low or E2 goes high, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

The $\overline{G}$ signal controls the output buffer. $\overline{G}$ is required to be low (along with $\overline{E1}$ low and E2 high) in order for I/O1 - I/O 8 to be active.

WRITE CYCLE

The write cycle of the IMS1630L is initiated by the later of $\overline{E1}$ or $\overline{W}$ to transition from a high to a low or E2 transitioning from low to high. The $\overline{G}$ control will remove bus contention if held high throughout the duration of the write cycle. If $\overline{G}$ is low during a $\overline{W}$ controlled write cycle (Write Cycle 1), the output buffer will be turned on by the later of tE1LQX after the falling edge of $\overline{E1}$ or tE2HQX after the rising edge of E2. The output buffer is then turned off within tWLQZ of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common input/output connections. Therefore the recommended mode of operation is to keep $\overline{G}$ high during the write cycle. During a write cycle, data on the inputs is written into the selected cells and the outputs are floating.

For any write cycle, tAVWL, tAVE1L, or tAVE2H must be met, depending on whether $\overline{E1}$, E2 or $\overline{W}$ is the last to transition. After either $\overline{W}$ or $\overline{E1}$ goes high or E2 goes low to terminate the write cycle, addresses may change. If address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways. The fidelity of the $\overline{W}$ control signal is very important Excessive ringing on high to low transitions may cause signals to rise above V_{IL} max, violating the minimum $\overline{W}$ pulse width specification - tWLWH.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high while $\overline{E1}$ is low and E2 is high, the outputs remain in a high impedance state (unless $\overline{G}$ is low). If $\overline{G}$ is low when $\overline{W}$ goes high at the end of a write cycle the data read from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform shows a write cycle terminated by the later $\overline{E1}$ going high or E2 going low. Data set-up and hold times are referenced to the later of the rising edge of $\overline{E1}$ or the falling edge of E2. With either $\overline{E1}$ high or E2 low the outputs remain in the high impedance state

When using WRITE CYCLE 1 proper management of the $\overline{G}$ control signal will avoid bus contention. If $\overline{G}$ is low when $\overline{W}$ goes high (with $\overline{E1}$ low and E2 high) the output buffers will be active tWHQX after the rising edge of $\overline{W}$ Data out will be the same as the data just written, unless the address changes. If input data from the previous cycle is still valid after the address changes, contention may result. Contention may also result if the device is selected ($\overline{E1}$ low, E2 high, $\overline{G}$ low) before $\overline{W}$ goes low and input data is valid early in the cycle. The recommended mode of operation is to keep $\overline{G}$ high except when reading data from the device, thus avoiding bus contention.

TTL VS. CMOS INPUTLEVELS

The INMOS 1630L is fully compatible with TTL input levels. The input circuitry of the IMS1630L is designed for maximum speed and also for conversion of TTL level signals to the CMOS levels required for internal operation. The IMS1630L consumes less power when CMOS levels are used instead of TTL levels. The lower CMOS Icc specifications (Icc3 and Icc4) may be achieved by using CMOS levels. The power consumption will be lower at typical TTL levels than at the worst case levels.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1630L. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 µF and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area. This will provide a solid ground reference for the drivers and prevent loss of operating margin due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically. A resistor of predetermined value may not properly terminate the transmission line.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing. It is wise to verify signal fidelity by observation utilising a wideband oscilloscope and probe.

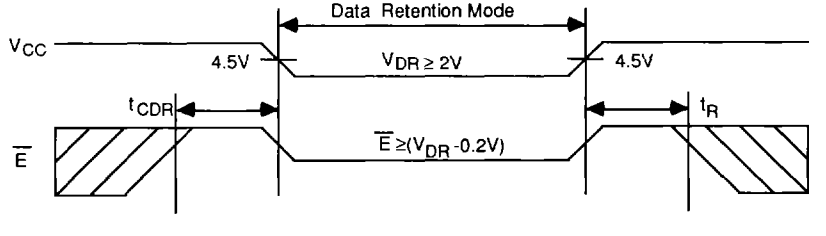
DATA RETENTION (L version only) ($0°C \le T_A \le 70°C$)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \le 0.2V$ or $\ge (Vcc - 0.2V)$ $\overline{E} \ge (Vcc - 0.2V)$
I_{CCDR1}	Data Retention Current		10	100	µA	$V_{CC} = 3.0$ volts
I_{CCDR2}	Data Retention Current		5	70	µA	$V_{CC} = 2.0$ volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j,k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j,k (t_{RC} = Read Cycle Time)

* Typical data retention parameters at 25 °C

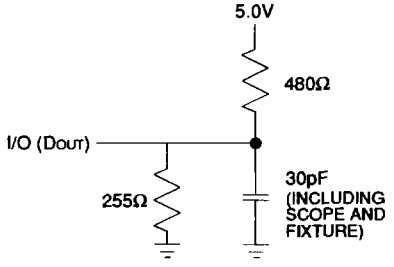
Note j: Parameter guaranteed but not tested

Note k: Supply recovery rate should not exceed 100mV per10µs from V_{DR} to V_{CC} min



Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD



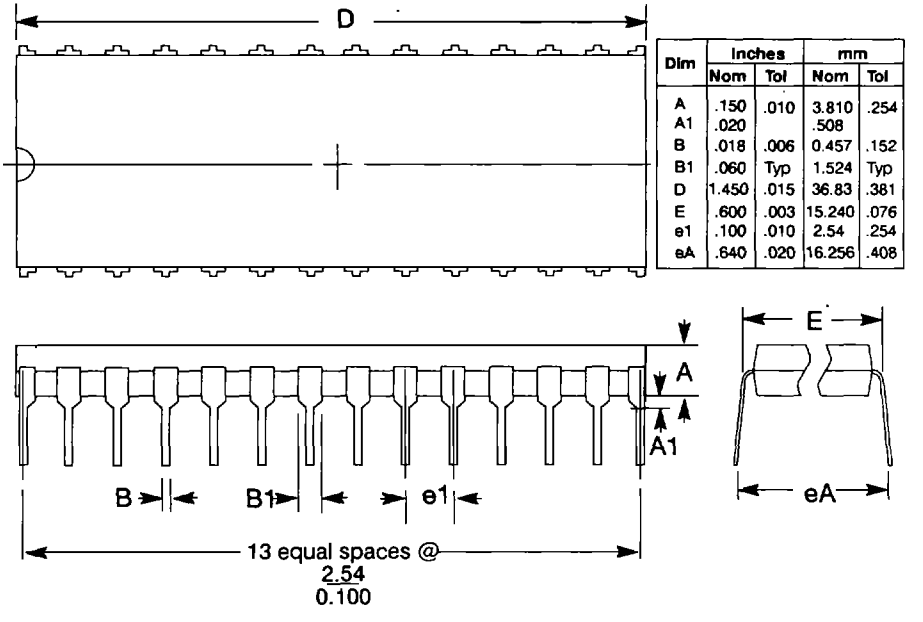
$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	I/O	MODE
H	X	X	X	HI-Z	Standby (Isb)
X	L	X	X	HI-Z	Standby (Isb)
L	H	H	H	HI-Z	Output disable
L	H	H	L	DOUT	Read
L	H	L	X	DIN	Write

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1630	45ns	PDIP	IMS1630LP45
	45ns	SOIC	IMS1630LH45
	45ns	Skinny DIP	IMS1630LP45Z
	55ns	PDIP	IMS1630LP55
	55ns	SOIC	IMS1630LH55
	55ns	Skinny DIP	IMS1630LP55Z
	70ns	PDIP	IMS1630LP70
	70ns	SOIC	IMS1630LH70
	70ns	Skinny DIP	IMS1630LP70Z
	100ns	PDIP	IMS1630LP10
	100ns	SOIC	IMS1630LH10
	100ns	Skinny DIP	IMS1630LP10Z
	120ns	PDIP	IMS1630LP12
	120ns	SOIC	IMS1630LH12
	120ns	Skinny DIP	IMS1630LP12Z

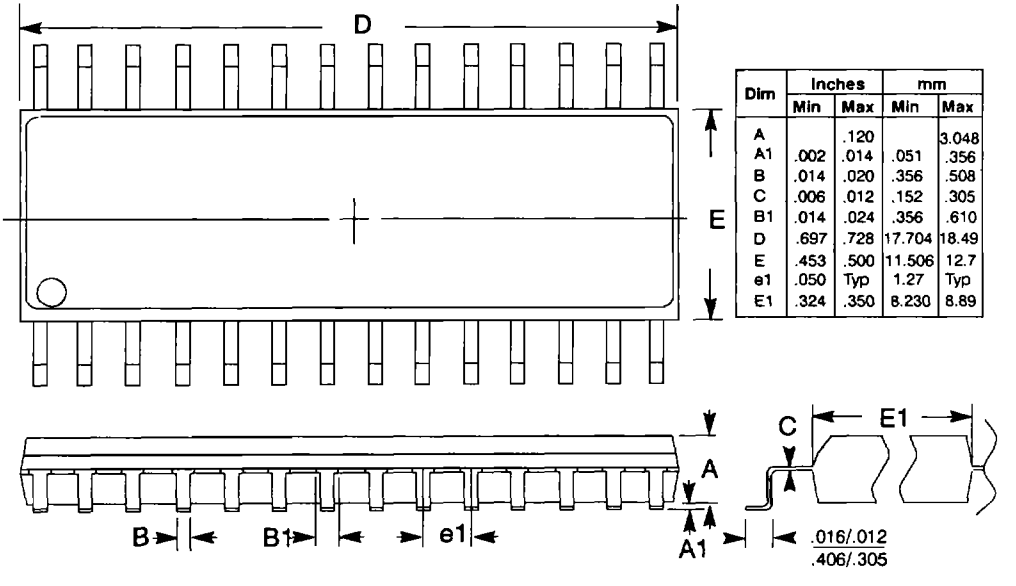
PACKAGING INFORMATION

28 Pin Plastic Dual-In-Line



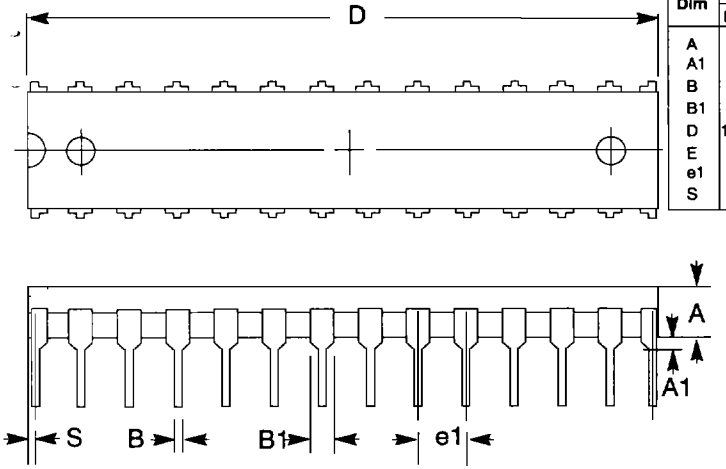
Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.150	.010	3.810	.254
A1	.020		.508	
B	.018	.006	0.457	.152
B1	.060	Typ	1.524	Typ
D	1.450	.015	36.83	.381
E	.600	.003	15.240	.076
e1	.100	.010	2.54	.254
eA	.640	.020	16.256	.408

28 Pin SOIC



Dim	Inches		mm	
	Min	Max	Min	Max
A		.120		3.048
A1	.002	.014	.051	.356
B	.014	.020	.356	.508
C	.006	.012	.152	.305
B1	.014	.024	.356	.610
D	.697	.728	17.704	18.49
E	.453	.500	11.506	12.7
e1	.050	Typ	1.27	Typ
E1	.324	.350	8.230	8.89

28 Pin Skinny DIP



Dim	Inches		mm	
	Min	Max	Min	Max
A	.130		3.302	
A1	.040		1.016	
B	.016	.020	0.406	.457
B1	.045	.055	1.143	1.397
D	1.345	1.355	34.163	3.442
E	.300	.325	7.62	8.255
e1	.100	Typ	2.54	Typ
S	.020	.030	.508	.762