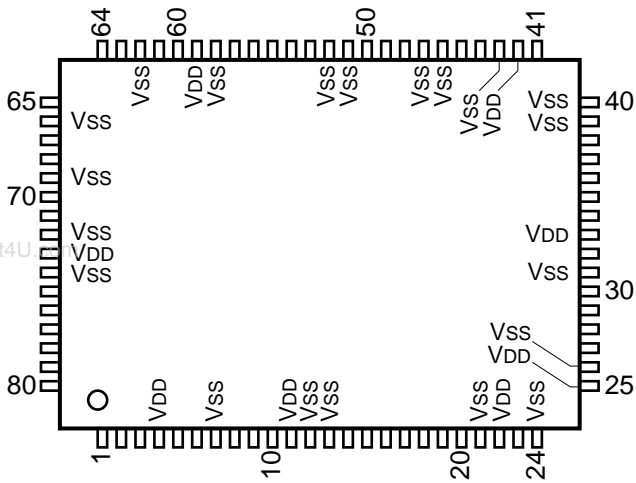


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C-MOS LASER DATA CONTROL (GATE ARRAY)

-TOP VIEW-



VDD = +5V  
VSS = GND

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	DPEAK T	21	-	Vss	41	O	WDATA N	61	I	CLKIN N
2	I	MS0 T	22	-	VDD	42	-	VDD	62	-	Vss
3	I	MS1 T	23	O	WDATA T	43	-	Vss	63	I	MS1 N
4	-	VDD	24	-	Vss	44	O	WBIAS N	64	I	MS0 N
5	I	CLKIN T	25	-	VDD	45	I	ACTS N	65	I	DPEAK N
6	I	DATAIN T	26	-	Vss	46	-	Vss	66	-	Vss
7	-	Vss	27	I	CS	47	-	Vss	67	O	PEF T
8	I	NDDI T	28	I	WR	48	O	PTRN N	68	O	PEF N
9	I	DLCI T	29	I	CD7	49	O	BIAS N	69	-	Vss
10	I	DLDI T	30	I	CD6	50	I	NDCI N	70	I	RES
11	-	VDD	31	-	Vss	51	-	Vss	71	I	OE
12	-	Vss (FIX)	32	I	CD5	52	-	Vss (FIX)	72	-	Vss
13	-	Vss	33	-	VDD (FIX)	53	O	CLK N	73	-	VDD (FIX)
14	O	DATA T	34	I	CD4	54	O	DATA N	74	-	Vss
15	O	CLK T	35	I	CD3	55	I	DLDI N	75	I	AD0
16	I	NDCI T	36	I	CD2	56	I	DLCI N	76	I	AD1
17	O	BIAS T	37	I	CD1	57	I	NDDI N	77	I	AD2
18	O	PTRN T	38	I	CD0	58	-	Vss	78	I	CKPH T
19	I	ACTS T	39	-	Vss	59	-	VDD	79	I	CKPH N
20	O	WBIAS T	40	-	Vss	60	I	DATAIN N	80	I	ACTM

**INPUT**

ACTM ; AC TEST MODE  
 ACTS N ; AC TEST SIGNAL N-CH  
 ACTS T ; AC TEST SIGNAL T-CH  
 AD0-2 ; CPU ADDRESS  
 CD0-7 ; CPU DATA  
 CKPH N ; CLOCK PHASE N-CH  
 CKPH T ; CLOCK PHASE T-CH  
 CLKIN N ; CLOCK INPUT N-CH  
 CLKIN T ; CLOCK INPUT T-CH  
 CS ; CHIP SELECT  
 DATAIN N ; DATA INPUT N-CH  
 DATAIN T ; DATA INPUT T-CH  
 DLCI N ; DELAYED CLOCK INPUT N-CH  
 DLCI T ; DELAYED CLOCK INPUT T-CH  
 DLDI N ; DELAYED DATA INPUT N-CH  
 DLDI T ; DELAYED DATA INPUT T-CH  
 DPEAK N ; DATA PEAK N-CH  
 DPEAK T ; DATA PEAK T-CH  
 MS0 N ; MODE SELECT 0 N-CH  
 MS0 T ; MODE SELECT 0 T-CH  
 MS1 N ; MODE SELECT 1 N-CH  
 MS1 T ; MODE SELECT 1 T-CH  
 NDCI N ; NO DELAYED CLOCK INPUT N-CH  
 NDCI T ; NO DELAYED CLOCK INPUT T-CH  
 NDDI N ; NO DELAYED DATA INPUT N-CH  
 NDDI T ; NO DELAYED DATA INPUT T-CH  
 OE ; OUTPUT ENABLE  
 RES ; RESET  
 WR ; WRITE ENABLE

**OUTPUT**

BIAS N ; BIAS OUTPUT N-CH  
 BIAS T ; BIAS OUTPUT T-CH  
 CLK N ; CLOCK OUTPUT N-CH  
 CLK T ; CLOCK OUTPUT T-CH  
 DATA N ; DATA OUTPUT N-CH  
 DATA T ; DATA OUTPUT T-CH  
 PEF N ; PULSE EXISTING FLAG N-CH  
 PEF T ; PULSE EXISTING FLAG T-CH  
 PTRN N ; PULSE TRAIN OUTPUT N-CH  
 PTRN T ; PULSE TRAIN OUTPUT T-CH  
 WBIAS N ; WRITE BIAS OUTPUT N-CH  
 WBIAS T ; WRITE BIAS OUTPUT T-CH  
 WDATA N ; WRITE DATA OUTPUT N-CH  
 WDATA T ; WRITE DATA OUTPUT T-CH