ANALOG DEVICES

Precision, Low Power BiFET Op Amp

AD548

FEATURES

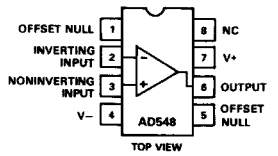
Enhanced Replacement for LF441 and TL061
DC Performance:
- **200μA max Quiescent Current**
- **10pA max Bias Current, Warmed Up (AD548C)**
- **250μV max Offset Voltage (AD548C)**
- **2μV/°C max Drift (AD548C)**
- **2μV p-p Noise, 0.1 to 10Hz**

AC Performance:
- **1.8V/μs Slew Rate**
- **1MHz Unity Gain Bandwidth**

Available in Plastic, Hermetic Cerdip and Hermetic Metal Can Packages and in Chip Form
Available in Tape and Reel in Accordance with EIA-481A Standard
MIL-STD-883B Parts Available
Dual Version Available: AD648
Surface Mount (SOIC) Package Available

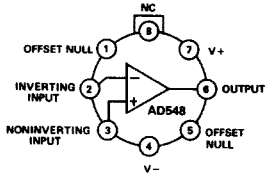
CONNECTION DIAGRAMS

Plastic Mini-DIP (N) Package,
Cerdip (Q) Package
and
SOIC (R) Package

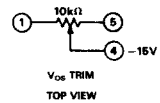


TOP VIEW

TO-99
(H) Package



NOTE: PIN 4 CONNECTED TO CASE



TOP VIEW

PRODUCT DESCRIPTION

The AD548 is a low power, precision monolithic operational amplifier. It offers both low bias current (10pA max, warmed up) and low quiescent current (200μA max) and is fabricated with ion-implanted FET and laser wafer trimming technologies. Input bias current is guaranteed over the AD548's entire common-mode voltage range.

The economical J grade has a maximum guaranteed input offset voltage of less than 2mV and an input offset voltage drift of less than 20μV/°C. The C grade reduces input offset voltage to less than 0.25mV and offset voltage drift to less than 2μV/°C. This level of dc precision is achieved utilizing Analog's laser wafer drift trimming process. The combination of low quiescent current and low offset voltage drift minimizes changes in input offset voltage due to self-heating effects. Five additional grades are offered over the commercial, industrial and military temperature ranges.

The AD548 is recommended for any dual supply op amp application requiring low power and excellent dc and ac performance. In applications such as battery-powered, precision instrument front ends and CMOS DAC buffers, the AD548's excellent combination of low input offset voltage and drift, low bias current and low 1/f noise reduces output errors. High common-mode rejection (86dB, min on the "C" grade) and high open-loop gain ensures better than 12-bit linearity in high impedance, buffer applications.

The AD548 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD548J and AD548K are rated over the commercial temperature range of 0 to +70°C. The AD548A, AD548B and AD548C are rated over the industrial temperature range of −40°C to +85°C. The AD548S and AD548T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available for parts specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD548 is available in an 8-pin plastic mini-DIP, cerdip, TO-99 metal can, surface mount (SOIC), or in chip form.

PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD548 the ideal op amp for high-performance, low-power applications.
2. The AD548 is pin compatible with industry standard op amps such as the LF441, TL061, and AD542, enabling designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low input offset voltage (2mV max) and drift (20μV/°C max) for the AD548J are achieved utilizing Analog Devices' laser drift trimming technology, eliminating the need for external trimming.
4. Analog Devices specifies each device in the warmed-up condition, insuring that the device will meet its published specifications in actual use.
5. A dual version, the AD648 is also available.
6. Enhanced replacement for LF441 and TL061.

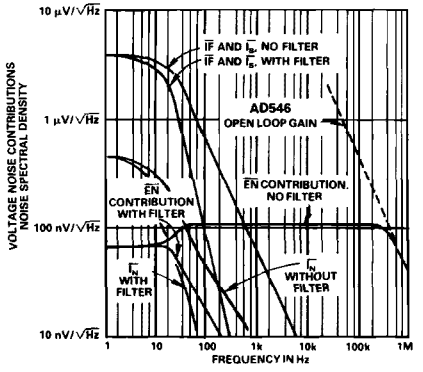


Figure 42. Photodiode Preamp Noise Sources' Spectral Density vs. Frequency

The photodiode preamp in Figure 39 can detect a signal current of 26 fA rms at a bandwidth of 16 Hz, which assuming a photodiode responsivity of 0.5 A/W, translates to a 52 fW rms minimum detectable power. The photodiode used has a high source resistance and low junction capacitance. C_F sets the signal bandwidth with R_F and also limits the "peak" in the noise gain that multiplies the op amp's input voltage noise contribution. A single pole filter at the amplifier's output limits the op amp's output voltage noise bandwidth to 26 Hz, a frequency comparable to the signal bandwidth. This greatly improves the preamplifier's signal to noise ratio (in this case, by a factor of three).

Photodiode Array Processor

The AD546 is a cost effective preamp for multichannel applications, such as amplifying signals from photo diode arrays, as illustrated in Figure 43. An AD546 preamp converts each of the diodes' output currents to a voltage. An 8 to 1 multiplexer switches a particular preamp output to the input of an AD1380 16-bit sampling ADC. The output of the ADC can be displayed or put onto a databus. Additional preamps and muxes can be added to handle larger arrays. Layout of multichannel circuits is critical. Refer to "PC board notes" for guidance.

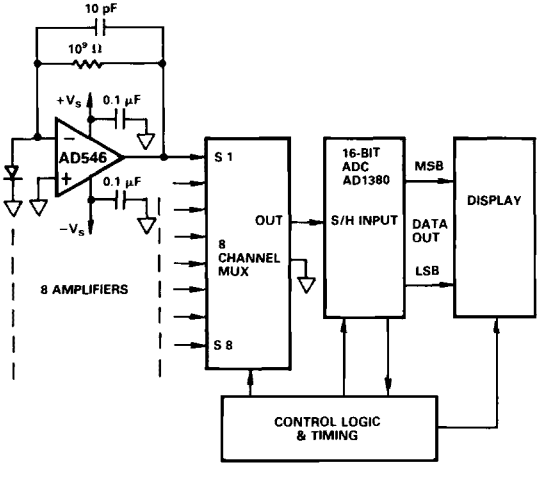


Figure 43. Photodiode Array Processor

pH PROBE AMPLIFIER

A pH probe can be modeled as a mV-level voltage source with a series source resistance dependent upon the electrode's composition and configuration. The glass bulb resistance of a typical pH electrode pair falls between 10^6 and 10^9 Ω. It is therefore important to select an amplifier with low enough input currents such that the voltage drop produced by the amplifier's input bias current and the electrode resistance does not become an appreciable percentage of a pH unit.

The circuit in Figure 44 illustrates the use of the AD546 as a pH probe amplifier. As with other electrometer applications, the use of guarding, shielding, Teflon standoffs, etc., is a must in order to capitalize on the AD546's low input current. If an AD546J (1 pA max input current) is used, the error contributed by input current will be held below 10 mV for pH electrode source impedances up to 10^9 Ω. Input offset voltage (which can be trimmed) will be below 2 mV. Refer to AD549 data sheet for temperature compensated pH probe amplifier circuit.

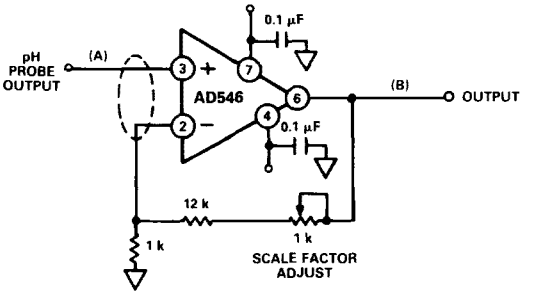


Figure 44. pH Probe Amplifier

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation[2]	500mW
Input Voltage[3]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (Q, H)	−65°C to +150°C
(N, R)	−65°C to +125°C
Operating Temperature Range	
AD548J/K	0 to +70°C
AD548A/B/C	−40°C to +85°C
AD548S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60sec)	300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics

8-Pin SOIC Package: $\theta_{JA} = 160°C/W$, $\theta_{JC} = 42°C/W$

8-Pin Plastic Package: $\theta_{JA} = 90°C/W$

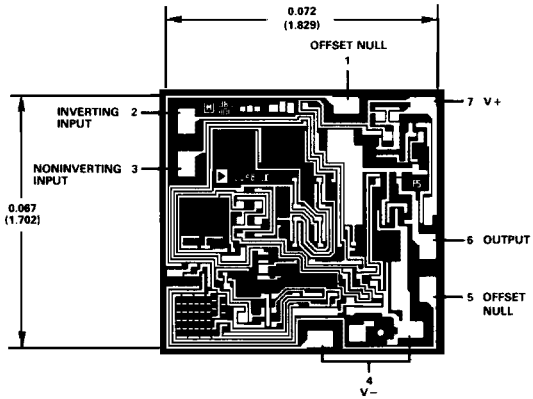
8-Pin Cerdip Package: $\theta_{JC} = 22°C/W$, $\theta_{JA} = 110°C/W$

8-Pin Metal Can Package: $\theta_{JC} = 65°C/W$, $\theta_{JA} = 150°C/W$

[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



2

Typical Characteristics

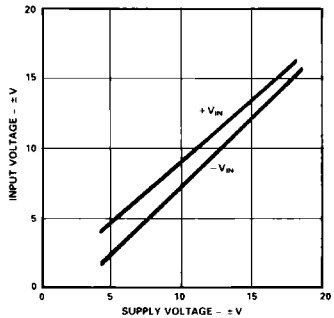


Figure 1. Input Voltage Range vs. Supply Voltage

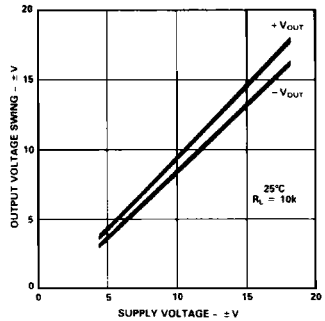


Figure 2. Output Voltage Swing vs. Supply Voltage

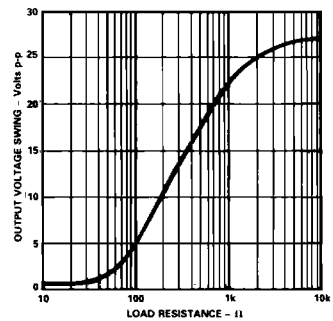


Figure 3. Output Voltage Swing vs. Load Resistance

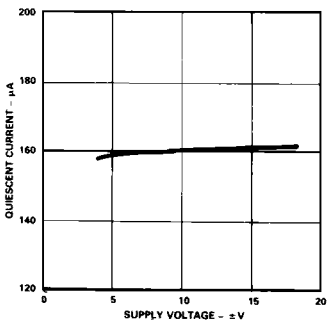


Figure 4. Quiescent Current vs. Supply Voltage

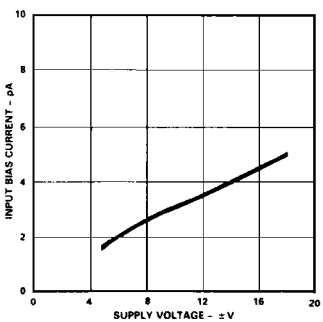


Figure 5. Input Bias Current vs. Supply Voltage

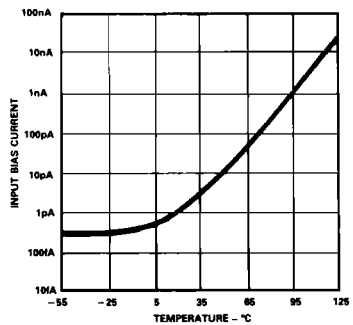


Figure 6. Input Bias Current vs. Temperature

AD548—Typical Characteristics

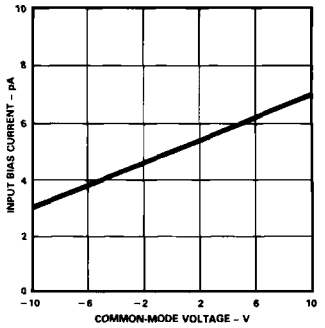


Figure 7. Input Bias Current vs. Common-Mode Voltage

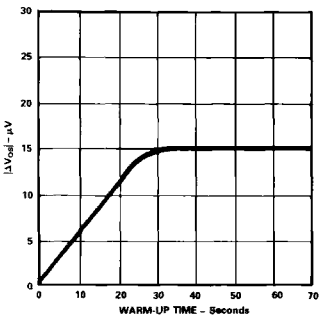


Figure 8. Change in Offset Voltage vs. Warm-Up Time

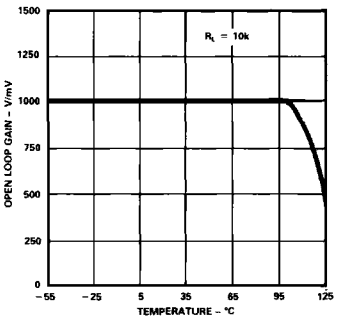


Figure 9. Open Loop Gain vs. Temperature

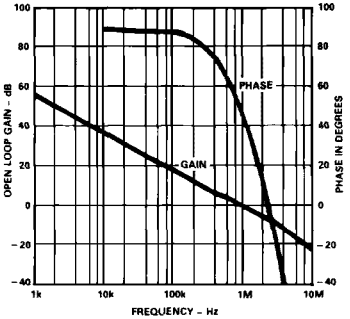


Figure 10. Open Loop Frequency Response

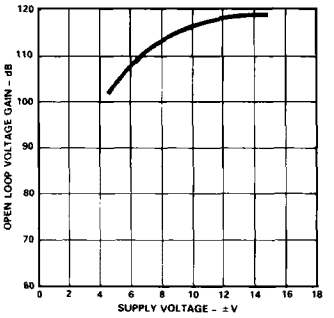


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

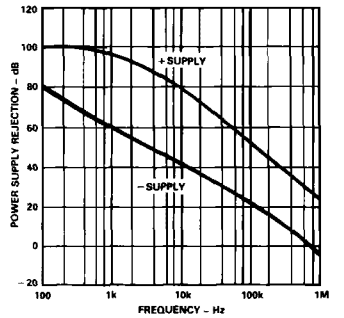


Figure 12. PSRR vs. Frequency

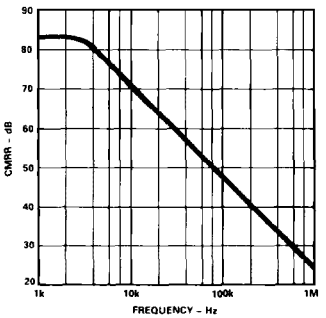


Figure 13. CMRR vs. Frequency

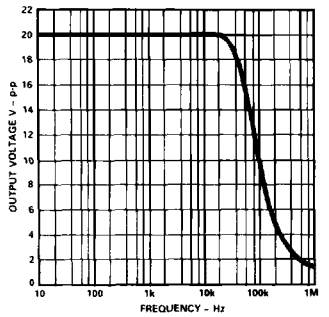


Figure 14. Large Signal Frequency Response

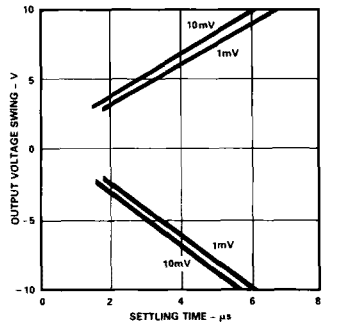


Figure 15. Output Swing and Error Voltage vs. Output Settling Time

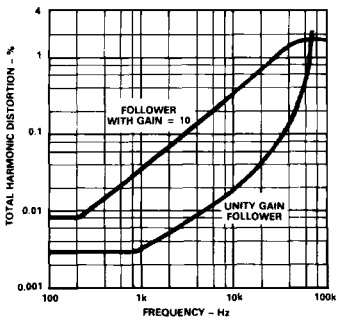


Figure 16. Total Harmonic Distortion vs. Frequency

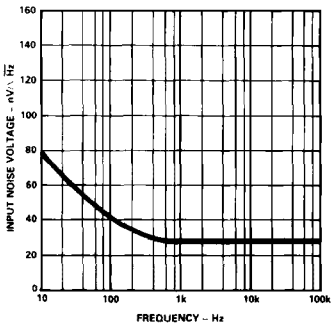


Figure 17. Input Noise Voltage Spectral Density

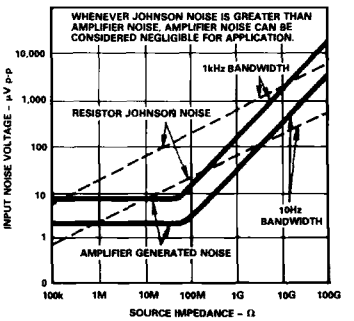


Figure 18. Total Noise vs. Source Impedance

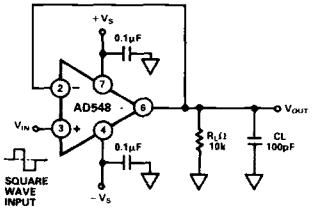


Figure 19a. Unity Gain Follower

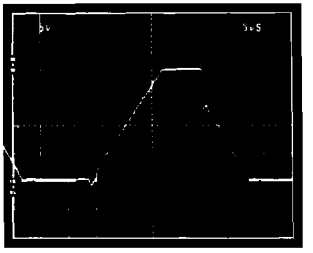


Figure 19b. Unity Gain Follower Pulse Response (Large Signal)

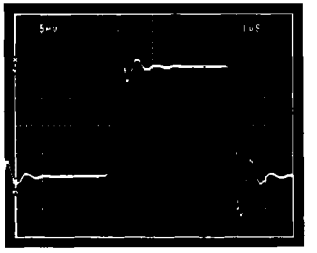


Figure 19c. Unity Gain Follower Pulse Response (Small Signal)

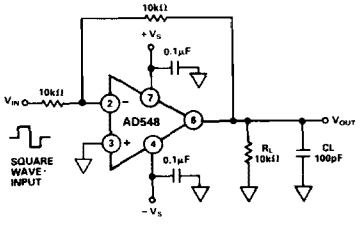


Figure 20a. Unity Gain Inverter

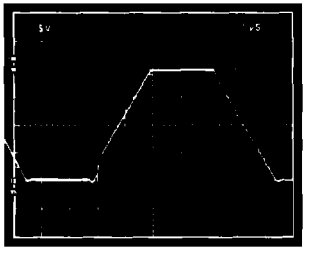


Figure 20b. Unity Gain Inverter Pulse Response (Large Signal)

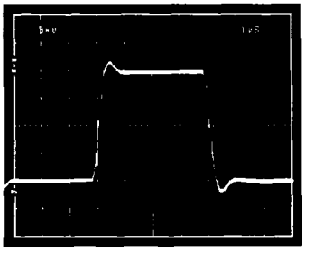


Figure 20c. Unity Gain Inverter Pulse Response (Small Signal)

2

Applying the AD548

APPLICATION NOTES

The AD548 is a JFET-input op amp with a guaranteed maximum I_B of less than 10pA, and offset and drift laser-trimmed to 0.25mV and 2μV/°C respectively (AD548C). AC specs include 1MHz bandwidth, 1.8V/μs typical slew rate and 8μs settling time for a 20V step to ±0.01% – all at a supply current less than 200μA. To capitalize on the device's performance, a number of error sources should be considered.

The minimal power drain and low offset drift of the AD548 reduce self-heating or "warm-up" effects on input offset voltage, making the AD548 ideal for on/off battery powered applications. The power dissipation due to the AD548's 200μA supply current has a negligible effect on input current, but heavy output loading will raise the chip temperature. Since a JFET's input current doubles for every 10°C rise in chip temperature, this can be a noticeable effect.

The amplifier is designed to be functional with power supply voltages as low as ±4.5V. It will exhibit a higher input offset voltage than at the rated supply voltage of ±15V, due to power supply rejection effects. The common-mode range of the AD548 extends from 3V more positive than the negative supply to 1V more negative than the positive supply. Designed to cleanly drive up to 10kΩ and 100pF loads, the AD548 will drive a 2kΩ load with reduced open loop gain.

OFFSET NULLING

Unlike bipolar input amplifiers, zeroing the input offset voltage of a BiFET op amp will not minimize offset drift. Using balance Pins 1 and 5 to adjust the input offset voltage as shown in Figure 21 will induce an added drift of 0.24μV/°C per 100μV of nulled offset. The low initial offset (0.25mV) of the AD548C results in only 0.6μV/°C of additional drift.

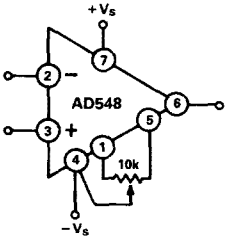


Figure 21. Offset Null Configuration

LAYOUT

To take full advantage of the AD548's 10pA max input current, parasitic leakages must be kept below an acceptable level. The practical limit of the resistance of epoxy or phenolic circuit board material is between $1 \times 10^{12}\Omega$ and $3 \times 10^{12}\Omega$. This can result in an additional leakage of 5pA between an input of 0V and a −15V supply line. Teflon or a similar low leakage material (with a resistance exceeding $10^{17}\Omega$) should be used to isolate high impedance input lines from adjacent lines carrying high voltages. The insulator should be kept clean, since contaminants will degrade the surface resistance.

A metal guard completely surrounding the high impedance nodes and driven by a voltage near the common-mode input potential can also be used to reduce some parasitic leakages. The guarding pattern in Figure 22 will reduce parasitic leakage due to finite board surface resistance; but it will not compensate for a low volume resistivity board.

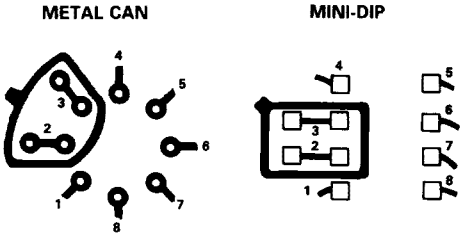


Figure 22. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD548 is guaranteed to withstand input voltages equal to the power supply potential. Exceeding the negative supply voltage on either input will forward bias the substrate junction of the chip. The induced current may destroy the amplifier due to excess heat.

Input protection is required in applications such as a flame detector in a gas chromatograph, where a very high potential may be applied to the input terminals during a sensor fault condition. Figure 23 shows a simple current limiting scheme that can be used. $R_{PROTECT}$ should be chosen such that the maximum overload current is 1.0mA (100kΩ for a 100V overload, for example).

Exceeding the negative common-mode range on either input terminal causes a phase reversal at the output, forcing the amplifier output to the corresponding high or low state. Exceeding the negative common-mode on both inputs simultaneously forces the output high. Exceeding the positive common-mode range on a single input doesn't cause a phase reversal, but if both inputs exceed the limit the output will be forced high. In all cases, normal amplifier operation is resumed when input voltages are brought back within the common-mode range.

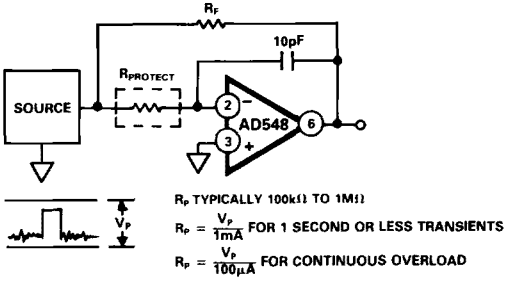


Figure 23. Input Protection of IV Converter

D/A CONVERTER OUTPUT BUFFER

The circuit in Figure 24 shows the AD548 and AD7545 12-bit CMOS D/A converter in a unipolar binary configuration. V_{OUT} will be equal to V_{REF} attenuated by a factor depending on the digital word. V_{REF} sets the full scale. Overall gain is trimmed by adjusting R_{IN}. The AD548's low input offset voltage, low drift and clean dynamics make it an attractive low power output buffer.

The input offset voltage of the AD548 output amplifier results in an output error voltage. This error voltage equals the input offset voltage of the op amp times the noise gain of the amplifier.

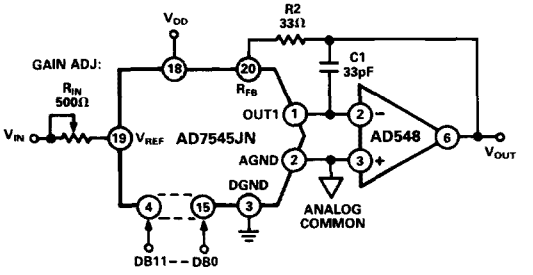


Figure 24. AD548 Used as DAC Output Amplifier

That is:

$$V_{OS}\ \text{Output} = V_{OS}\ \text{Input}\left(1+\frac{R_{FB}}{R_O}\right)$$

R_{FB} is the feedback resistor for the op amp, which is internal to the DAC. R_O is the DAC's R-2R ladder output resistance. The value of R_O is code dependent. This has the effect of changing the offset error voltage at the amplifier's output. An output amplifier with a sub millivolt input offset voltage is needed to preserve the linearity of the DAC's transfer function.

The AD548 in this configuration provides a 700kHz small signal bandwidth and 1.8V/μs typical slew rate. The 33pF capacitor across the feedback resistor optimizes the circuit's response. The oscilloscope photos in Figures 25 and 26 show small and large signal outputs of the circuit in Figure 24. Upper traces show the input signal V_{IN}. Lower traces are the resulting output voltage with the DAC's digital input set to all 1s. The AD548 settles to ±0.01% for a 20V input step in 14μs.

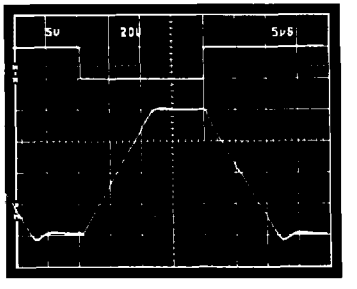


Figure 25. Response to ±20V p-p Reference Square Wave

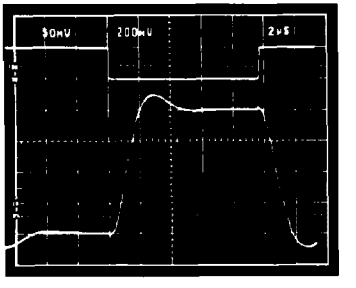


Figure 26. Response to ±100mV p-p Reference Square Wave

PHOTODIODE PREAMP

The performance of the photodiode preamp shown in Figure 27 is enhanced by the AD548's low input current, input voltage offset and offset voltage drift. The photodiode sources a current proportional to the incident light power on its surface. R_F converts the photodiode current to an output voltage equal to $R_F \times I_S$.

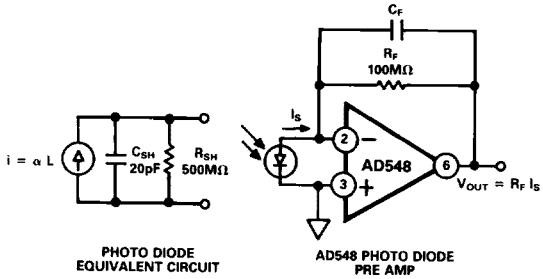


Figure 27.

An error budget illustrating the importance of low amplifier input current, voltage offset and offset voltage drift to minimize output voltage errors can be developed by considering the equivalent circuit for the small (0.2mm² area) photodiode shown in Figure 27. The input current results in an error proportional to the feedback resistance used. The amplifier's offset will produce an error proportional to the preamp's noise gain $(1 + R_F/R_{SH})$, where R_{SH} is the photodiode shunt resistance. The amplifier's input current will double with every 10°C rise in temperature, and the photodiode's shunt resistance halves with every 10°C rise. The error budget in Figure 28 assumes a room temperature photodiode R_{SH} of 500MΩ, and the maximum input current and input offset voltage specs of an AD548C.

TEMP °C	R_{SH} (MΩ)	V_{OS} (μV)	$(1 + R_F/R_{SH})\,V_{OS}$	I_B (pA)	$I_B R_F$	TOTAL
−25	15,970	150	151μV	0.30	30μV	181μV
0	2,830	200	207μV	2.26	262μV	469μV
+25	500	250	300μV	10.00	1.0mV	1.30mV
+50	88.5	300	640μV	56.6	5.6mV	6.24mV
+75	15.6	350	2.6mV	320	32mV	34.6mV
+85	7.8	370	5.1mV	640	64mV	69.1mV

Figure 28. Photo Diode Pre-Amp Errors Over Temperature

The capacitance at the amplifier's negative input (the sum of the photodiode's shunt capacitance, the op amp's differential input capacitance, stray capacitance due to wiring, etc.) will cause a rise in the preamp's noise gain over frequency. This can result in excess noise over the bandwidth of interest. C_F reduces the noise gain "peaking" at the expense of bandwidth.

INSTRUMENTATION AMPLIFIER

The AD548C's maximum input current of 10pA makes it an excellent building block for the high input impedance instrumentation amplifier shown in Figure 29. Total current drain for this circuit is under 600μA. This configuration is optimal for conditioning differential voltages from high impedance sources.

The overall gain of the circuit is controlled by R_G, resulting in the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{(R_1 + R_2)}{R_G}$$

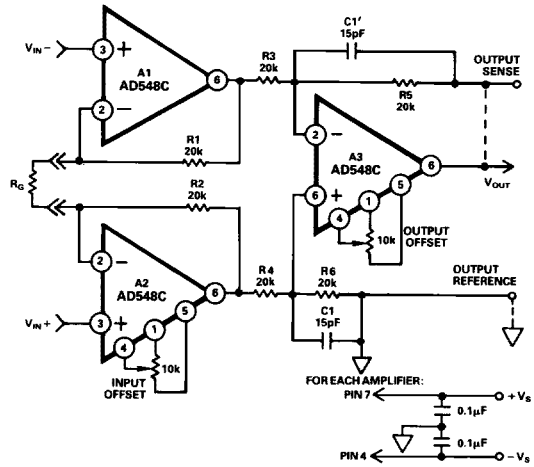


Figure 29. Low Power Instrumentation Amplifier

Gains of 1 to 100 can be accommodated with gain nonlinearities of less than 0.01%. Referred to input errors, which contribute an output error proportional to in amp gain, include a maximum untrimmed input offset voltage of 0.5mV and an input offset voltage drift over temperature of 4μV/°C. Output errors, which are independent of gain, will contribute an additional 0.5mV offset and 4μV/°C drift. The maximum input current is 15pA over the common-mode range, with a common-mode impedance of over $1 \times 10^{12}\Omega$. Resistor pairs R3/R5 and R4/R6 should be ratio matched to 0.01% to take full advantage of the AD548's high common mode rejection. Capacitors C1 and C1′ compensate for peaking in the gain over frequency caused by input capacitance when gains of 1 to 3 are used.

The −3dB small signal bandwidth for this low power instrumentation amplifier is 700kHz for a gain of 1 and 10kHz for a gain of 100. The typical output slew rate is 1.8V/μs.

LOG RATIO AMPLIFIER

Log ratio amplifiers are useful for a variety of signal conditioning applications, such as linearizing exponential transducer outputs and compressing analog signals having a wide dynamic range. The AD548's picoamp level input current and low input offset voltage make it a good choice for the front-end amplifier of the log ratio circuit shown in Figure 30. This circuit produces an output voltage equal to the log base 10 of the ratio of the input currents I_1 and I_2. Resistive inputs R1 and R2 are provided for voltage inputs.

Input currents I_1 and I_2 set the collector currents of Q1 and Q2, a matched pair of logging transistors. Voltages at points A and B are developed according to the following familiar diode equation:

$$V_{BE} = (kT/q)\ \ln\ (I_C/I_{ES})$$

In this equation, k is Boltzmann's constant, T is absolute temperature, q is an electron charge, and I_{ES} is the reverse saturation current of the logging transistors. The difference of these two voltages is taken by the subtractor section and scaled by a factor of approximately 16 by resistors R9, R10, and R8. Temperature

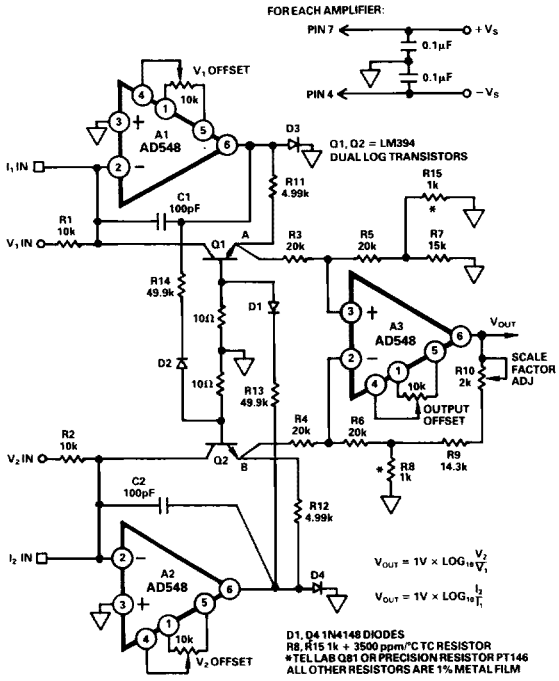


Figure 30. Log Ratio Amplifier

compensation is provided by resistors R8 and R15, which have a positive 3500 ppm/°C temperature coefficient. The transfer function for the output voltage is:

$$V_{OUT} = 1V \log_{10} (I_2/I_1)$$

Frequency compensation is provided by R11, R12, C1, and C2. Small signal bandwidth is approximately 300kHz at input currents above 100μA and will proportionally decrease with lower signal levels. D1, D2, R13, and R14 compensate for the effects of the two logging transistors' ohmic emitter resistance.

To trim this circuit, set the two input currents to 10μA and adjust V_{OUT} to zero by adjusting the potentiometer on A3. Then set I_2 to 1μA and adjust the scale factor such that the output voltage is 1V by trimming potentiometer R10. Offset adjustment for A1 and A2 is provided to increase the accuracy of the voltage inputs.

This circuit ensures a 1% log conformance error over an input current range of 300pA to 1mA, with low level accuracy limited by the AD548's input current. The low level input voltage accuracy of this circuit is limited by the input offset voltage and drift of the AD548.