

NT1GT72U89D0BD-AC / NT2GT72U8PD0BD-AC / NT4GT72U4ND0BD-AC / NT4GT72U8ND9BD-AC
 NT1GT72U89D1BD-3C / NT2GT72U8PD1BD-3C / NT4GT72U4ND1BD-3C / NT8GTT72U4ND3YD-3C
 NT1GT72U89D1BN-3C / NT2GT72U8PD1BN-3C / NT4GT72U4ND1BN-3C / NT8GTT72U4ND4YD-3C
 NT1GT72U89D2BD-3C / NT2GT72U8PD2BD-3C / NT4GT72U4ND2BD-3C / NT8GTT72U4ND5YD-3C
 NT1GT72U89D6BD-AC / NT2GT72U8PD6BD-AC / NT4GT72U8ND9BD-3C



240pin DDR2 SDRAM Fully Buffered DIMM

Based on 128Mx8 (1GB/2GB/4GB), 256Mx4 (4GB), and 512Mx4 (8GB) DDR2 SDRAM

Features

•Performance:

| Speed Sort | PC2-5300 | PC2-6400 | Unit |
|--------------------------|----------|----------|------|
| | -3C | -AC | |
| DIMM CAS Latency | 5 | 5 | |
| fck – Clock Frequency | 333 | 400 | MHz |
| tck – Clock Cycle | 3 | 2.5 | ns |
| fDQ – DQ Burst Frequency | 667 | 800 | Mbps |

- 1GB/2GB: 128Mx72/256Mx72 DDR2 Fully Buffered DIMM based on 128Mx8 DDR2 SDRAM (NT5TU128M8DE-3C/-AC)
- 4GB: 512Mx72 DDR2 Fully Buffered DIMM based on 128Mx8/256Mx4 DDR2 SDRAM (NT5TU256M4DE-3C/-AC)/ (NT5TU128M8DE-3C/-AC)
- 8GB: 1Gx72 DDR2 Fully Buffered DIMM based on 512Mx4 DDR2 SDRAM (NT5TU512T4DY-3C)
- JEDEC Standard 240-pin Fully Buffered ECC Dual In-Line Memory Module.
- Intended for 333MHz/400MHz applications.
- Inputs and outputs are SSTL-18 compatible.
- VDD = 1.8V ± 0.1V, VDDQ = 1.8V ± 0.1V.
- Host Interface and AMB component industry standard compliant.
- Support SMBus protocol interface for access to the AMB configuration registers.
- Detects errors on the channel and reports them to the host memory controller.
- Automatic DDR2 DRAM Bus Calibration.
- Full Host Control of the DDR2 DRAMs.
- Over-Temperature Detection and Alert.
- MBIST & IBIST Test Functions.
- Transparent Mode for DRAM Test Support.
- Serial Presence Detect (SPD)
- Gold contacts
- RoHS Compliant products
- SDRAMs in 60-ball BGA Package

Description

Fully Buffered 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Dual In-Line Memory Module (DIMM), organized as an eight bank 128Mx72 (1GB), 256Mx72 (2GB), 512Mx72 (4GB), or 1Gx72 (8GB) high-speed memory array. The module uses nine 128Mx8 (1GB), eighteen 128Mx8 (2GB), thirty-six 128Mx8/256Mx4 (4GB), or thirty-six 512Mx4 (8GB) DDR2 SDRAMs in BGA packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 333MHz/400 MHz clock speeds and achieves high-speed data transfer rates of up to 667 Mbps/800 Mbps. Prior to any access operation, the device $\overline{\text{CAS}}$ latency and burst type/length/operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0, BA1, and BA2 using the mode register set cycle.

NT1GT72U89D0BD-AC / NT2GT72U8PD0BD-AC / NT4GT72U4ND0BD-AC / NT4GT72U8ND9BD-AC
 NT1GT72U89D1BD-3C / NT2GT72U8PD1BD-3C / NT4GT72U4ND1BD-3C / NT8GTT72U4ND3YD-3C
 NT1GT72U89D1BN-3C / NT2GT72U8PD1BN-3C / NT4GT72U4ND1BN-3C / NT8GTT72U4ND4YD-3C
 NT1GT72U89D2BD-3C / NT2GT72U8PD2BD-3C / NT4GT72U4ND2BD-3C / NT8GTT72U4ND5YD-3C
 NT1GT72U89D6BD-AC / NT2GT72U8PD6BD-AC / NT4GT72U8ND9BD-3C



Ordering Information

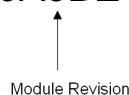
| Part Number | AMB | Speed | | | Organization | Leads | Power |
|--------------------|----------|----------------------------|----------|----------|--------------------------|---------|----------|
| NT1GT72U89D0BD-AC | IDT C1 | 400MHz (2.5ns @ CL = 5) | DDR2-800 | PC2-6400 | 128Mx72 | Gold | 1.8V |
| NT1GT72U89D6BD-AC | | | | | | | |
| NT1GT72U89D1BD-3C | IDT C1 | 333MHz (3ns @ CL = 5) | DDR2-667 | PC2-5300 | | | |
| NT1GT72U89D2BD-3C | IDT AMB+ | | | | | | |
| NT1GT72U89D1BN-3C | Intel D1 | 400MHz (2.5ns @ CL = 5) | DDR2-800 | PC2-6400 | | | |
| NT2GT72U8PD0BD-AC | IDT C1 | | | | | | |
| NT2GT72U8PD6BD-AC | IDT C1 | | | | | | |
| NT2GT72U8PD1BD-3C | IDT C1 | 333MHz (3ns @ CL = 5) | DDR2-667 | PC2-5300 | 256Mx72 | | |
| NT2GT72U8PD2BD-3C | IDT AMB+ | | | | | | |
| NT2GT72U8PD1BN-3C | Intel D1 | 400MHz (2.5ns @ CL = 5) | DDR2-800 | PC2-6400 | | | |
| NT4GT72U4ND0BD-AC | IDT C1 | | | | | | |
| NT4GT72U8ND9BD-AC | IDT AMB+ | | | | | | |
| NT4GT72U4ND1BD-3C | IDT C1 | 333MHz (3ns @ CL = 5) | DDR2-667 | PC2-5300 | | 512Mx72 | |
| NT4GT72U4ND2BD-3C | IDT AMB+ | | | | | | |
| NT4GT72U4ND1BN-3C | Intel D1 | 333MHz (3ns @ CL = 5) | DDR2-667 | PC2-5300 | | | |
| NT4GT72U8ND9BD-3C | IDT AMB+ | | | | | | |
| NT8GTT72U4ND3YD-3C | IDT D0 | | | | 333MHz (3ns @ CL = 5) | | DDR2-667 |
| NT8GTT72U4ND4YD-3C | | | | | | | |
| NT8GTT72U4ND5YD-3C | IDT AMB+ | 1Gx72 | | | | | |

Note:

FBDIMM module revision will change if AMB, PCB, or Heat spreader version changes.

Ex:

NT512T72U89A0BE-4B





DIMM Connector Pin Description

| Pin Name | Pin Description | Note |
|------------------------------|--|------|
| SCK | System Clock Input, positive line | 1 |
| $\overline{\text{SCK}}$ | System Clock Input, negative line | 1 |
| PN0-PN13 | Primary Northbound Data, positive lines | |
| $\overline{\text{PN0-PN13}}$ | Primary Northbound Data, negative lines | |
| PS0-PS9 | Primary Southbound Data, positive lines | |
| $\overline{\text{PS0-PS9}}$ | Primary Southbound Data, negative lines | |
| SN0-SN13 | Secondary Northbound Data, positive lines | |
| $\overline{\text{SN0-SN13}}$ | Secondary Northbound Data, negative lines | |
| SS0-SS9 | Secondary Southbound Data, positive lines | |
| $\overline{\text{SS0-SS9}}$ | Secondary Southbound Data, negative lines | |
| SCL | Serial Presence Detect (SPD) Clock Input | |
| SDA | SPD Data Input / Output | |
| S0-S1 | SPD Address Inputs, also used to select the DIMM number in the AMB | |
| VID0-VID1 | Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs VID0 is V_{DD} value: OPEN=1.8V, GND=1.5V; VID1 is V_{CC} value: OPEN=1.5V, GND=1.2V | |
| $\overline{\text{RESET}}$ | AMB reset signal | |
| RFU | Reserved for Future Use | 2 |
| V_{CC} | AMB Core Power and AMB Channel Interface Power (1.5V) | |
| V_{DD} | DRAM Power and AMB DRAM I/O Power (1.8V) | |
| V_{TT} | DRAM Address/Command/Clock Termination Power ($V_{DD}/2$) | |
| V_{DDSPD} | SPD Power (3.3V) | |
| V_{SS} | Ground | |
| DNU/M_TEST | It provides an external connection on R/Cs A-D for testing the margin of V_{ref} which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time. | 1 |

Note: 1. System Clock Signals SCK and $\overline{\text{SCK}}$ switch at one half the DRAM CK/ $\overline{\text{CK}}$ frequency
 2. Eight pins reserved for forwarded clocks, eight pins reserved for future architecture flexibility



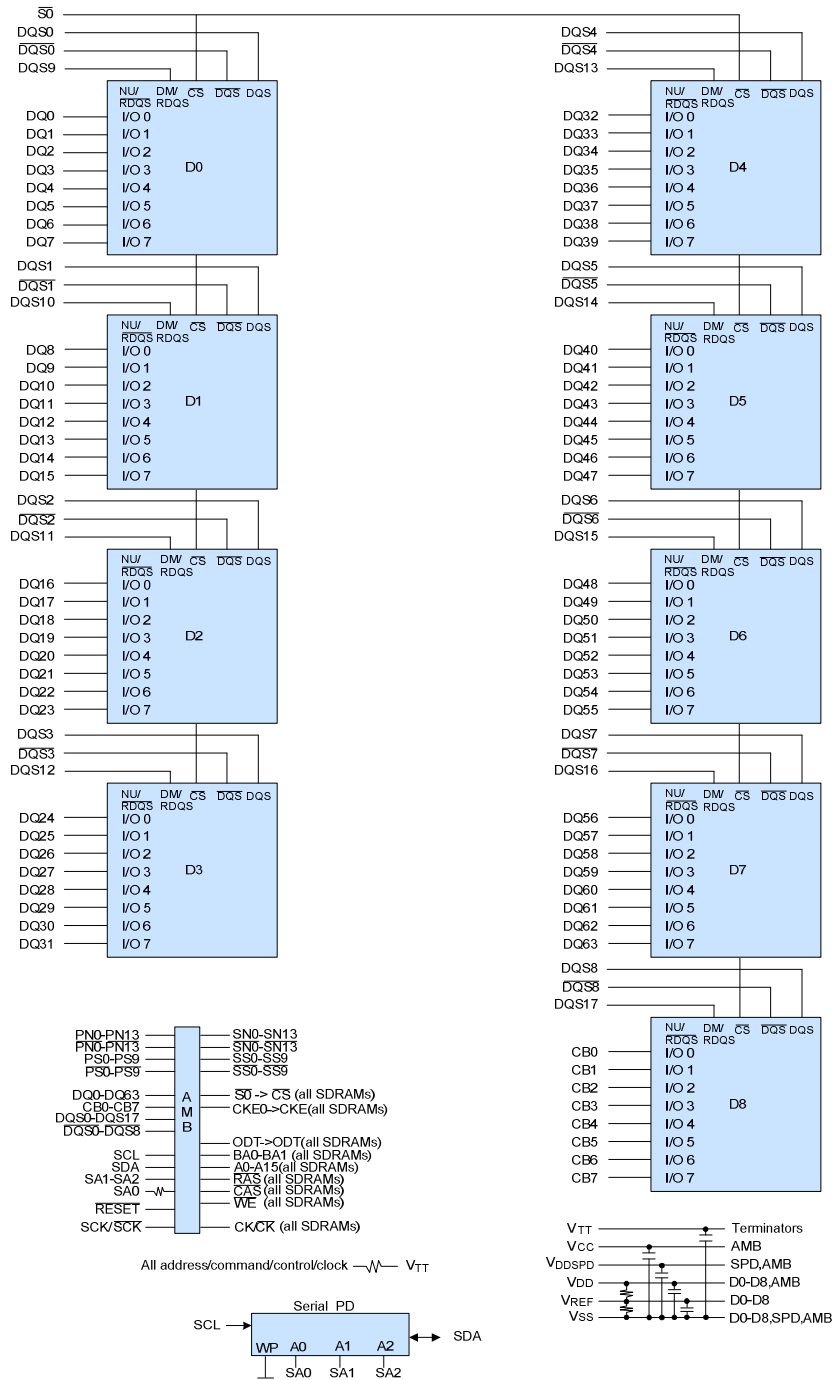
DDR2 240-pin FBDIMM Pinout

| Pin | Front Side | Pin | Front Side | Pin | Front Side | Pin | Back Side | Pin | Back Side | Pin | Back Side |
|-----|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|--------------------|
| 1 | V _{DD} | 42 | V _{SS} | 82 | PS4 | 121 | V _{DD} | 162 | V _{SS} | 202 | SS4 |
| 2 | V _{DD} | 43 | V _{SS} | 83 | PS4 | 122 | V _{DD} | 163 | V _{SS} | 203 | SS4 |
| 3 | V _{DD} | 44 | RFU* | 84 | V _{SS} | 123 | V _{DD} | 164 | RFU* | 204 | V _{SS} |
| 4 | V _{SS} | 45 | RFU* | 85 | V _{SS} | 124 | V _{SS} | 165 | RFU* | 205 | V _{SS} |
| 5 | V _{DD} | 46 | V _{SS} | 86 | RFU* | 125 | V _{DD} | 166 | V _{SS} | 206 | RFU* |
| 6 | V _{DD} | 47 | V _{SS} | 87 | RFU* | 126 | V _{DD} | 167 | V _{SS} | 207 | RFU* |
| 7 | V _{DD} | 48 | PN12 | 88 | V _{SS} | 127 | V _{DD} | 168 | SN12 | 208 | V _{SS} |
| 8 | V _{SS} | 49 | PN12 | 89 | V _{SS} | 128 | V _{SS} | 169 | SN12 | 209 | V _{SS} |
| 9 | V _{CC} | 50 | V _{SS} | 90 | PS9 | 129 | V _{CC} | 170 | V _{SS} | 210 | SS9 |
| 10 | V _{CC} | 51 | PN6 | 91 | PS9 | 130 | V _{CC} | 171 | SN6 | 211 | SS9 |
| 11 | V _{SS} | 52 | PN6 | 92 | V _{SS} | 131 | V _{SS} | 172 | SN6 | 212 | V _{SS} |
| 12 | V _{CC} | 53 | V _{SS} | 93 | PS5 | 132 | V _{CC} | 173 | V _{SS} | 213 | SS5 |
| 13 | V _{CC} | 54 | PN7 | 94 | PS5 | 133 | V _{CC} | 174 | SN7 | 214 | SS5 |
| 14 | V _{SS} | 55 | PN7 | 95 | V _{SS} | 134 | V _{SS} | 175 | SN7 | 215 | V _{SS} |
| 15 | V _{TT} | 56 | V _{SS} | 96 | PS6 | 135 | V _{TT} | 176 | V _{SS} | 216 | SS6 |
| 16 | VID1 | 57 | PN8 | 97 | PS6 | 136 | VID0 | 177 | SN8 | 217 | SS6 |
| 17 | RESET | 58 | PN8 | 98 | V _{SS} | 137 | DNU/M_TEST | 178 | SN8 | 218 | V _{SS} |
| 18 | V _{SS} | 59 | V _{SS} | 99 | PS7 | 138 | V _{SS} | 179 | V _{SS} | 219 | SS7 |
| 19 | RFU** | 60 | PN9 | 100 | PS7 | 139 | RFU** | 180 | SN9 | 220 | SS7 |
| 20 | RFU** | 61 | PN9 | 101 | V _{SS} | 140 | RFU** | 181 | SN9 | 221 | V _{SS} |
| 21 | V _{SS} | 62 | V _{SS} | 102 | PS8 | 141 | V _{SS} | 182 | V _{SS} | 222 | SS8 |
| 22 | PN0 | 63 | PN10 | 103 | PS8 | 142 | SN0 | 183 | SN10 | 223 | SS8 |
| 23 | PN0 | 64 | PN10 | 104 | V _{SS} | 143 | SN0 | 184 | SN10 | 224 | V _{SS} |
| 24 | V _{SS} | 65 | V _{SS} | 105 | RFU** | 144 | V _{SS} | 185 | V _{SS} | 225 | RFU** |
| 25 | PN1 | 66 | PN11 | 106 | RFU** | 145 | SN1 | 186 | SN11 | 226 | RFU** |
| 26 | PN1 | 67 | PN11 | 107 | V _{SS} | 146 | SN1 | 187 | SN11 | 227 | V _{SS} |
| 27 | V _{SS} | 68 | V _{SS} | 108 | V _{DD} | 147 | V _{SS} | 188 | V _{SS} | 228 | SCK |
| 28 | PN2 | KEY | | 109 | V _{DD} | 148 | SN2 | KEY | | 229 | SCK |
| 29 | PN2 | 69 | V _{SS} | 110 | V _{SS} | 149 | SN2 | 189 | V _{SS} | 230 | V _{SS} |
| 30 | V _{SS} | 70 | PS0 | 111 | V _{DD} | 150 | V _{SS} | 190 | SS0 | 231 | V _{DD} |
| 31 | PN3 | 71 | PS0 | 112 | V _{DD} | 151 | SN3 | 191 | SS0 | 232 | V _{DD} |
| 32 | PN3 | 72 | V _{SS} | 113 | V _{DD} | 152 | SN3 | 192 | V _{SS} | 233 | V _{DD} |
| 33 | V _{SS} | 73 | PS1 | 114 | V _{SS} | 153 | V _{SS} | 193 | SS1 | 234 | V _{SS} |
| 34 | PN4 | 74 | PS1 | 115 | V _{DD} | 154 | SN4 | 194 | SS1 | 235 | V _{DD} |
| 35 | PN4 | 75 | V _{SS} | 116 | V _{DD} | 155 | SN4 | 195 | V _{SS} | 236 | V _{DD} |
| 36 | V _{SS} | 76 | PS2 | 117 | V _{TT} | 156 | V _{SS} | 196 | SS2 | 237 | V _{TT} |
| 37 | PN5 | 77 | PS2 | 118 | SA2 | 157 | SN5 | 197 | SS2 | 238 | V _{DDSPD} |
| 38 | PN5 | 78 | V _{SS} | 119 | SDA | 158 | SN5 | 198 | V _{SS} | 239 | SA0 |
| 39 | V _{SS} | 79 | PS3 | 120 | SCL | 159 | V _{SS} | 199 | SS3 | 240 | SA1 |
| 40 | PN13 | 80 | PS3 | | | 160 | SN13 | 200 | SS3 | | |
| 41 | PN13 | 81 | V _{SS} | | | 161 | SN13 | 201 | V _{SS} | | |

Note: 1. RFU = Reserved Future Use
 2. * These pin positions are reserved for forwarded clocks to be used in future module implementation
 3. ** These pin positions are reserved for future architecture flexibility
 4. The following signals are CRC bits and thus appear out of the normal sequence: PN12/PN12, SN12/SN12, PN13/PN13, SN13/SN13, PS9/PS9, SS9/SS9

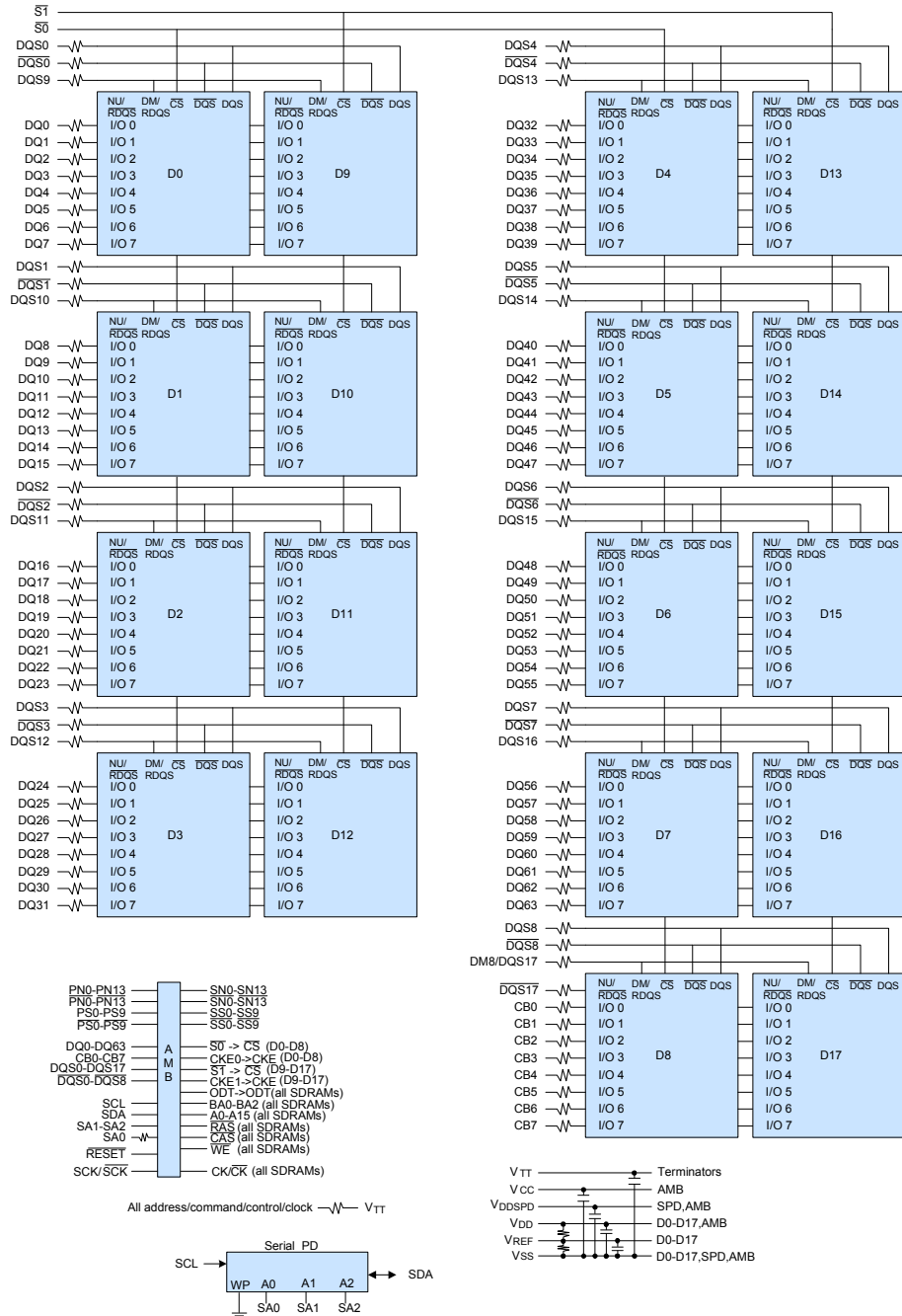


Functional Block Diagram (1GB, 1Rank, 128Mx8 DDR2 SDRAMs)





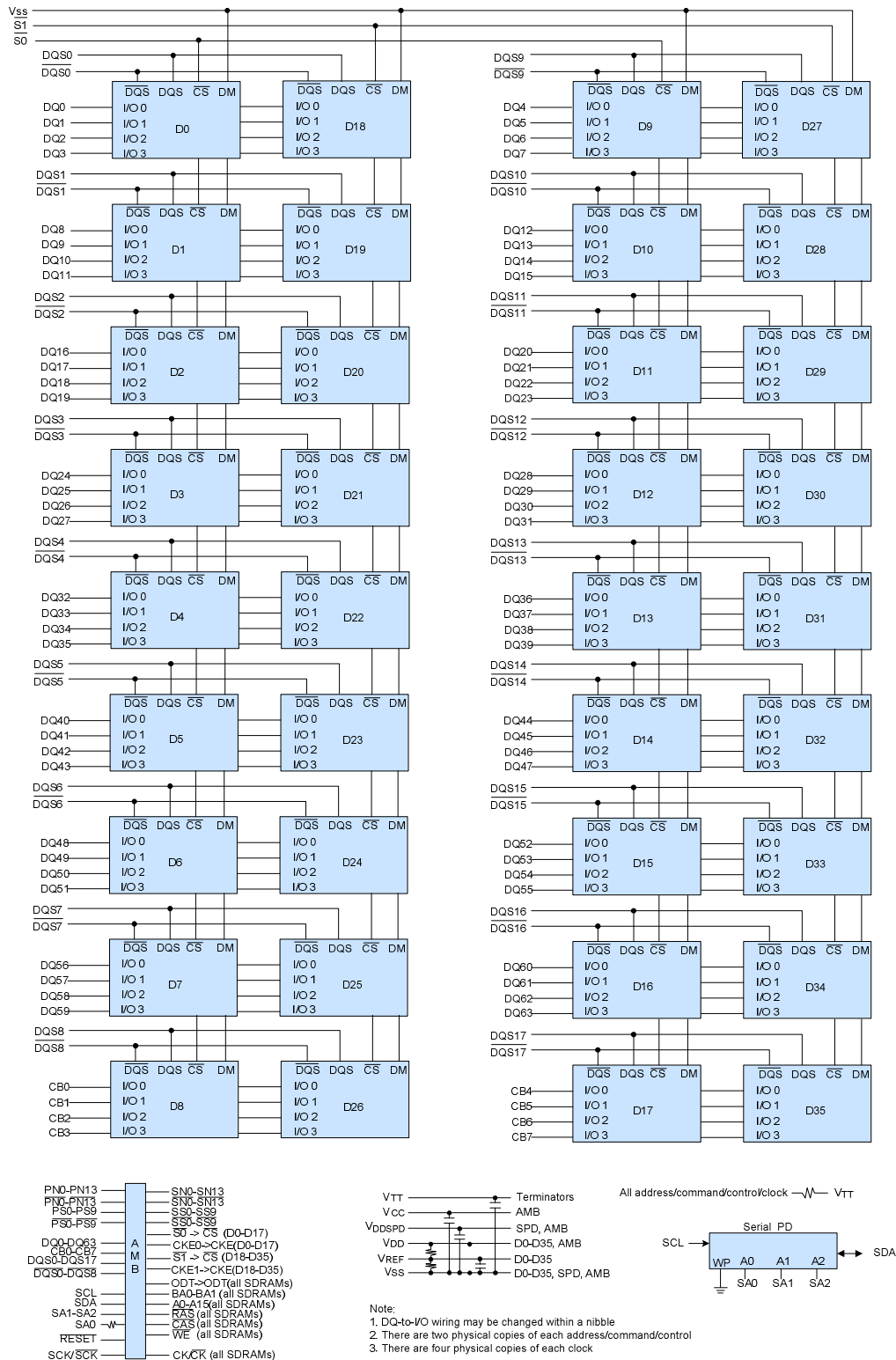
Functional Block Diagram (2GB, 2Ranks, 128Mx8 DDR2 SDRAMs)



- Notes:
1. DQ-to-I/O wiring may be changed within a byte
 2. There are two physical copies of each address/command/control/clock

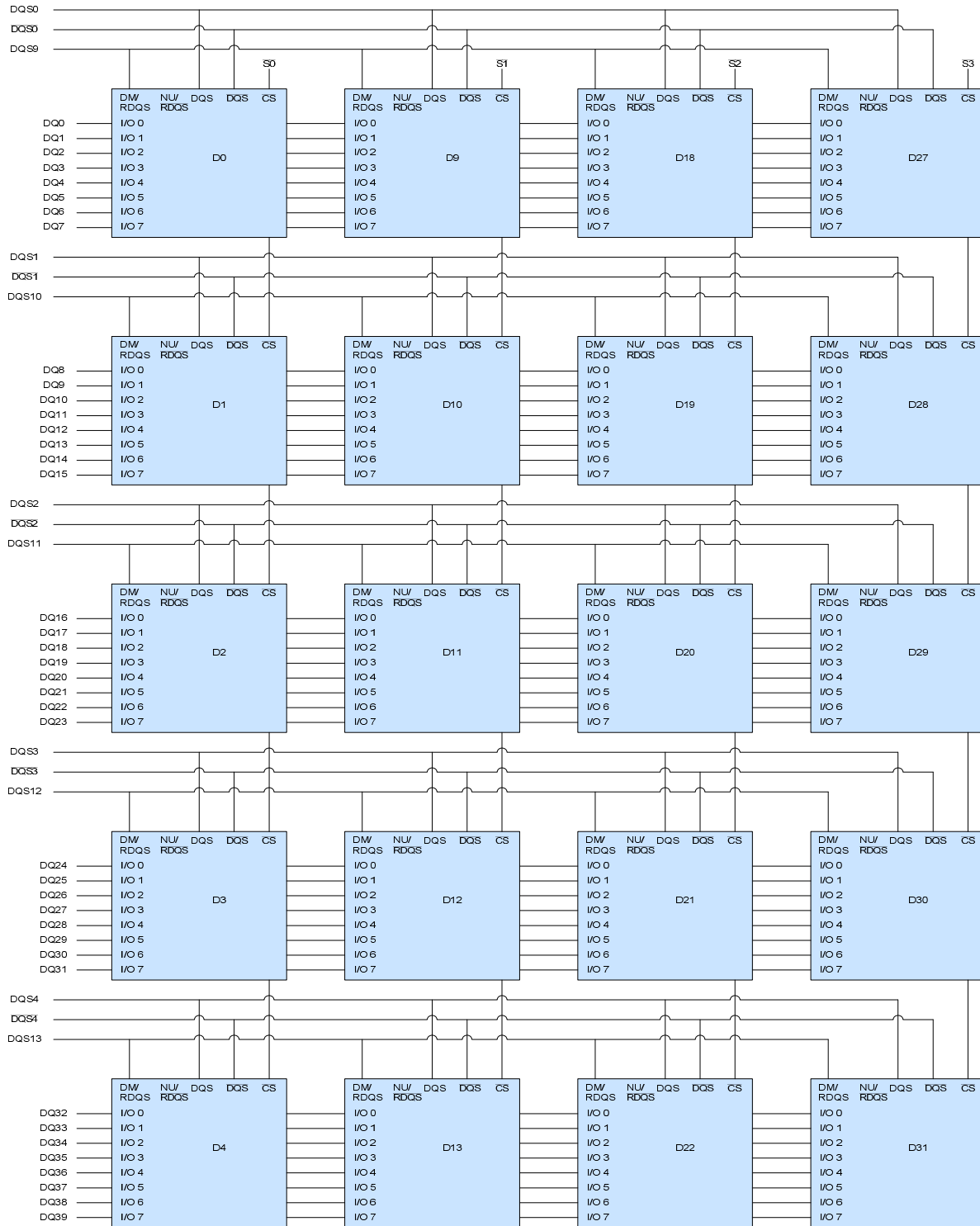


Functional Block Diagram (4GB, 2Ranks, 256Mx4 DDR2 SDRAMs)



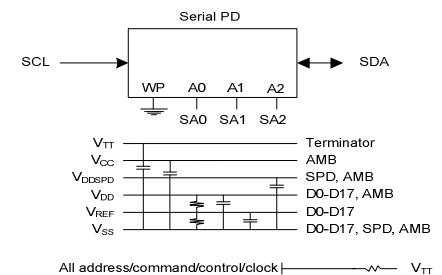
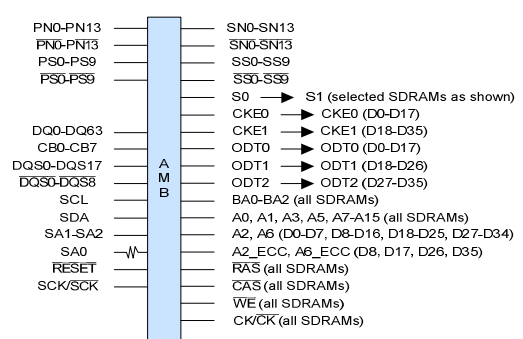
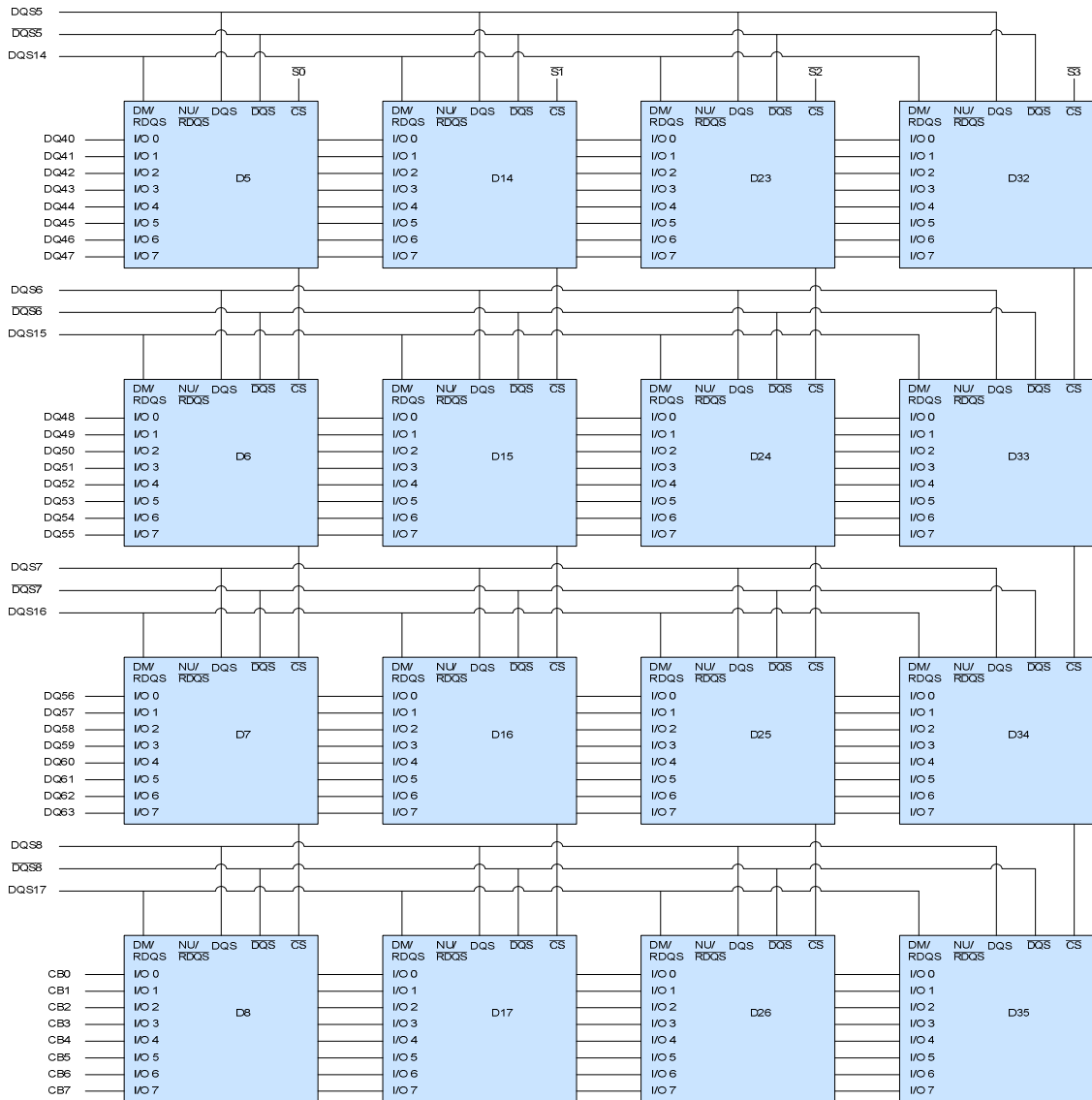


Functional Block Diagram (Part 1 of 2) (4GB, 4Rank, 128Mx8 DDR2 SDRAMs)





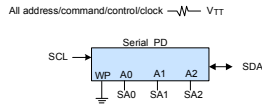
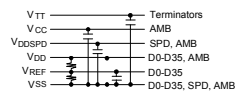
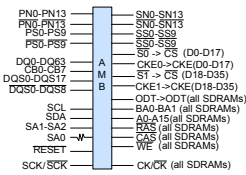
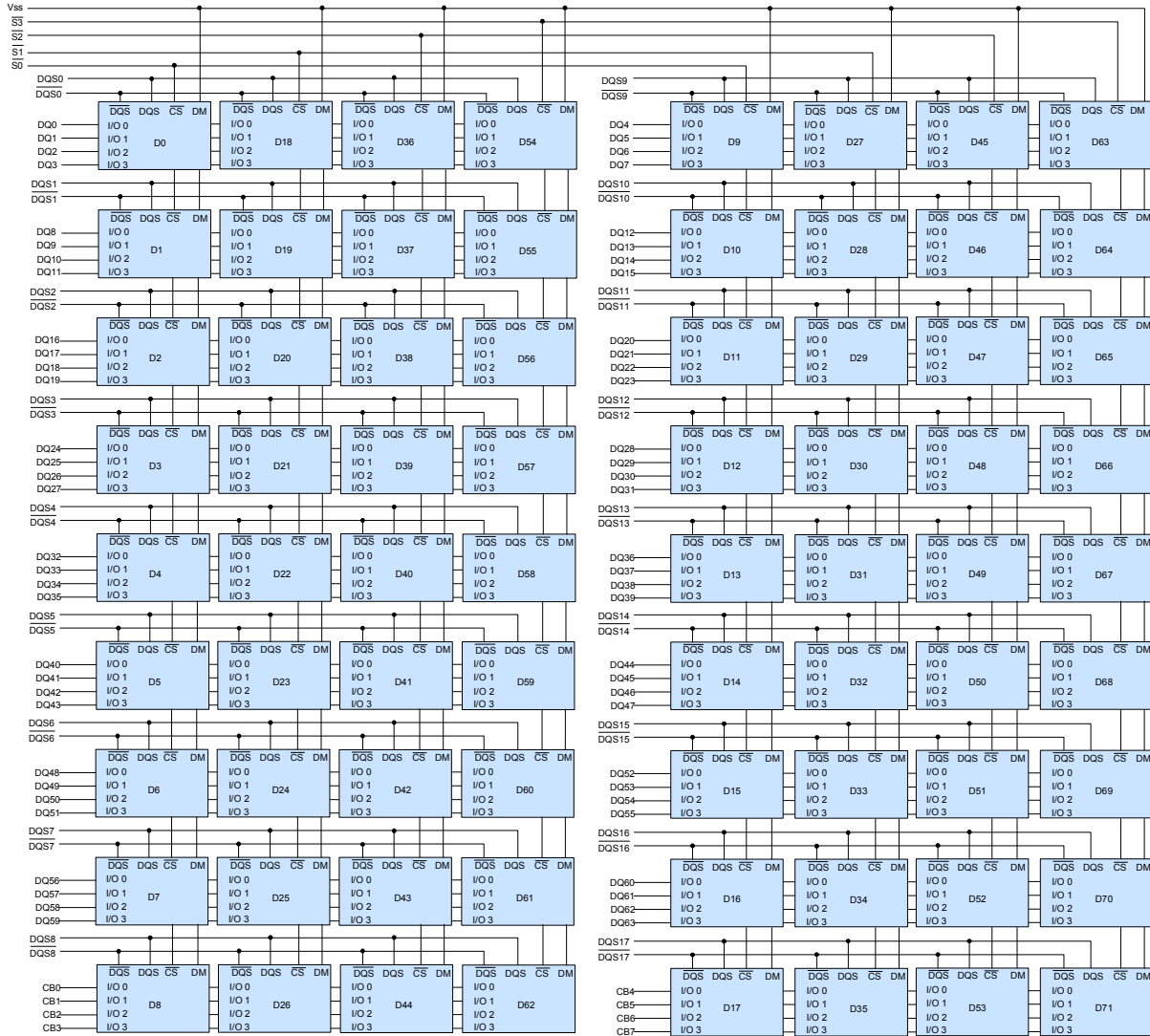
Functional Block Diagram (Part 2 of 2) (4GB, 4Rank, 128Mx8 DDR2 SDRAMs)



Notes :
 1. DQ-to-I/O wiring may be changed within a byte.
 2. There are two physical copies of each address/command/control/clock excluding CKE0/1, ODT0/1, CS.



Functional Block Diagram (8GB, 4Ranks, 512Mx4 DDR2 SDRAMs)



Note:
 1. DQ-to-I/O wiring may be changed within a nibble
 2. There are two physical copies of each address/command/control
 3. There are four physical copies of each clock



Absolute Maximum DC Ratings

| Symbol | Min | Typical | Max | Units | Notes |
|---|----------------------|---------------------|----------------------|-------|-------|
| DRAM V_{DD} / V_{DDQ} , AMB V_{DDQ} | 1.7 | 1.8 | 1.9 | V | |
| AMB V_{CC} / V_{CCFBD} | 1.46 | 1.5 | 1.54 | V | 1 |
| DRAM Interface V_{TT} | $0.48 \times V_{DD}$ | $0.5 \times V_{DD}$ | $0.52 \times V_{DD}$ | V | |
| V_{DDSPD} | 3.0 | 3.3 | 3.6 | V | |
| Note: 1. Estimate | | | | | |

Operating Temperature Range

| Symbol | Parameter | Min | Max | Units | Notes |
|--|--|-----|------|-------|-------|
| Tcase | DRAM Component Operating Temperature (Ambient) | 0 | +95 | °C | 1 |
| Tcase | AMB Component Operating Temperature (Ambient) | 0 | +110 | °C | |
| Note: 1. Within the DRAM Temperature range all DRAM will be support. | | | | | |

Electrical Characteristics and Operating Conditions

| Symbol | Parameter | Min | Max | Units | Notes |
|---|--|------------------------------|------------------------------|-------|-------|
| V_{DD} , V_{DDQ} | Supply Voltage, I/O Supply Voltage | 1.7 | 1.9 | V | 1 |
| V_{IH} (DC) | Input High (Logic1) Voltage | $V_{REF} + 0.125$ | $V_{DDQ} + 0.3$ | V | 1 |
| V_{IL} (DC) | Input Low (Logic0) Voltage | -0.3 | $V_{REF} - 0.125$ | V | 1 |
| V_{IH} (AC) | Input High (Logic1) Voltage | $V_{REF} + 0.2$ | - | V | |
| V_{IL} (AC) | Input Low (Logic0) Voltage | - | $V_{REF} - 0.2$ | V | |
| V_{ID} (AC) | AC differential input voltage | 0.5 | $V_{DDQ} + 0.6$ | V | |
| V_{IX} (AC) | AC Differential cross point input Voltage | $0.5 \times V_{DDQ} - 0.175$ | $0.5 \times V_{DDQ} + 0.175$ | V | |
| V_{OX} (AC) | AC Differential cross point output Voltage | $0.5 \times V_{DDQ} - 0.125$ | $0.5 \times V_{DDQ} + 0.125$ | V | |
| V_{SS} , V_{SSQ} | Supply Voltage, I/O Supply Voltage | 0 | 0 | V | |
| V_{REF} | I/O Reference Voltage | $0.49 \times V_{DDQ}$ | $0.51 \times V_{DDQ}$ | V | 1, 2 |
| V_{TT} | I/O Termination Voltage (System) | $V_{REF} - 0.04$ | $V_{REF} + 0.04$ | V | 1, 3 |
| Note: 1. Inputs are not recognized as valid until V_{REF} stabilizes. 2. V_{REF} is expected to be equal to $0.5 \times V_{DDQ}$ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value. 3. V_{TT} is not applied directly to the DIMM. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in the DC level of V_{REF} . | | | | | |



Serial Presence Detect (Part 1 of 2)

NT1GT72U89xxx-xx, 1 RANK Fully Buffered DDR2 SDRAM DIMM
 Based on 128Mx8, 8Banks, 8K Refresh, DDR2 SDRAMs with SPD

| Byte | Description | Serial PD Data Entry (Hexadecimal) | | | | |
|-------|--|---------------------------------------|---------|---------|---------|---------|
| | | D0BD-AC | D1BD-3C | D1BN-3C | D2BD-3C | D6BD-3C |
| 0 | Number of Serial PD Bytes in CRC | 92 | 92 | 92 | 92 | 92 |
| 1 | SPD Revision | 11 | 11 | 11 | 11 | 11 |
| 2 | Key Byte / DRAM Device Type | 09 | 09 | 09 | 09 | 09 |
| 3 | Voltage Levels of this Assembly | 12 | 12 | 12 | 12 | 12 |
| 4 | SDRAM Addressing | 45 | 45 | 45 | 45 | 45 |
| 5 | Module Physical Attributes | 24 | 24 | 24 | 24 | 24 |
| 6 | Modules Type | 07 | 07 | 07 | 07 | 07 |
| 7 | Module Organization | 09 | 09 | 09 | 09 | 09 |
| 8 | Fine Timebase Dividend and Divisor | 52 | 52 | 52 | 52 | 52 |
| 9 | Medium Timebase Dividend | 01 | 01 | 01 | 01 | 01 |
| 10 | Medium Timebase Divisor | 04 | 04 | 04 | 04 | 04 |
| 11 | SDRAM Minimum Cycle Time (tCKmin) | 0A | 0C | 0C | 0C | 0A |
| 12 | SDRAM Maximum Cycle Time (tCKmax) | 20 | 20 | 20 | 20 | 20 |
| 13 | SDRAM $\overline{\text{CAS}}$ Latencies Supported | 43 | 43 | 43 | 43 | 43 |
| 14 | SDRAM Minimum CAS Latency Time (tAA) | 32 | 3C | 3C | 3C | 32 |
| 15 | SDRAM Write Recovery Times Supported | 42 | 42 | 42 | 42 | 42 |
| 16 | SDRAM Write Recovery Time (tWR) | 3C | 3C | 3C | 3C | 3C |
| 17 | SDRAM Write Latencies Supported | 42 | 42 | 42 | 42 | 42 |
| 18 | SDRAM Additive Latencies Supported | 60 | 60 | 60 | 60 | 60 |
| 19 | SDRAM Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay (tRCD) | 32 | 3C | 3C | 3C | 32 |
| 20 | SDRAM Minimum Row Active to Row Active Delay (tRRD) | 1E | 1E | 1E | 1E | 1E |
| 21 | SDRAM Minimum Row Precharge Time (tRP) | 32 | 3C | 3C | 3C | 32 |
| 22 | SDRAM Upper Nibbles for tRAS and tRC | 00 | 00 | 00 | 00 | 00 |
| 23 | SDRAM Minimum Active to Precharge Time (tRAS) | B4 | B4 | B4 | B4 | B4 |
| 24 | SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Time (tRC) | E6 | F0 | F0 | F0 | E6 |
| 25~26 | SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC) | FE01 | FE01 | FE01 | FE01 | FE01 |
| 27 | SDRAM Internal Write to Read Command Delay (tWTR) | 1E | 1E | 1E | 1E | 1E |
| 28 | SDRAM Internal Read to Precharge Command Delay (tRTP) | 1E | 1E | 1E | 1E | 1E |
| 29 | SDRAM Burst Lengths Supported | 03 | 03 | 03 | 03 | 03 |
| 30 | SDRAM Terminations Supported | 07 | 07 | 07 | 07 | 07 |
| 31 | SDRAM Drivers Supported | 01 | 01 | 01 | 01 | 01 |
| 32 | SDRAM Average Refresh Interval (tREFI)/Double Refresh mode bit/High Temperature self-refresh rate support indication | C2 | C2 | C2 | C2 | C2 |
| 33 | Tcasemax | 00 | 00 | 00 | 00 | 00 |
| 34 | Thermal resistance of SDRAM device package from top (case0 to ambient) (Psi T-A SDRAM) | 00 | 00 | 00 | 00 | 00 |

Serial Presence Detect (Part 2 of 2)

NT1GT72U89xxx-xx, 1 RANK Fully Buffered DDR2 SDRAM DIMM

REV 1.3

03/2009

NT1GT72U89D0BD-AC / NT2GT72U8PD0BD-AC / NT4GT72U4ND0BD-AC / NT4GT72U8ND9BD-AC
 NT1GT72U89D1BD-3C / NT2GT72U8PD1BD-3C / NT4GT72U4ND1BD-3C / NT8GTT72U4ND3YD-3C
 NT1GT72U89D1BN-3C / NT2GT72U8PD1BN-3C / NT4GT72U4ND1BN-3C / NT8GTT72U4ND4YD-3C
 NT1GT72U89D2BD-3C / NT2GT72U8PD2BD-3C / NT4GT72U4ND2BD-3C / NT8GTT72U4ND5YD-3C
 NT1GT72U89D6BD-AC / NT2GT72U8PD6BD-AC / NT4GT72U8ND9BD-3C



Based on 128Mx8, 8Banks, 8K Refresh, DDR2 SDRAMs with SPD

| Byte | Description | Serial PD Data Entry (Hexadecimal) | | | | |
|---------|--|---------------------------------------|---------|---------|---------|---------|
| | | D0BD-AC | D1BD-3C | D1BN-3C | D2BD-3C | D6BD-3C |
| 35-41 | Delta Temperature | -- | -- | -- | -- | -- |
| 42-80 | Reserved | -- | -- | -- | -- | -- |
| 81~82 | FB-DIMM Channel Protocols Supported | 0200 | 0200 | 0200 | 0200 | 0200 |
| 83 | Additional Back to Back Access Turnaround Time | 10 | 10 | 10 | 10 | 10 |
| 84 | AMB Read Access Time for DDR2-800 | 36 | 36 | 56 | 4A | 36 |
| 85 | AMB Read Access Time for DDR2-667 | 34 | 34 | 40 | 46 | 34 |
| 86 | AMB Read Access Time for DDR2-533 | 32 | 32 | 36 | 38 | 32 |
| 87 | Thermal Resistance of AMB Package from top (case) to ambient (Psi T-A SDRAM) at still air condition. | 2A | 2A | 30 | 2A | 2A |
| 88 | AMB DT Idle_0 | 5D | 56 | 60 | 33 | 5D |
| 89 | AMB DT Idle_1 | 71 | 6B | 7A | 40 | 71 |
| 90 | AMB DT Idle_2 | 65 | 5C | 6E | 37 | 65 |
| 91 | AMB DT Active_1 | 9B | 91 | A1 | 57 | 9B |
| 92 | AMB DT Active_2 | 7F | 76 | 7F | 46 | 7F |
| 93 | AMB DT L0s | 00 | 00 | 00 | 00 | 00 |
| 94~114 | Reserved | -- | -- | -- | -- | -- |
| 115~116 | AMB Manufacturer ID Code | 7FB3 | 7FB3 | 8089 | 7FB3 | 7FB3 |
| 117-118 | Module ID: Module Manufacture's JEDEC ID Code | 830B | 830B | 830B | 830B | 830B |
| 119-125 | Reserved for Module ID | -- | -- | -- | -- | -- |
| 126-127 | Cyclical Redundancy Code | -- | -- | -- | -- | -- |
| 128-145 | Module Part Number | -- | -- | -- | -- | -- |
| 146-147 | Module Revision Code | -- | -- | -- | -- | -- |
| 148-149 | SDRAM Manufacture's JEDEC ID Code | 830B | 830B | 830B | 830B | 830B |
| 150-255 | Reserved | -- | -- | -- | -- | -- |



Serial Presence Detect (Part 1 of 2)

NT2GT72U8Pxxxx-xx, 2 RANK Fully Buffered DDR2 SDRAM DIMM

Based on 128Mx8, 8Banks, 8K Refresh, DDR2 SDRAMs with SPD

| Byte | Description | Serial PD Data Entry (Hexadecimal) | | | | |
|-------|--|---------------------------------------|---------|---------|---------|---------|
| | | D0BD-AC | D1BD-3C | D1BN-3C | D2BD-3C | D6BD-3C |
| 0 | Number of Serial PD Bytes in CRC | 92 | 92 | 92 | 92 | 92 |
| 1 | SPD Revision | 11 | 11 | 11 | 11 | 11 |
| 2 | Key Byte / DRAM Device Type | 09 | 09 | 09 | 09 | 09 |
| 3 | Voltage Levels of this Assembly | 12 | 12 | 12 | 12 | 12 |
| 4 | SDRAM Addressing | 45 | 45 | 45 | 45 | 45 |
| 5 | Module Physical Attributes | 24 | 24 | 24 | 24 | 24 |
| 6 | Modules Type | 07 | 07 | 07 | 07 | 07 |
| 7 | Module Organization | 11 | 11 | 11 | 11 | 11 |
| 8 | Fine Timebase Dividend and Divisor | 52 | 52 | 52 | 52 | 52 |
| 9 | Medium Timebase Dividend | 01 | 01 | 01 | 01 | 01 |
| 10 | Medium Timebase Divisor | 04 | 04 | 04 | 04 | 04 |
| 11 | SDRAM Minimum Cycle Time (tCKmin) | 0A | 0C | 0C | 0C | 0A |
| 12 | SDRAM Maximum Cycle Time (tCKmax) | 20 | 20 | 20 | 20 | 20 |
| 13 | SDRAM $\overline{\text{CAS}}$ Latencies Supported | 43 | 43 | 43 | 43 | 43 |
| 14 | SDRAM Minimum CAS Latency Time (tAA) | 32 | 3C | 3C | 3C | 32 |
| 15 | SDRAM Write Recovery Times Supported | 42 | 42 | 42 | 42 | 42 |
| 16 | SDRAM Write Recovery Time (tWR) | 3C | 3C | 3C | 3C | 3C |
| 17 | SDRAM Write Latencies Supported | 42 | 42 | 42 | 42 | 42 |
| 18 | SDRAM Additive Latencies Supported | 60 | 60 | 60 | 60 | 60 |
| 19 | SDRAM Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay (tRCD) | 32 | 3C | 3C | 3C | 32 |
| 20 | SDRAM Minimum Row Active to Row Active Delay (tRRD) | 1E | 1E | 1E | 1E | 1E |
| 21 | SDRAM Minimum Row Precharge Time (tRP) | 32 | 3C | 3C | 3C | 32 |
| 22 | SDRAM Upper Nibbles for tRAS and tRC | 00 | 00 | 00 | 00 | 00 |
| 23 | SDRAM Minimum Active to Precharge Time (tRAS) | B4 | B4 | B4 | B4 | B4 |
| 24 | SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Time (tRC) | E6 | F0 | F0 | F0 | E6 |
| 25~26 | SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC) | FE01 | FE01 | FE01 | FE01 | FE01 |
| 27 | SDRAM Internal Write to Read Command Delay (tWTR) | 1E | 1E | 1E | 1E | 1E |
| 28 | SDRAM Internal Read to Precharge Command Delay (tRTP) | 1E | 1E | 1E | 1E | 1E |
| 29 | SDRAM Burst Lengths Supported | 03 | 03 | 03 | 03 | 03 |
| 30 | SDRAM Terminations Supported | 07 | 07 | 07 | 07 | 07 |
| 31 | SDRAM Drivers Supported | 01 | 01 | 01 | 01 | 01 |
| 32 | SDRAM Average Refresh Interval (tREFI)/Double Refresh mode bit/High Temperature self-refresh rate support indication | C2 | C2 | C2 | C2 | C2 |
| 33 | Tcasemax | 00 | 00 | 00 | 00 | 00 |
| 34 | Thermal resistance of SDRAM device package from top (case0 to ambient) (Psi T-A SDRAM) | 00 | 00 | 00 | 00 | 00 |

NT1GT72U89D0BD-AC / NT2GT72U8PD0BD-AC / NT4GT72U4ND0BD-AC / NT4GT72U8ND9BD-AC
 NT1GT72U89D1BD-3C / NT2GT72U8PD1BD-3C / NT4GT72U4ND1BD-3C / NT8GTT72U4ND3YD-3C
 NT1GT72U89D1BN-3C / NT2GT72U8PD1BN-3C / NT4GT72U4ND1BN-3C / NT8GTT72U4ND4YD-3C
 NT1GT72U89D2BD-3C / NT2GT72U8PD2BD-3C / NT4GT72U4ND2BD-3C / NT8GTT72U4ND5YD-3C
 NT1GT72U89D6BD-AC / NT2GT72U8PD6BD-AC / NT4GT72U8ND9BD-3C



Serial Presence Detect (Part 2 of 2)

NT2GT72U8Pxxxx-xx, 2 RANK Fully Buffered DDR2 SDRAM DIMM

Based on 128Mx8, 8Banks, 8K Refresh, DDR2 SDRAMs with SPD

| Byte | Description | Serial PD Data Entry (Hexadecimal) | | | | |
|---------|--|---------------------------------------|---------|---------|---------|---------|
| | | D0BD-AC | D1BD-3C | D1BN-3C | D2BD-3C | D6BD-3C |
| 35-41 | Delta Temperature | -- | -- | -- | -- | -- |
| 42-80 | Reserved | -- | -- | -- | -- | -- |
| 81~82 | FB-DIMM Channel Protocols Supported | 0200 | 0200 | 0200 | 0200 | 0200 |
| 83 | Additional Back to Back Access Turnaround Time | 10 | 10 | 10 | 10 | 10 |
| 84 | AMB Read Access Time for DDR2-800 | 36 | 36 | 56 | 4A | 36 |
| 85 | AMB Read Access Time for DDR2-667 | 34 | 34 | 40 | 46 | 34 |
| 86 | AMB Read Access Time for DDR2-533 | 32 | 32 | 36 | 38 | 32 |
| 87 | Thermal Resistance of AMB Package from top (case) to ambient (Psi T-A SDRAM) at still air condition. | 2A | 2A | 30 | 2A | 2A |
| 88 | AMB DT Idle_0 | 5D | 56 | 60 | 33 | 5D |
| 89 | AMB DT Idle_1 | 71 | 6B | 7A | 40 | 71 |
| 90 | AMB DT Idle_2 | 65 | 5C | 6E | 37 | 65 |
| 91 | AMB DT Active_1 | 9B | 91 | A1 | 57 | 9B |
| 92 | AMB DT Active_2 | 7F | 76 | 7F | 46 | 7F |
| 93 | AMB DT L0s | 00 | 00 | 00 | 00 | 00 |
| 94~114 | Reserved | -- | -- | -- | -- | -- |
| 115~116 | AMB Manufacturer ID Code | 7FB3 | 7FB3 | 8089 | 7FB3 | 7FB3 |
| 117-118 | Module ID: Module Manufacture's JEDEC ID Code | 830B | 830B | 830B | 830B | 830B |
| 119-125 | Reserved for Module ID | -- | -- | -- | -- | -- |
| 126-127 | Cyclical Redundancy Code | -- | -- | -- | -- | -- |
| 128-145 | Module Part Number | -- | -- | -- | -- | -- |
| 146-147 | Module Revision Code | -- | -- | -- | -- | -- |
| 148-149 | SDRAM Manufacture's JEDEC ID Code | 830B | 830B | 830B | 830B | 830B |
| 150-255 | Reserved | -- | -- | -- | -- | -- |



Serial Presence Detect (Part 1 of 2)

NT4GT72U4Nxxx-xx, 2 RANK Fully Buffered DDR2 SDRAM DIMM

Based on 256Mx4, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

| Byte | Description | Serial PD Data Entry (Hexadecimal) | | | |
|-------|--|---------------------------------------|---------|---------|---------|
| | | D0BD-AC | D1BD-3C | D1BN-3C | D2BD-3C |
| 0 | Number of Serial PD Bytes in CRC | 92 | 92 | 92 | 92 |
| 1 | SPD Revision | 11 | 11 | 11 | 11 |
| 2 | Key Byte / DRAM Device Type | 09 | 09 | 09 | 09 |
| 3 | Voltage Levels of this Assembly | 12 | 12 | 12 | 12 |
| 4 | SDRAM Addressing | 49 | 49 | 49 | 49 |
| 5 | Module Physical Attributes | 24 | 24 | 24 | 24 |
| 6 | Modules Type | 07 | 07 | 07 | 07 |
| 7 | Module Organization | 10 | 10 | 10 | 10 |
| 8 | Fine Timebase Dividend and Divisor | 52 | 52 | 52 | 52 |
| 9 | Medium Timebase Dividend | 01 | 01 | 01 | 01 |
| 10 | Medium Timebase Divisor | 04 | 04 | 04 | 04 |
| 11 | SDRAM Minimum Cycle Time (tCKmin) | 0A | 0C | 0C | 0C |
| 12 | SDRAM Maximum Cycle Time (tCKmax) | 20 | 20 | 20 | 20 |
| 13 | SDRAM $\overline{\text{CAS}}$ Latencies Supported | 43 | 43 | 43 | 43 |
| 14 | SDRAM Minimum CAS Latency Time (tAA) | 3C | 3C | 3C | 3C |
| 15 | SDRAM Write Recovery Times Supported | 42 | 42 | 42 | 42 |
| 16 | SDRAM Write Recovery Time (tWR) | 3C | 3C | 3C | 3C |
| 17 | SDRAM Write Latencies Supported | 42 | 42 | 42 | 42 |
| 18 | SDRAM Additive Latencies Supported | 60 | 60 | 60 | 60 |
| 19 | SDRAM Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay (tRCD) | 3C | 3C | 3C | 3C |
| 20 | SDRAM Minimum Row Active to Row Active Delay (tRRD) | 1E | 1E | 1E | 1E |
| 21 | SDRAM Minimum Row Precharge Time (tRP) | 3C | 3C | 3C | 3C |
| 22 | SDRAM Upper Nibbles for tRAS and tRC | 00 | 00 | 00 | 00 |
| 23 | SDRAM Minimum Active to Precharge Time (tRAS) | B4 | B4 | B4 | B4 |
| 24 | SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Time (tRC) | F0 | F0 | F0 | F0 |
| 25~26 | SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC) | FE01 | FE01 | FE01 | FE01 |
| 27 | SDRAM Internal Write to Read Command Delay (tWTR) | 1E | 1E | 1E | 1E |
| 28 | SDRAM Internal Read to Precharge Command Delay (tRTP) | 1E | 1E | 1E | 1E |
| 29 | SDRAM Burst Lengths Supported | 03 | 03 | 03 | 03 |
| 30 | SDRAM Terminations Supported | 07 | 07 | 07 | 07 |
| 31 | SDRAM Drivers Supported | 01 | 01 | 01 | 01 |
| 32 | SDRAM Average Refresh Interval (tREFI)/Double Refresh mode bit/High Temperature self-refresh rate support indication | C2 | C2 | C2 | C2 |
| 33 | Tcasemax | 00 | 00 | 00 | 00 |
| 34 | Thermal resistance of SDRAM device package from top (case0 to ambient (Psi T-A SDRAM) | 00 | 00 | 00 | 00 |



Serial Presence Detect (Part 2 of 2)

NT4GT72U4Nxxx-xx, 2 RANK Fully Buffered DDR2 SDRAM DIMM

Based on 256Mx4, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

| Byte | Description | Serial PD Data Entry (Hexadecimal) | | | |
|---------|--|---------------------------------------|---------|---------|---------|
| | | D0BD-AC | D1BD-3C | D1BN-3C | D2BD-3C |
| 35-41 | Delta Temperature | -- | -- | -- | -- |
| 42-80 | Reserved | -- | -- | -- | -- |
| 81~82 | FB-DIMM Channel Protocols Supported | 0200 | 0200 | 0200 | 0200 |
| 83 | Additional Back to Back Access Turnaround Time | 10 | 10 | 10 | 10 |
| 84 | AMB Read Access Time for DDR2-800 | 36 | 36 | 56 | 4A |
| 85 | AMB Read Access Time for DDR2-667 | 34 | 34 | 40 | 46 |
| 86 | AMB Read Access Time for DDR2-533 | 32 | 32 | 36 | 38 |
| 87 | Thermal Resistance of AMB Package from top (case) to ambient (Psi T-A SDRAM) at still air condition. | 2A | 2A | 30 | 2A |
| 88 | AMB DT Idle_0 | 64 | 56 | 60 | 38 |
| 89 | AMB DT Idle_1 | 7B | 6B | 7A | 45 |
| 90 | AMB DT Idle_2 | 65 | 5C | 6E | 37 |
| 91 | AMB DT Active_1 | A3 | 91 | A1 | 5D |
| 92 | AMB DT Active_2 | 87 | 76 | 7F | 4C |
| 93 | AMB DT L0s | 00 | 00 | 00 | 00 |
| 94~114 | Reserved | -- | -- | -- | -- |
| 115~116 | AMB Manufacturer ID Code | 7FB3 | 7FB3 | 8089 | 7FB3 |
| 117-118 | Module ID: Module Manufacture's JEDEC ID Code | 830B | 830B | 830B | 830B |
| 119-125 | Reserved for Module ID | -- | -- | -- | -- |
| 126-127 | Cyclical Redundancy Code | -- | -- | -- | -- |
| 128-145 | Module Part Number | -- | -- | -- | -- |
| 146-147 | Module Revision Code | -- | -- | -- | -- |
| 148-149 | SDRAM Manufacture's JEDEC ID Code | 830B | 830B | 830B | 830B |
| 150-255 | Reserved | -- | -- | -- | -- |



Serial Presence Detect (Part 1 of 2)

NT4GTT72U8Nxxx-xx, 4 RANK Fully Buffered DDR2 SDRAM DIMM

Based on 128Mx8, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

| Byte | Description | Serial PD Data Entry (Hexadecimal) | |
|-------|--|------------------------------------|---------|
| | | D9BD-3C | D9BD-AC |
| 0 | Number of Serial PD Bytes in CRC | 92 | 92 |
| 1 | SPD Revision | 11 | 11 |
| 2 | Key Byte / DRAM Device Type | 09 | 09 |
| 3 | Voltage Levels of this Assembly | 12 | 12 |
| 4 | SDRAM Addressing | 45 | 45 |
| 5 | Module Physical Attributes | 24 | 24 |
| 6 | Modules Type | 07 | 07 |
| 7 | Module Organization | 21 | 21 |
| 8 | Fine Timebase Dividend and Divisor | 52 | 52 |
| 9 | Medium Timebase Dividend | 01 | 01 |
| 10 | Medium Timebase Divisor | 04 | 04 |
| 11 | SDRAM Minimum Cycle Time (tCKmin) | 0C | 0A |
| 12 | SDRAM Maximum Cycle Time (tCKmax) | 20 | 20 |
| 13 | SDRAM CAS Latencies Supported | 43 | 43 |
| 14 | SDRAM Minimum CAS Latency Time (tAA) | 3C | 3C |
| 15 | SDRAM Write Recovery Times Supported | 42 | 42 |
| 16 | SDRAM Write Recovery Time (tWR) | 3C | 3C |
| 17 | SDRAM Write Latencies Supported | 42 | 42 |
| 18 | SDRAM Additive Latencies Supported | 60 | 60 |
| 19 | SDRAM Minimum RAS to CAS Delay (tRCD) | 3C | 32 |
| 20 | SDRAM Minimum Row Active to Row Active Delay (tRRD) | 1E | 1E |
| 21 | SDRAM Minimum Row Precharge Time (tRP) | 3C | 32 |
| 22 | SDRAM Upper Nibbles for tRAS and tRC | 00 | 00 |
| 23 | SDRAM Minimum Active to Precharge Time (tRAS) | B4 | B4 |
| 24 | SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Time (tRC) | F0 | E6 |
| 25-26 | SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC) | FE01 | FE01 |
| 27 | SDRAM Internal Write to Read Command Delay (tWTR) | 1E | 1E |
| 28 | SDRAM Internal Read to Precharge Command Delay (tRTP) | 1E | 1E |
| 29 | SDRAM Burst Lengths Supported | 03 | 03 |
| 30 | SDRAM Terminations Supported | 07 | 07 |
| 31 | SDRAM Drivers Supported | 01 | 01 |
| 32 | SDRAM Average Refresh Interval (tREFI)/Double Refresh mode bit/High Temperature self-refresh rate support indication | C2 | C2 |
| 33 | Tcasemax | 00 | 00 |
| 34 | Thermal resistance of SDRAM device package from top (case0 to ambient (Psi T-A SDRAM)) | 00 | 00 |

NT1GT72U89D0BD-AC / NT2GT72U8PD0BD-AC / NT4GT72U4ND0BD-AC / NT4GT72U8ND9BD-AC
 NT1GT72U89D1BD-3C / NT2GT72U8PD1BD-3C / NT4GT72U4ND1BD-3C / NT8GTT72U4ND3YD-3C
 NT1GT72U89D1BN-3C / NT2GT72U8PD1BN-3C / NT4GT72U4ND1BN-3C / NT8GTT72U4ND4YD-3C
 NT1GT72U89D2BD-3C / NT2GT72U8PD2BD-3C / NT4GT72U4ND2BD-3C / NT8GTT72U4ND5YD-3C
 NT1GT72U89D6BD-AC / NT2GT72U8PD6BD-AC / NT4GT72U8ND9BD-3C



Serial Presence Detect (Part 2 of 2)

NT4GTT72U8Nxxx-xx, 4 RANK Fully Buffered DDR2 SDRAM DIMM

Based on 128Mx8, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

| Byte | Description | Serial PD Data Entry (Hexadecimal) | |
|---------|--|---------------------------------------|---------|
| | | D9BD-3C | D9BD-AC |
| 35-41 | Delta Temperature | -- | -- |
| 42-80 | Reserved | -- | -- |
| 81~82 | FB-DIMM Channel Protocols Supported | 0200 | 0200 |
| 83 | Additional Back to Back Access Turnaround Time | 10 | 10 |
| 84 | AMB Read Access Time for DDR2-800 | 4A | 4A |
| 85 | AMB Read Access Time for DDR2-667 | 46 | 46 |
| 86 | AMB Read Access Time for DDR2-533 | 38 | 38 |
| 87 | Thermal Resistance of AMB Package from top (case) to ambient (Psi T-A SDRAM) at still air condition. | 2A | 2A |
| 88 | AMB DT Idle_0 | 3A | 3E |
| 89 | AMB DT Idle_1 | 47 | 4B |
| 90 | AMB DT Idle_2 | 3A | 40 |
| 91 | AMB DT Active_1 | 5F | 64 |
| 92 | AMB DT Active_2 | 4F | 53 |
| 93 | AMB DT L0s | 00 | 00 |
| 94~114 | Reserved | -- | -- |
| 115~116 | AMB Manufacturer ID Code | 7FB3 | 7FB3 |
| 117-118 | Module ID: Module Manufacture's JEDEC ID Code | 830B | 830B |
| 119-125 | Reserved for Module ID | -- | -- |
| 126-127 | Cyclical Redundancy Code | -- | -- |
| 128-145 | Module Part Number | -- | -- |
| 146-147 | Module Revision Code | -- | -- |
| 148-149 | SDRAM Manufacture's JEDEC ID Code | 830B | 830B |
| 150-255 | Reserved | -- | -- |



Serial Presence Detect (Part 1 of 2)

NT8GTT72U4Nxxx-xx, 4 RANK Fully Buffered DDR2 SDRAM DIMM

Based on 512Mx4, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

| Byte | Description | Serial PD Data Entry (Hexadecimal) | | |
|-------|--|---------------------------------------|---------|---------|
| | | D3YD-3C | D4YD-3C | D5YD-3C |
| 0 | Number of Serial PD Bytes in CRC | 92 | 92 | 92 |
| 1 | SPD Revision | 11 | 11 | 11 |
| 2 | Key Byte / DRAM Device Type | 09 | 09 | 09 |
| 3 | Voltage Levels of this Assembly | 12 | 12 | 12 |
| 4 | SDRAM Addressing | 49 | 49 | 49 |
| 5 | Module Physical Attributes | 24 | 24 | 24 |
| 6 | Modules Type | 07 | 07 | 07 |
| 7 | Module Organization | 20 | 20 | 20 |
| 8 | Fine Timebase Dividend and Divisor | 52 | 52 | 52 |
| 9 | Medium Timebase Dividend | 01 | 01 | 01 |
| 10 | Medium Timebase Divisor | 04 | 04 | 04 |
| 11 | SDRAM Minimum Cycle Time (tCKmin) | 0C | 0C | 0C |
| 12 | SDRAM Maximum Cycle Time (tCKmax) | 20 | 20 | 20 |
| 13 | SDRAM CAS Latencies Supported | 43 | 43 | 43 |
| 14 | SDRAM Minimum CAS Latency Time (tAA) | 3C | 3C | 3C |
| 15 | SDRAM Write Recovery Times Supported | 42 | 42 | 42 |
| 16 | SDRAM Write Recovery Time (tWR) | 3C | 3C | 3C |
| 17 | SDRAM Write Latencies Supported | 42 | 42 | 42 |
| 18 | SDRAM Additive Latencies Supported | 40 | 40 | 40 |
| 19 | SDRAM Minimum RAS to CAS Delay (tRCD) | 3C | 3C | 3C |
| 20 | SDRAM Minimum Row Active to Row Active Delay (tRRD) | 1E | 1E | 1E |
| 21 | SDRAM Minimum Row Precharge Time (tRP) | 3C | 3C | 3C |
| 22 | SDRAM Upper Nibbles for tRAS and tRC | 00 | 00 | 00 |
| 23 | SDRAM Minimum Active to Precharge Time (tRAS) | B4 | B4 | B4 |
| 24 | SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Time (tRC) | F0 | F0 | F0 |
| 25-26 | SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC) | FE01 | FE01 | FE01 |
| 27 | SDRAM Internal Write to Read Command Delay (tWTR) | 1E | 1E | 1E |
| 28 | SDRAM Internal Read to Precharge Command Delay (tRTP) | 1E | 1E | 1E |
| 29 | SDRAM Burst Lengths Supported | 03 | 03 | 03 |
| 30 | SDRAM Terminations Supported | 07 | 07 | 07 |
| 31 | SDRAM Drivers Supported | 01 | 01 | 01 |
| 32 | SDRAM Average Refresh Interval (tREFI)/Double Refresh mode bit/High Temperature self-refresh rate support indication | C2 | C2 | C2 |
| 33 | Tcasemax | 00 | 00 | 00 |
| 34 | Thermal resistance of SDRAM device package from top (case0 to ambient (Psi T-A SDRAM)) | 00 | 00 | 00 |



Serial Presence Detect (Part 2 of 2)

NT8GTT72U4Nxxx-xx, 4 RANK Fully Buffered DDR2 SDRAM DIMM

Based on 512Mx4, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

| Byte | Description | Serial PD Data Entry (Hexadecimal) | | |
|---------|--|---------------------------------------|---------|---------|
| | | D3YD-3C | D4YD-3C | D5YD-3C |
| 35-41 | Delta Temperature | -- | -- | -- |
| 42-80 | Reserved | -- | -- | -- |
| 81~82 | FB-DIMM Channel Protocols Supported | 0200 | 0200 | 0200 |
| 83 | Additional Back to Back Access Turnaround Time | 10 | 10 | 10 |
| 84 | AMB Read Access Time for DDR2-800 | 36 | 36 | 4A |
| 85 | AMB Read Access Time for DDR2-667 | 34 | 34 | 46 |
| 86 | AMB Read Access Time for DDR2-533 | 32 | 32 | 38 |
| 87 | Thermal Resistance of AMB Package from top (case) to ambient (Psi T-A SDRAM) at still air condition. | 2A | 2A | 2A |
| 88 | AMB DT Idle_0 | 62 | 62 | 3A |
| 89 | AMB DT Idle_1 | 77 | 77 | 47 |
| 90 | AMB DT Idle_2 | 61 | 61 | 3A |
| 91 | AMB DT Active_1 | 9F | 9F | 5F |
| 92 | AMB DT Active_2 | 84 | 84 | 4F |
| 93 | AMB DT L0s | 00 | 00 | 00 |
| 94~114 | Reserved | -- | -- | -- |
| 115~116 | AMB Manufacturer ID Code | 7FB3 | 7FB3 | 7FB3 |
| 117-118 | Module ID: Module Manufacture's JEDEC ID Code | 830B | 830B | 830B |
| 119-125 | Reserved for Module ID | -- | -- | -- |
| 126-127 | Cyclical Redundancy Code | -- | -- | -- |
| 128-145 | Module Part Number | -- | -- | -- |
| 146-147 | Module Revision Code | -- | -- | -- |
| 148-149 | SDRAM Manufacture's JEDEC ID Code | 830B | 830B | 830B |
| 150-255 | Reserved | -- | -- | -- |

NT1GT72U89D0BD-AC / NT2GT72U8PD0BD-AC / NT4GT72U4ND0BD-AC / NT4GT72U8ND9BD-AC
 NT1GT72U89D1BD-3C / NT2GT72U8PD1BD-3C / NT4GT72U4ND1BD-3C / NT8GTT72U4ND3YD-3C
 NT1GT72U89D1BN-3C / NT2GT72U8PD1BN-3C / NT4GT72U4ND1BN-3C / NT8GTT72U4ND4YD-3C
 NT1GT72U89D2BD-3C / NT2GT72U8PD2BD-3C / NT4GT72U4ND2BD-3C / NT8GTT72U4ND5YD-3C
 NT1GT72U89D6BD-AC / NT2GT72U8PD6BD-AC / NT4GT72U8ND9BD-3C



Environmental Requirements

| Symbol | Parameter | Rating | Units | Note |
|------------------|---|-------------|----------|------|
| T _{OPR} | Operating temperature | - | | 1 |
| H _{OPR} | Operating humidity (relative) | 10 to 90 | % | 2 |
| T _{STG} | Storage temperature | -50 to +100 | °C | 2 |
| H _{STG} | Storage humidity (without condensation) | 5 to 95 | % | 2 |
| P _{BAR} | Barometric pressure (operating & Storage) | 105 to 69 | K pascal | 2 |

Note:

1. The designer must meet the case temperature specifications for individual module components.
2. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



Operating, Standby, and Refresh Currents Definition table

| Symbol | Parameter/Condition |
|---|---|
| Idd_Idle_0 Icc_Idle_0 | Idle Current, single or last DIMM. L0 state, idle (0BW). Primary channel enabled; Secondary Channel disabled. CKE high. Command and address line stable. DRAM clock active. |
| Idd_Idle_1 Icc_Idle_1 | Idle Current, first DIMM. L0 stage, idle (0BW). Primary and Secondary channels enabled. CKE high. Command and address line stable. DRAM clock active. |
| Idd_Idle_2 Icc_Idle_2 | Idle Current, DRAM power down. L0 stage, idle (0BW). Primary and Secondary channels enabled CKE low. Command and address lines floated. DRAM clock active, ODT and CKE driven low. |
| Idd_Active_1 Icc_Active_1 (Write) | Active Power. L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high. |
| Idd_Active_1 Icc_Active_1 (Read) | Active Power. L0 state. 50% DRAM BW to downstream DIMM, 100% read. Primary and Secondary channels enabled. DRAM clock active, CKE high. |
| Idd_Active_2 Icc_Active_2 | Active Power, data pass through. L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled. CKE high. Command and address lines stable. DRAM clock active. |
| Idd_Training Icc_Training | Primary and Secondary channels enabled. 100% toggle on all channel lanes. DRAMs idle. 0BW. CKE high, Command and address line stable. DRAM clock active. |

| Part Number | Idle_0 | | Idle_1 | | Idle_2 | | Active_1 (W) | | Active_1 (R) | | Active_2 | | Training | | Unit |
|--------------------|--------|------|--------|------|--------|------|--------------|------|--------------|------|----------|------|----------|------|------|
| | Idd | Icc | Idd | Icc | Idd | Icc | Idd | Icc | Idd | Icc | Idd | Icc | Idd | Icc | |
| NT1GT72U89D0BD-AC | 0.96 | 3.39 | 0.97 | 4.16 | 0.97 | 4.16 | 0.99 | 4.18 | 0.99 | 4.18 | 0.97 | 4.18 | 0.94 | 3.96 | A |
| NT1GT72U89D6BD-AC | 0.96 | 3.39 | 0.97 | 4.16 | 0.97 | 4.16 | 0.99 | 4.18 | 0.99 | 4.18 | 0.97 | 4.18 | 0.94 | 3.96 | A |
| NT1GT72U89D1BD-3C | 0.91 | 2.86 | 0.91 | 2.92 | 0.88 | 3.76 | 0.92 | 3.75 | 0.94 | 3.74 | 0.88 | 3.74 | 0.90 | 3.41 | A |
| NT1GT72U89D2BD-3C | 0.77 | 1.85 | 0.77 | 2.37 | 0.79 | 2.37 | 0.77 | 2.35 | 0.77 | 2.37 | 0.77 | 2.42 | 0.77 | 2.33 | A |
| NT1GT72U89D1BN-3C | 0.77 | 2.64 | 0.77 | 3.87 | 0.77 | 3.87 | 0.94 | 4.20 | 0.99 | 4.22 | 0.99 | 4.13 | 0.88 | 3.87 | A |
| NT2GT72U8PD0BD-AC | 1.34 | 3.34 | 1.35 | 4.04 | 1.35 | 4.05 | 1.43 | 4.20 | 1.33 | 4.19 | 1.98 | 4.09 | 1.98 | 3.92 | A |
| NT2GT72U8PD6BD-AC | 1.34 | 3.34 | 1.35 | 4.04 | 1.35 | 4.05 | 1.43 | 4.20 | 1.33 | 4.19 | 1.98 | 4.09 | 1.98 | 3.92 | A |
| NT2GT72U8PD1BD-3C | 1.30 | 2.51 | 1.30 | 3.55 | 1.31 | 3.72 | 1.30 | 3.72 | 1.30 | 3.72 | 2.09 | 3.72 | 1.99 | 3.47 | A |
| NT2GT72U8PD2BD-3C | 1.16 | 1.89 | 1.16 | 2.40 | 1.18 | 2.42 | 1.16 | 2.42 | 1.16 | 2.43 | 1.13 | 2.42 | 1.16 | 2.37 | A |
| NT2GT72U8PD1BN-3C | 1.10 | 2.67 | 1.11 | 3.93 | 1.11 | 3.94 | 1.25 | 4.18 | 1.25 | 4.27 | 1.25 | 4.19 | 1.24 | 3.96 | A |
| NT4GT72U4ND0BD-AC | 2.28 | 2.85 | 2.31 | 4.03 | 2.32 | 4.02 | 2.39 | 4.27 | 2.41 | 4.28 | 2.31 | 4.28 | 2.34 | 3.93 | A |
| NT4GT72U4ND1BD-3C | 2.09 | 2.86 | 2.11 | 3.63 | 2.15 | 3.74 | 2.23 | 3.76 | 2.21 | 3.77 | 2.21 | 3.76 | 2.11 | 3.52 | A |
| NT4GT72U4ND2BD-3C | 2.04 | 1.90 | 2.04 | 2.42 | 2.10 | 2.44 | 2.11 | 2.45 | 2.11 | 2.45 | 2.01 | 2.44 | 2.01 | 2.40 | A |
| NT4GT72U4ND1BN-3C | 1.93 | 2.70 | 1.93 | 4.10 | 2.50 | 4.22 | 2.51 | 4.24 | 2.51 | 4.24 | 1.93 | 4.16 | 1.93 | 3.87 | A |
| NT8GTT72U4ND3YD-3C | 3.60 | 2.96 | 3.67 | 3.74 | 3.70 | 3.78 | 3.78 | 3.80 | 3.76 | 3.80 | 3.63 | 3.81 | 3.63 | 3.74 | A |
| NT8GTT72U4ND4YD-3C | 3.60 | 2.96 | 3.67 | 3.74 | 3.70 | 3.78 | 3.78 | 3.80 | 3.76 | 3.80 | 3.63 | 3.81 | 3.63 | 3.74 | A |
| NT4GT72U8ND9BD-3C | 1.81 | 1.5 | 1.83 | 2.26 | 1.84 | 2.26 | 4.01 | 2.51 | 4.01 | 2.51 | 1.86 | 2.3 | 1.87 | 2.21 | A |
| NT4GT72U8ND9BD-AC | 1.97 | 1.7 | 1.97 | 2.52 | 1.97 | 2.53 | 4.02 | 2.82 | 4.03 | 2.82 | 1.99 | 2.56 | 1.97 | 2.51 | A |

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

($T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$; $V_{DDQ} = 1.8\text{V} \pm 0.1\text{V}$; $V_{DD} = 1.8\text{V} \pm 0.1\text{V}$, See AC Characteristics) (Part 1 of 2)

| Symbol | Parameter | -3C | | -AC | | Unit | Notes |
|---------------|--|-----------------------------|---------------|-----------------------------|---------------|---------------|-------|
| | | Min. | Max. | Min. | Max. | | |
| t_{AC} | DQ output access time from CK/\overline{CK} | -0.45 | +0.45 | -0.40 | +0.40 | ns | |
| t_{DQSCK} | DQS output access time from CK/\overline{CK} | -0.4 | +0.4 | -0.35 | +0.35 | ns | |
| t_{CH} | CK high-level width | 0.48 | 0.52 | 0.48 | 0.52 | t_{CK} | |
| t_{CL} | CK low-level width | 0.48 | 0.52 | 0.48 | 0.52 | t_{CK} | |
| t_{HP} | Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time | Min (t_{CH} , t_{CL}) | - | Min (t_{CH} , t_{CL}) | - | t_{CK} | |
| t_{CK} | Clock Cycle Time | 3 | 8 | 2.5 | 8 | ns | |
| t_{DH} | DQ and DM input hold time | 175 | - | 125 | - | ps | |
| t_{DS} | DQ and DM input setup time | 100 | - | 50 | - | ps | |
| t_{IPW} | Input pulse width | 0.6 | - | 0.6 | - | t_{CK} | |
| t_{DIPW} | DQ and DM input pulse width (each input) | 0.35 | - | 0.35 | - | t_{CK} | |
| t_{HZ} | Data-out high-impedance time from CK/\overline{CK} | - | $t_{AC\ max}$ | - | $t_{AC\ max}$ | ns | |
| $t_{LZ(DQ)}$ | Data-out low-impedance time from CK/\overline{CK} | $2t_{AC\ min}$ | $t_{AC\ max}$ | $2t_{AC\ min}$ | $t_{AC\ max}$ | ns | |
| $t_{LZ(DQS)}$ | DQS/ \overline{DQS} low-impedance time from CK/\overline{CK} | $t_{AC\ min}$ | $t_{AC\ max}$ | $t_{AC\ min}$ | $t_{AC\ max}$ | ns | |
| t_{DQSQ} | DQS-DQ skew (DQS & associated DQ signals) | - | 0.24 | - | 0.20 | ns | |
| t_{QHS} | Data hold Skew Factor | - | 0.34 | - | 0.30 | ns | |
| t_{QH} | Data output hold time from DQS | $t_{HP} - t_{QHS}$ | - | $t_{HP} - t_{QHS}$ | - | ns | |
| t_{DQSS} | Write command to 1st DQS latching transition | -0.25 | 0.25 | -0.25 | 0.25 | t_{CK} | |
| $t_{DQSL(H)}$ | DQS input low (high) pulse width (write cycle) | 0.35 | - | 0.35 | - | t_{CK} | |
| t_{DSS} | DQS falling edge to CK setup time (write cycle) | 0.2 | - | 0.2 | - | t_{CK} | |
| t_{DSH} | DQS falling edge hold time from CK (write cycle) | 0.2 | - | 0.2 | - | t_{CK} | |
| t_{MRD} | Mode register set command cycle time | 2 | - | 2 | - | t_{CK} | |
| t_{WPST} | Write postamble | 0.40 | 0.60 | 0.40 | 0.60 | t_{CK} | |
| t_{WPRE} | Write preamble | 0.35 | - | 0.35 | - | t_{CK} | |
| t_{IH} | Address and control input hold time | 0.275 | - | 0.250 | - | ps | |
| t_{IS} | Address and control input setup time | 0.2 | - | 0.175 | - | ps | |
| t_{RPRE} | Read preamble | 0.9 | 1.1 | 0.9 | 1.1 | t_{CK} | |
| t_{RPST} | Read postamble | 0.4 | 0.6 | 0.4 | 0.6 | t_{CK} | |
| t_{Delay} | Minimum time clocks remains ON after CKE asynchronously drops Low | $t_{IS} + t_{CK} + t_{IH}$ | | $t_{IS} + t_{CK} + t_{IH}$ | | ns | |
| t_{RFC} | Refresh to active/Refresh command time | 127.5 | | 127.5 | | ns | |
| t_{REFI} | Average Periodic Refresh Interval ($85^{\circ}\text{C} < T_{CASE} \leq 95^{\circ}\text{C}$) | 3.9 | | 3.9 | | μs | |
| | Average Periodic Refresh Interval ($0^{\circ}\text{C} \leq T_{CASE} \leq 85^{\circ}\text{C}$) | 7.8 | | 7.8 | | μs | |
| t_{RRD} | Active bank A to Active bank B command | 7.5 | - | 7.5 | - | ns | |



AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

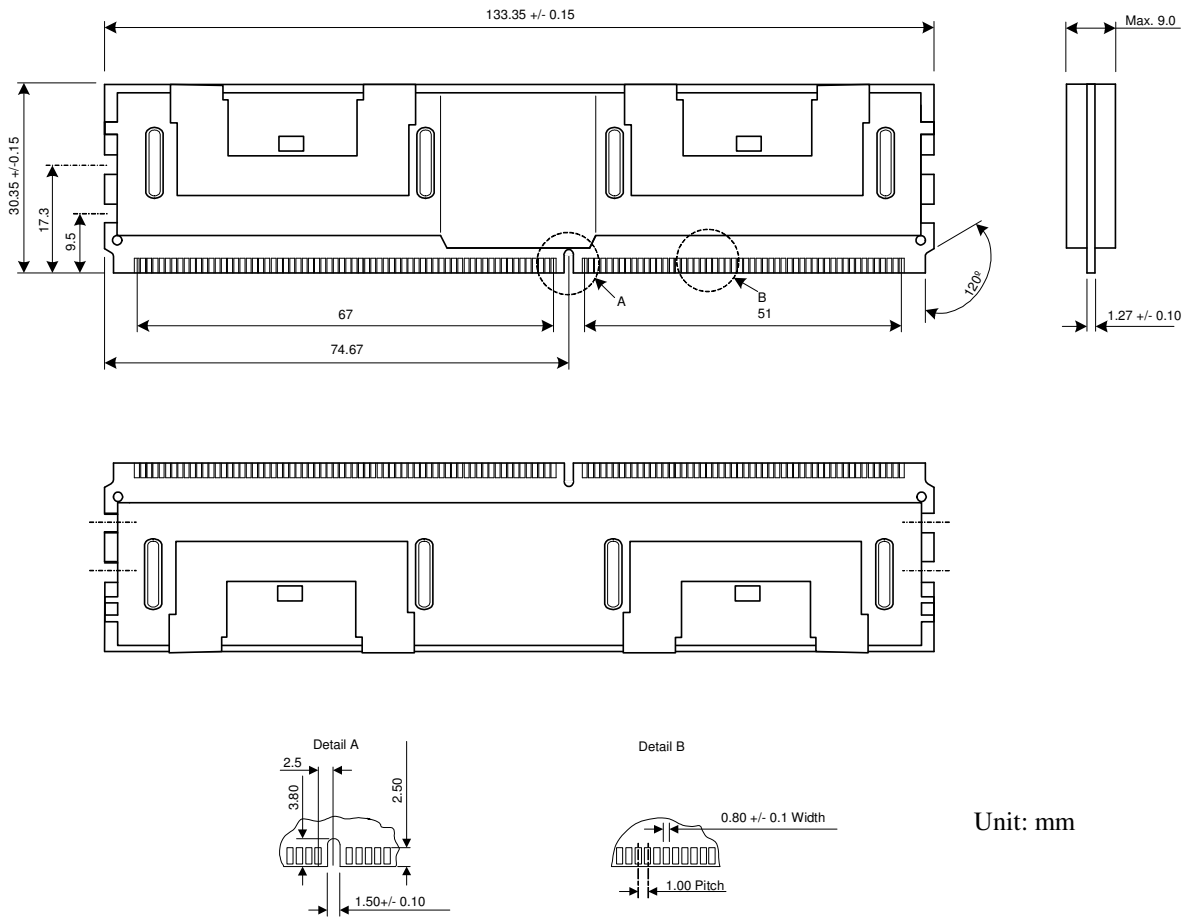
| Symbol | Parameter | -3C | | -AC | | Unit | Notes |
|-------------------------------|--|----------------------------------|--|----------------------------------|--|-----------------|-------|
| | | Min. | Max. | Min. | Max. | | |
| t _{CCD} | $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ | 2 | - | 2 | - | t _{CK} | |
| t _{WR} | Write recovery time | 15 | - | 15 | - | ns | |
| WR | Write recovery time with Auto-Precharge | t _{WR} /t _{CK} | | t _{WR} /t _{CK} | | ns | |
| t _{DAL} | Auto precharge write recovery + precharge time | WR + t _{RP} | - | WR + t _{RP} | - | t _{CK} | |
| t _{WTR} | Internal write to read command delay | 7.5 | - | 7.5 | - | ns | |
| t _{RTP} | Internal read to precharge command delay | 7.5 | | 7.5 | | ns | |
| t _{XSNR} | Exit self refresh to a Non-read command | t _{RFC} + 10 | | t _{RFC} + 10 | | ns | |
| t _{XSRD} | Exit self refresh to a Read command | 200 | | 200 | | t _{CK} | |
| t _{XP} | Exit precharge power down to any Non- read command | 2 | - | 2 | - | t _{CK} | |
| t _{XARD} | Exit active power down to read command | 2 | - | 2 | - | t _{CK} | |
| t _{XARDS} | Exit active power down to read command | 7-AL | | 8-AL | | t _{CK} | |
| t _{CKE} | CKE minimum pulse width | 3 | | 3 | | t _{CK} | |
| t _{OIT} | OCD drive mode output delay | 0 | 12 | 0 | 12 | ns | |
| ODT | | | | | | | |
| t _{AOND} | ODT turn-on delay | 2 | 2 | 2 | 2 | t _{CK} | |
| t _{AON} | ODT turn-on | t _{AC} (min) | t _{AC} (max) + 1 | t _{AC} (min) | t _{AC} (max) + 0.7 | ns | |
| t _{AONPD} | ODT turn-on (Power down mode) | t _{AC} (min) + 2 | 2t _{CK} + t _{AC} (max) + 1 | t _{AC} (min) + 2 | 2t _{CK} + t _{AC} (max) + 1 | ns | |
| t _{AOFD} | ODT turn-off delay | 2.5 | 2.5 | 2.5 | 2.5 | t _{CK} | |
| t _{AOF} | ODT turn-off | t _{AC} (min) | t _{AC} (max) + 0.6 | t _{AC} (min) | t _{AC} (max) + 0.6 | ns | |
| t _{AOFPD} | ODT turn-off (Power down mode) | t _{AC} (min) + 2 | 2.5t _{CK} + t _{AC} (max) + 1 | t _{AC} (min) + 2 | 2.5t _{CK} + t _{AC} (max) + 1 | ns | |
| t _{ANPD} | ODT to power down entry latency | 3 | | 3 | | t _{CK} | |
| t _{AXPD} | ODT power down exit latency | 8 | | 8 | | t _{CK} | |
| Speed Grade Definition | | | | | | | |
| t _{RAS} | Row Active Time | 45 | 70000 | 45 | 70000 | ns | |
| t _{RCD} | RAS to CAS delay | 15 | - | 12.5 | - | ns | |
| t _{RC} | Row Cycle Time | 60 | - | 57.5 | - | ns | |
| t _{RP} | Row Precharge Time | 15 | - | 12.5 | - | ns | |

NT1GT72U89D0BD-AC / NT2GT72U8PD0BD-AC / NT4GT72U4ND0BD-AC / NT4GT72U8ND9BD-AC
 NT1GT72U89D1BD-3C / NT2GT72U8PD1BD-3C / NT4GT72U4ND1BD-3C / NT8GTT72U4ND3YD-3C
 NT1GT72U89D1BN-3C / NT2GT72U8PD1BN-3C / NT4GT72U4ND1BN-3C / NT8GTT72U4ND4YD-3C
 NT1GT72U89D2BD-3C / NT2GT72U8PD2BD-3C / NT4GT72U4ND2BD-3C / NT8GTT72U4ND5YD-3C
 NT1GT72U89D6BD-AC / NT2GT72U8PD6BD-AC / NT4GT72U8ND9BD-3C



Package Dimensions for the following part numbers:

NT1GT72U89D0BD-AC / NT2GT72U8PD0BD-AC / NT4GT72U4ND0BD-AC
 NT1GT72U89D1BD-3C / NT2GT72U8PD1BD-3C / NT4GT72U4ND1BD-3C
 NT1GT72U89D1BN-3C / NT2GT72U8PD1BN-3C / NT4GT72U4ND1BN-3C
 NT1GT72U89D2BD-3C / NT2GT72U8PD2BD-3C / NT4GT72U4ND2BD-3C
 NT8GTT72U4ND3YD-3C / NT8GTT72U4ND4YD-3C / NT4GT72U8ND9BD-3C
 NT4GT72U8ND9BD-AC / NT8GTT72U4ND5YD-3C



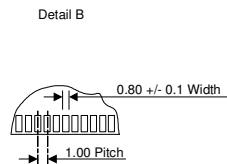
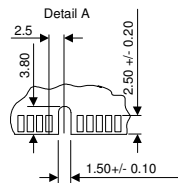
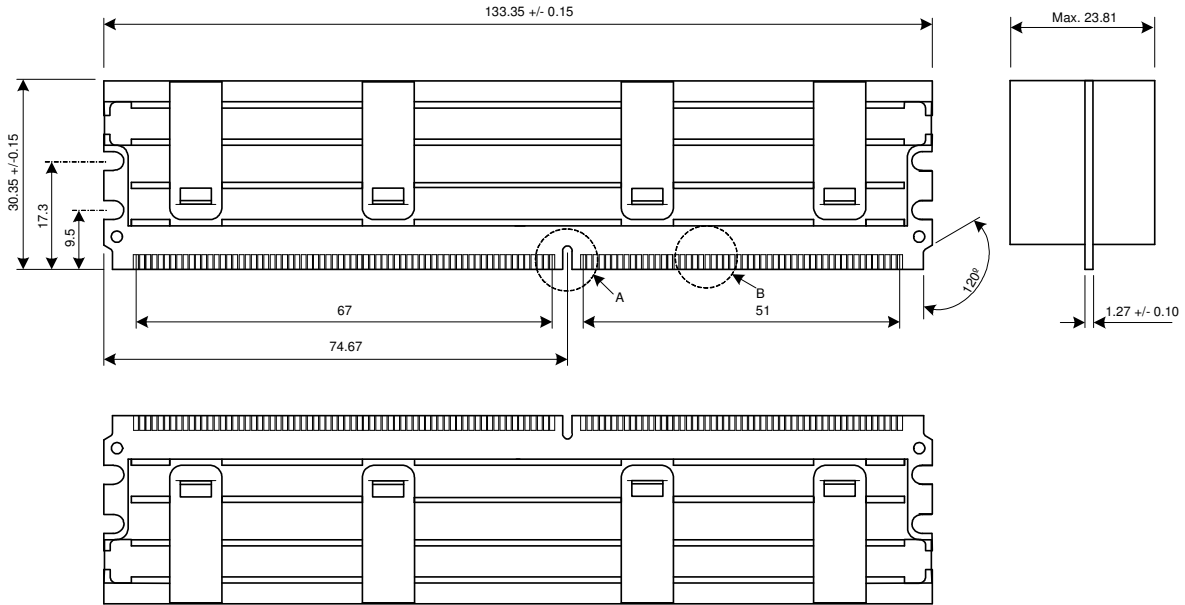
Unit: mm

NT1GT72U89D0BD-AC / NT2GT72U8PD0BD-AC / NT4GT72U4ND0BD-AC / NT4GT72U8ND9BD-AC
 NT1GT72U89D1BD-3C / NT2GT72U8PD1BD-3C / NT4GT72U4ND1BD-3C / NT8GTT72U4ND3YD-3C
 NT1GT72U89D1BN-3C / NT2GT72U8PD1BN-3C / NT4GT72U4ND1BN-3C / NT8GTT72U4ND4YD-3C
 NT1GT72U89D2BD-3C / NT2GT72U8PD2BD-3C / NT4GT72U4ND2BD-3C / NT8GTT72U4ND5YD-3C
 NT1GT72U89D6BD-AC / NT2GT72U8PD6BD-AC / NT4GT72U8ND9BD-3C



Package Dimensions for the following part numbers:

NT1GT72U89D6BD-AC / NT2GT72U8PD6BD-AC



Unit: mm



Revision Log

| Rev | Date | Modification |
|-----|---------|--|
| 0.1 | 02/2008 | Preliminary Release |
| 0.2 | 03/2008 | Add IDT AMB+ Product Information |
| 0.3 | 04/2008 | Add 4GB product information Add environmental parameters Update Package Dimensions |
| 0.4 | 05/2008 | Add 8GB product information Update Package Dimensions Update typo |
| 1.0 | 05/2008 | Official release |
| 1.1 | 06/2008 | Add NT1GT72U89D6BD-AC, NT2GT72U8PD6BD-AC, and NT8GTT72U4ND4YD-3C related specification. |
| 1.2 | 12/2008 | Add NT4GT72U8ND9BD-3C/AC |
| 1.3 | 03/2009 | Add NT8GTT72U4ND5YD-3C |

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