EC²

low profile

T²L COMPATIBLE

Mini SIP LOGIC DELAY LINE

- **T²L FAST input and output**
- **Delay stable and precise**
- **5-pin SIP package (.350 high)**
- **Available in delays from 5 to 500ns**
- **Output isolated and with 10 T²L fan-out capacity**
- **Rise time 4ns maximum**

design notes

The "Mini Sip Series" Logic Delay Lines developed by Engineered Components Company have been designed to provide precise delays with required driving and pick-off circuitry contained in a 5-pin SIP package compatible with T²L FAST circuits. These logic delay lines are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 3 million hours. Module design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the desired delay.

The MSFLDL-TTL is offered in 48 delays from 5ns to 500ns. Delay tolerances are maintained as shown in the accompanying part number table, when tested under the "Test Conditions" shown. Delay time is measured at the +1.5V level on the leading edge. Rise time for all modules is 4ns maximum when measured from 0.75V to 2.4V. Temperature coefficient of delay is approximately +1200 ppm/°C over the operating temperature range of 0 to +70° C.

These modules accept either logic "1" or logic "0" inputs and reproduce the logic at the output without inversion. The delay modules are intended primarily for use with positive going pulses and are calibrated to the tolerances shown in the table on rising edge delay; where best accuracy is desired in applications using falling edge timing, it is recommended that a special unit be calibrated for the specific application. Each module has the capability of driving up to 10 T²L loads.

These "Mini SIP Series" modules are packaged in a 5-pin SIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, Type SDG-F, and are fully encapsulated in epoxy resin. Leads meet the solderability requirements of MIL-STD-202, Method 208. Corner standoffs on the housing provide positive standoff from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

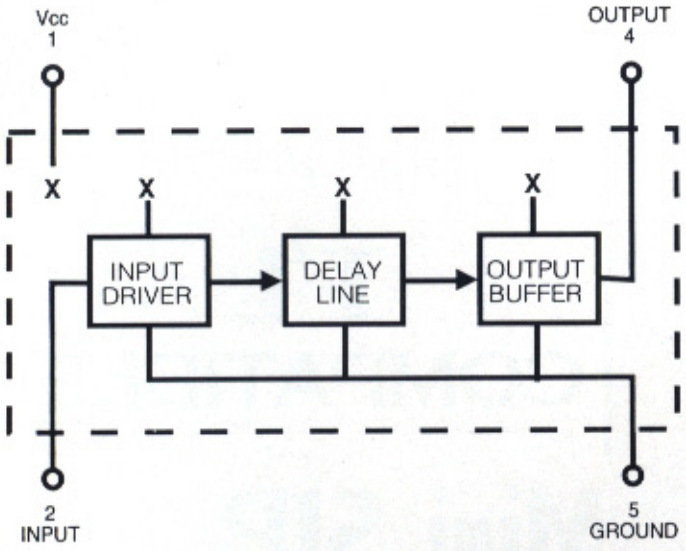
Marking consists of manufacturer's logo (EC²), Federal Supply Code, part number, pin one (1) identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

EC² **engineered components company**

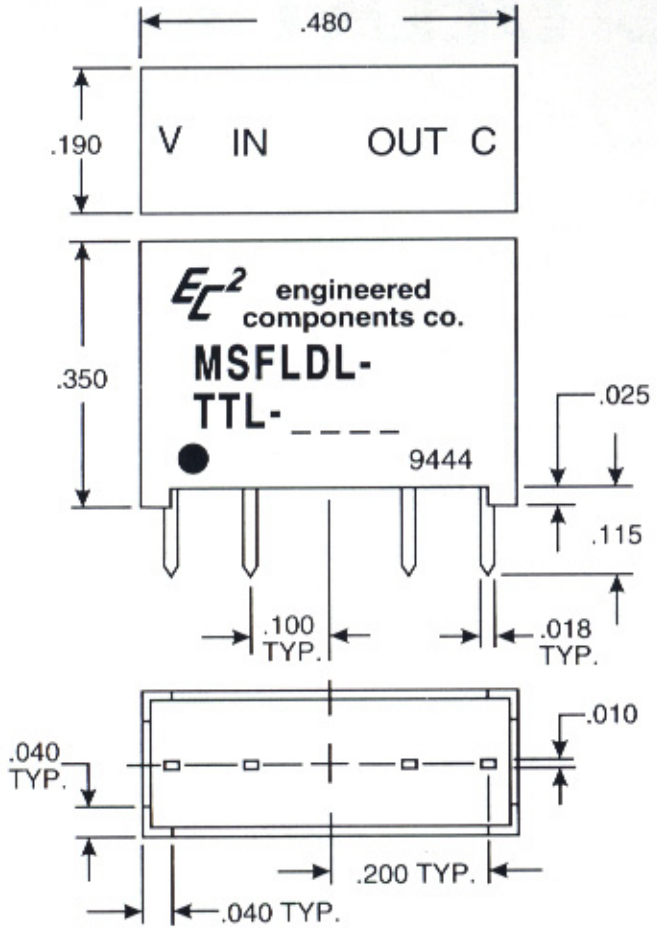
3580 SACRAMENTO DRIVE • P.O. BOX 8121, SAN LUIS OBISPO, CA 93403-8121

(805) 544-3800 • OUTSIDE CALIFORNIA (800) 235-4144 • FAX (805) 544-8091

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



OPERATING SPECIFICATIONS

* V_{CC} supply voltage: . . . . . 4.75 to 5.25V DC
V_{CC} supply current:
Constant "0" in . . . . . 60mA typical
Constant "1" in . . . . . 7mA typical

Logic 1 Input:
Voltage . . . . . 2V min.; V_{CC} max.
Current . . . . . 2.7V = 20uA max.
5.5V = 1mA max.

Logic 0 Input:
Voltage . . . . . .8V max.
Current . . . . . –.6mA max.

Logic 1 Voltage out: . . . . . 2.7V min.
Logic 0 Voltage out: . . . . . .5V max.
Operating temperature range: . . . . . 0 to 70°C.
Storage temperature: . . . . . –55 to +125°C.

* Delays increase or decrease approximately 4% for a respective increase or decrease of 5% in supply voltage.

PART NUMBER TABLE

DELAYS AND TOLERANCES (in ns)			
PART NUMBER	OUTPUT	PART NUMBER	OUTPUT
MSFLDL-TTL-5	5±1	MSFLDL-TTL-45	45±2
MSFLDL-TTL-6	6±1	MSFLDL-TTL-50	50±2
MSFLDL-TTL-7	7±1	MSFLDL-TTL-55	55±2
MSFLDL-TTL-8	8±1	MSFLDL-TTL-60	60±2
MSFLDL-TTL-9	9±1	MSFLDL-TTL-65	65±2.5
MSFLDL-TTL-10	10±1	MSFLDL-TTL-70	70±2.5
MSFLDL-TTL-11	11±1	MSFLDL-TTL-75	75±2.5
MSFLDL-TTL-12	12±1	MSFLDL-TTL-80	80±2.5
MSFLDL-TTL-13	13±1	MSFLDL-TTL-85	85±3
MSFLDL-TTL-14	14±1	MSFLDL-TTL-90	90±3
MSFLDL-TTL-15	15±1	MSFLDL-TTL-95	95±3
MSFLDL-TTL-16	16±1	MSFLDL-TTL-100	100±3
MSFLDL-TTL-17	17±1	MSFLDL-TTL-125	125±4
MSFLDL-TTL-18	18±1	MSFLDL-TTL-150	150±4.5
MSFLDL-TTL-19	19±1	MSFLDL-TTL-175	175±5
MSFLDL-TTL-20	20±1	MSFLDL-TTL-200	200±6
MSFLDL-TTL-21	21±1	MSFLDL-TTL-225	225±7
MSFLDL-TTL-22	22±1	MSFLDL-TTL-250	250±8
MSFLDL-TTL-23	23±1	MSFLDL-TTL-275	275±9
MSFLDL-TTL-24	24±1	MSFLDL-TTL-300	300±10
MSFLDL-TTL-25	25±1	MSFLDL-TTL-350	350±11
MSFLDL-TTL-30	30±1.5	MSFLDL-TTL-400	400±12
MSFLDL-TTL-35	35±1.5	MSFLDL-TTL-450	450±14
MSFLDL-TTL-40	40±1.5	MSFLDL-TTL-500	500±15

TEST CONDITIONS

1. All measurements are made at 25°C.
2. V_{CC} supply voltage is maintained at 5.0V DC.
3. All units are tested using a FAST toggle-type positive input pulse and one FAST load at the output.

ø 4. Input pulse width used is 100% longer than delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

ø All modules can be operated with a minimum input pulse width of 100% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified delay times for specific applications.