MSC23832-xxBS16/DS16

Preliminary

8,388,608-Word by 32-Bit DRAM Module: Fast Page Mode

DESCRIPTION

The OKI MSC23832-xxBS16/DS16 is a fully decoded 8,388,608-word x 32-bit CMOS dynamic Random Access Memory module composed of sixteen 16-Mb DRAMs in SOJ (MSM5117400) packages mounted with sisteen 0.2 µF decoupling capacitors on a 72-pin glass epoxy single-inline package. This module is generally used for non-parity memory expansion applications such as fax machines, printers and personal computers.

FEATURES

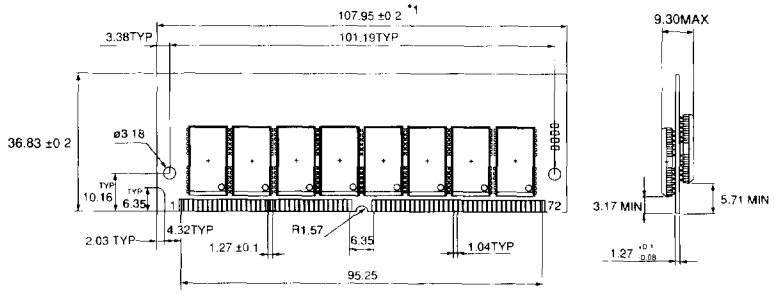
- 8-Meg x 32-bit organization
- 72-pin socket insertable module
  - MSC23832-xxBS16: Gold tab
  - MSC23832-xxDS16: Solder tab
- Single +5 V supply ±10% tolerance
- Access times: 60, 70, 80 ns
- Input: TTL compatible
- Output: TTL compatible, three-state
- Refresh: 2048 cycles/32 ms
- $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{CAS}$-before-$\overline{RAS}$ hidden refresh, $\overline{RAS}$-only refresh capability

Family Organization

Part Number	Access Time (Max)			Cycle Time (Min)	Power Dissipation (Max)	
	t_{RAC}	t_{AA}	t_{CAC}		Operating	Standby
MSC23832-60BS16/DS16	60 ns	30 ns	15 ns	110 ns	5500 mW	88 mW (MOS level)
MSC23832-70BS16/DS16	70 ns	35 ns	20 ns	130 ns	5060 mW	
MSC23832-80BS16/DS16	80 ns	40 ns	20 ns	150 ns	4620 mW	

PIN CONFIGURATION

MSC23832-xxBS16/DS16



*1 The common size difference of the board width 12.5mm of its height is specified as ±0.2. The value above 12.5mm is specified as ±0.5.

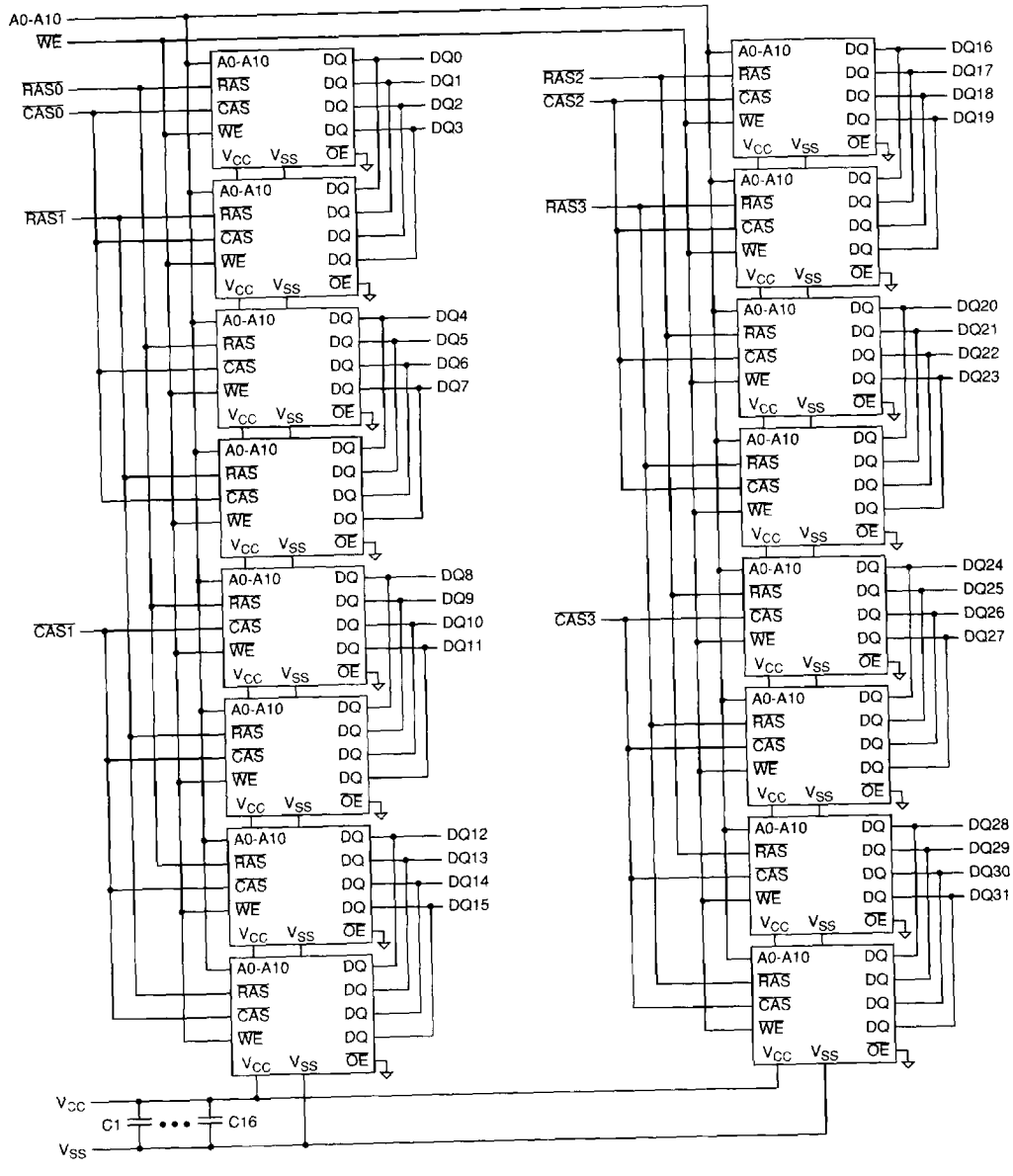
Pin Configuration

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	V_{SS}	16	A4	31	A8	46	N.C.	61	DQ13
2	DQ0	17	A5	32	A9	47	$\overline{WE}$	62	DQ30
3	DQ16	18	A6	33	$\overline{RAS3}$	48	N.C.	63	DQ14
4	DQ1	19	A10	34	$\overline{RAS2}$	49	DQ8	64	DQ31
5	DQ17	20	DQ4	35	N.C.	50	DQ24	65	DQ15
6	DQ2	21	DQ20	36	N.C.	51	DQ9	66	N.C.
7	DQ18	22	DQ5	37	N.C.	52	DQ25	67	PD0
8	DQ3	23	DQ21	38	N.C.	53	DQ10	68	PD1
9	DQ19	24	DQ6	39	V_{SS}	54	DQ26	69	PD2
10	V_{CC}	25	DQ22	40	$\overline{CAS0}$	55	DQ11	70	PD3
11	N.C.	26	DQ7	41	$\overline{CAS2}$	56	DQ27	71	N.C.
12	A0	27	DQ23	42	$\overline{CAS3}$	57	DQ12	72	V_{SS}
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ28		
14	A2	29	N.C.	44	$\overline{RAS0}$	59	V_{CC}		
15	A3	30	V_{CC}	45	$\overline{RAS1}$	60	DQ29		

Presence Detect Pins

Pin Number	Pin Name	60 ns	70 ns	80 ns
67	PD0	N.C.	N.C.	N.C.
68	PD1	V_{SS}	V_{SS}	V_{SS}
69	PD2	N.C.	V_{SS}	N.C.
70	PD3	N.C.	N.C.	V_{SS}

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ +7.0	V
Voltage V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 ~ +7.0	V
Short circuit output current	I_{OS}	50	mA
Power dissipation	P_D	16	W
Operating temperature	T_{OPR}	0 ~ +70	°C
Storage temperature	T_{STG}	-40 ~ +125	°C

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (T_a = 0 ~ +70°C)

Parameter	Symbol	Rated Value			Unit
		Min	Typ	Max	
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	6.5	V
Input low voltage	V_{IL}	-1.0	-	0.8	V

Capacitance (T_a = 25°C, f = 1 MHz) [1]

Parameter	Symbol	Typ	Max	Unit
Input capacitance (A0 ~ A10)	C_{IN1}	-	130	pF
Input capacitance ($\overline{WE}$)	C_{IN2}	-	132	pF
Input capacitance ($\overline{RAS0}$ ~ $\overline{RAS3}$, $\overline{CAS0}$ ~ $\overline{CAS3}$)	C_{IN3}	-	48	pF
I/O capacitance (DQ0 ~ DQ31)	C_{DQ}	-	30	pF

1. Capacitance measured with Boonton Meter.

DC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C)

Parameter	Symbol	Condition		60 ns		70 ns		80 ns		Unit	Note
				Min	Max	Min	Max	Min	Max		
Input leakage current	I_{LI}	0 V ≤ V_I ≤ 6.5 V; All other pins not under test = 0 V		-160	160	-160	160	-160	160	µA	
Output leakage current	I_{LO}	D_{OUT} disable 0 V ≤ V_O ≤ 5.5 V		-20	20	-20	20	-20	20	µA	
Output high voltage	V_{OH}	I_{OH} = -5.0 mA		2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA		0	0.4	0	0.4	0	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min.		-	1000	-	920	-	840	mA	[1] [2]
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = Hi-Z	TTL	-	32	-	32	-	32	mA	
			MOS	-	16	-	16	-	16	mA	
Average power supply current ($\overline{RAS}$-only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min.		-	1000	-	920	-	840	mA	[1] [2]
Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$, t_{RC} = min.		-	1000	-	920	-	840	mA	[1]
Average power supply current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min.		-	920	-	840	-	760	mA	[1] [3]

1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C) [1] [2] [3]

Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110	-	130	-	150	-	ns	
Fast Page Mode cycle time	t_{PC}	40	-	45	-	50	-	ns	
Access time from $\overline{RAS}$	t_{RAC}	-	60	-	70	-	80	ns	[4] [5] [6]
Access time for $\overline{CAS}$	t_{CAC}	-	15	-	20	-	20	ns	[4] [5]
Access time from column address	t_{AA}	-	30	-	35	-	40	ns	[4] [6]
Access time from $\overline{CAS}$ precharge	t_{CPA}	-	35	-	40	-	45	ns	[4]
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	-	0	-	0	-	ns	
Output buffer turn-off delay time	t_{OFF}	0	15	0	20	0	20	ns	[7]
Transition time	t_T	3	50	3	50	3	50	ns	[3]
Refresh period	t_{REF}	-	32	-	32	-	32	ms	
$\overline{RAS}$ precharge time	t_{RP}	40	-	50	-	60	-	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15	-	20	-	20	-	ns	
$\overline{CAS}$ precharge time (Fast Page Mode)	t_{CP}	10	-	10	-	10	-	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10K	20	10K	20	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	-	70	-	80	-	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	-	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	[5]
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	[6]
Row address set-up time	t_{ASR}	0	-	0	-	0	-	ns	
Row address hold time	t_{RAH}	10	-	10	-	10	-	ns	
Column address set-up time	t_{ASC}	0	-	0	-	0	-	ns	
Column address hold time	t_{CAH}	15	-	15	-	15	-	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	50	-	55	-	60	-	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	-	35	-	40	-	ns	
Read command set-up time	t_{RCS}	0	-	0	-	0	-	ns	
Read command hold time	t_{RCH}	0	-	0	-	0	-	ns	[8]
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	-	0	-	0	-	ns	[8]
Write command set-up time	t_{WCS}	0	-	0	-	0	-	ns	
Write command hold time	t_{WCH}	10	-	15	-	15	-	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	45	-	55	-	60	-	ns	
Write command pulse width	t_{WP}	10	-	10	-	10	-	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	-	20	-	20	-	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	-	20	-	20	-	ns	
Data-in set-up time	t_{DS}	0	-	0	-	0	-	ns	
Data-in hold time	t_{DH}	15	-	15	-	15	-	ns	

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C) [1] [2] [3] (Continued)

Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
Data-in hold time from $\overline{RAS}$	t_{DHR}	50	-	55	-	60	-	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	-	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{CSR}	10	-	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{CHR}	20	-	20	-	20	-	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	-	40	-	40	-	ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{WRP}	10	-	10	-	10	-	ns	
$\overline{WE}$ hold time from $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{WRH}	10	-	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{WE}$ set-up time (Test Mode)	t_{WSR}	10	-	10	-	10	-	ns	[9] [10]
$\overline{RAS}$ to $\overline{WE}$ hold time (Test Mode)	t_{WHR}	20	-	20	-	20	-	ns	[9] [10]

1. A start-up delay of 200 µs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh) before proper device operation is achieved. When using the internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles is required.
2. AC measurements assume t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring input timing signals. Transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2 TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, access time is controlled by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, access time is controlled by t_{AA}.
7. t_{OFF} (max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is an 8-bit parallel test function. CA10, CA1, CA0 are not used. In a read cycle, if all internal bits are equal, the I/O pin will indicate a high level. If any internal bits are not equal, the data I/O pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
10. In a test mode read cycle, the access time parameters are delayed by 5 ns.The test mode parameters are obtained by adding 5 ns to the normal read cycle values.

See ADDENDUM F for AC Timing Waveforms