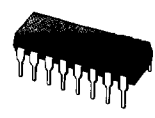
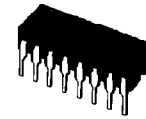
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

- HIGH SPEED
  t_{PD} = 25 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  STANDBY STATE I_{CC}=4 μA (MAX.) AT T_A=25°C
  ACTIVE STATE I_{CC} = 200 μA (TYP.) AT V_{CC}=5V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OH} = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- WIDE OUTPUT PULSE WIDTH RANGE
  t_{WOUT} = 120 ns ~ 60 s OVER AT V_{CC} = 4.5 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS123



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

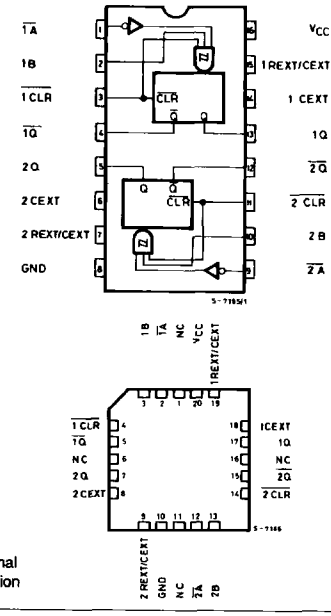
ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

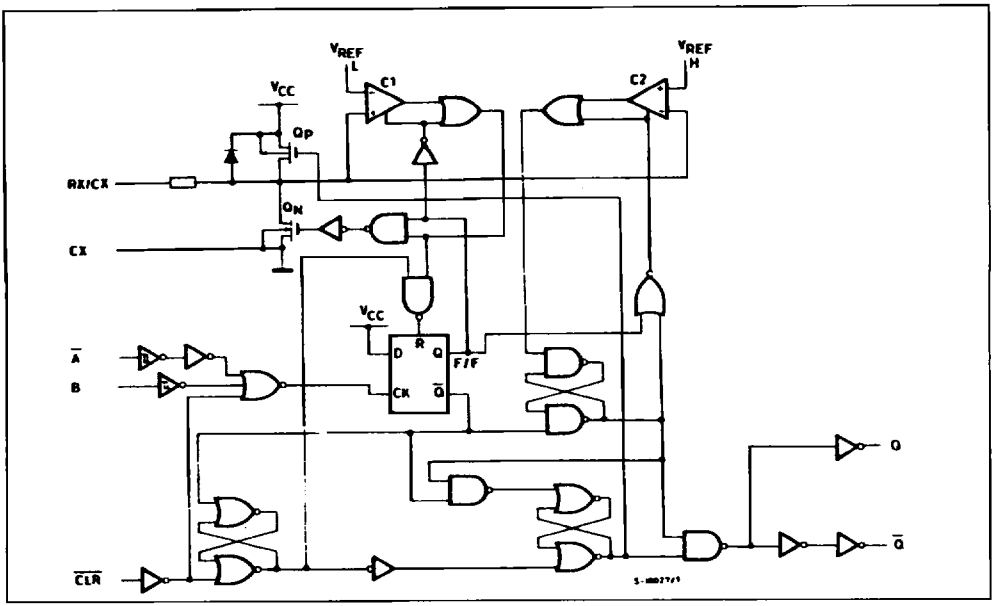
DESCRIPTION

The M54/74HC123 is a high speed CMOS MONOSTABLE multivibrator fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs, $\overline{A}$ INPUT (negative edge) and B INPUT (positive edge). These inputs are valid for slow rising/falling signals, (tr = tf = I sec). The device may also be triggered by using the CLR input (positive-edge) because of the Schmitt-trigger input ; after triggering the output maintains the MONOSTABLE state for the time period determined by the external resistor Rx and capacitor Cx. When Cx ≥ 10nF and Rx ≥ 10KΩ, the output pulse width value is approssimatively given by the formula: $t_{w(out)} = K \bullet Cx \bullet Rx$.
Two different pulse width constant are available:
K ≅ 0.45 for HC123 K ≅ 1 for HC123A.
Taking $\overline{CLR}$ low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer. Limit for values of Cx and Rx :
Cx : NO LIMIT
Rx : V_{CC} < 3.0 V 5 KΩ to 1 MΩ
V_{CC} ≥ 3.0 V 1 KΩ to 1 MΩ
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

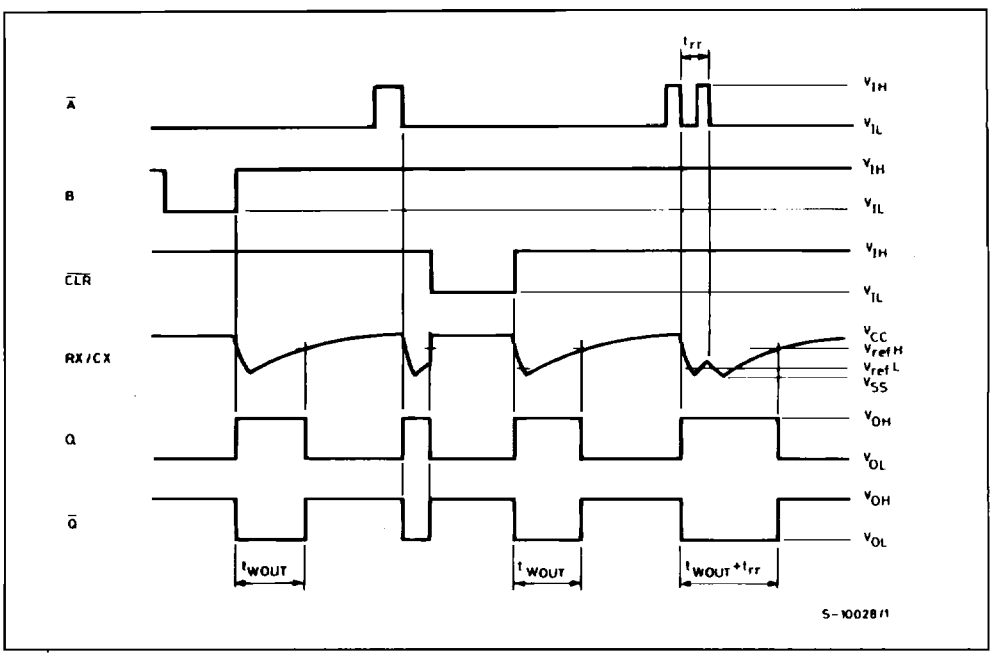
PIN CONNECTIONS (top view)



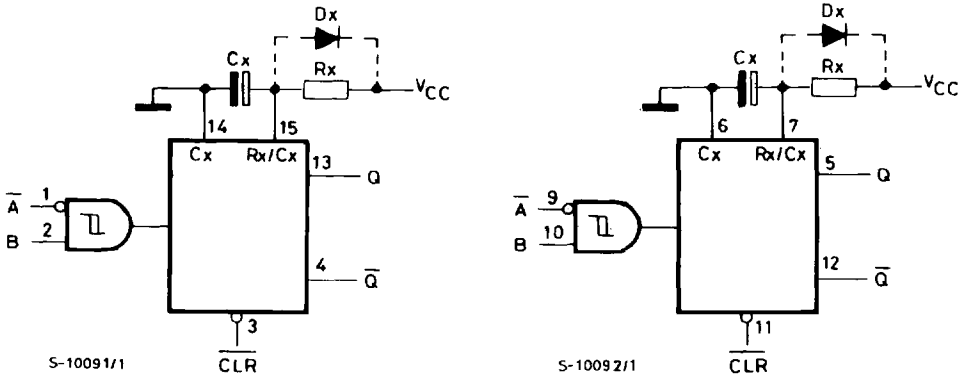
SYSTEM DIAGRAM



TIMING CHART



BLOCK DIAGRAM



Note :

(1) Cx, Rx, Dx are external components.

(2) Dx is a clamping diode.

The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly through an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidy, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows :

$t_f \geq (V_{CC} - 0.7) \cdot Cx/20mA$

In cases where t_f is too short an external clamping diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

STAND-BY STATE

The external capacitor, Cx, is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned-off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

TRIGGER OPERATION

Triggering occurs when :

1 st) A is "low" and B has a falling edge ;
2 nd) B is "high" and A has a rising edge ;
3 rd) A is low and B is high and C1 has a rising edge.

After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node R/C external falls.

When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn resets the flip-flop and Qn is turned off.

At this point C1 stops functioning but C2 continues to operate.

The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx.

Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH}. At this point C2 output goes low and O goes low. C2 stop operating. That means that after triggering when the voltage R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where Rx · Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse tw (out) is as follows :

$$t_{W(OUT)} = 0.46\ Cx \cdot Rx\ (HC123)$$

$$t_{W(OUT)} = Cx \cdot Rx\ (HC123A)$$

FUNCTIONAL DESCRIPTION (continued)

RE-TRIGGERED OPERATION

When a second trigger pulse follows the first its effect will depend on the state of the multivibrator. If the capacitor Cx is being charged the voltage level of R/C external falls to Vrefl again and Q remains high i.e. the retrigger pulse arrives in a time shorter than the period Rx · Cx seconds, the capacitor charging time constant. If the second trigger pulse is very close to the initial trigger pulse it is ineffective ; i.e. the second trigger must arrive in the capacitor discharge cycle to be ineffective; Hence the minimum time for a second trigger to be effective depends on Vcc and Cx.

RESET OPERATION

CL is normally high. If CL is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.

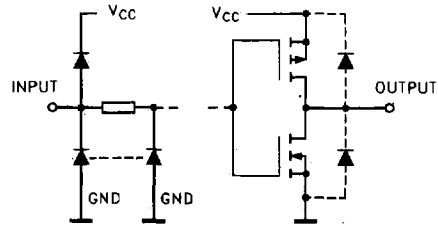
Also transistor Op is turned on and Cx is charged quicky to Vcc. This means if CL input goes low, the IC becomes waiting state both in operating and non operating state.

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
⌐	H	H	⌐	⌐	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	⌐	H	⌐	⌐	OUTPUT ENABLE
L	H	⌐	⌐	⌐	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X: Don't Care Z: High Impedance

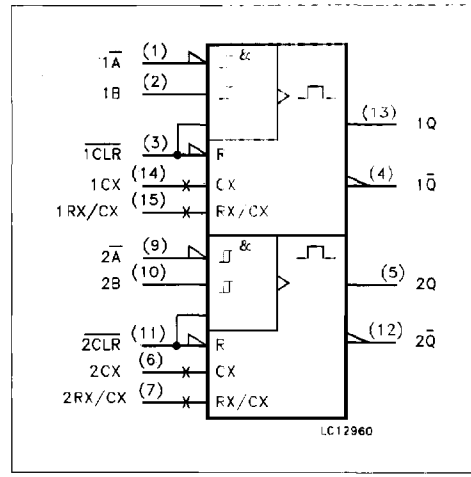
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	Trigger Inputs (Negative Edge Triggered)
2, 10	1B, 2B	Trigger Inputs (Positive Edge Triggered)
3, 11	$1\overline{CLR}$, $2\overline{CLR}$	Direct Reset LOW and Trigger Action at Positive Edge
4, 12	$1\overline{Q}$, $2\overline{Q}$	Outputs (Active LOW)
7	$2R_{EXT}/C_{EXT}$	External Resistor Capacitor Connection
13, 5	1Q, 2Q	Outputs (Active HIGH)
14, 6	$1C_{EXT}$ $2C_{EXT}$	External Capacitor Connection
15	$1R_{EXT}/C_{EXT}$	External Resistor Capacitor Connection
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time		0 to 1000	ns
			0 to 500	
			0 to 400	
C_X	External Capacitor		NO LIMITATION	pF
R_X	External Resistor	V_{CC} < 3 V	5K to 1M	Ω
		V_{CC} ≥ 3 V	1K to 1M	

(*) The maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of device and leakage due to the board layout and surface resistance. Susceptibility to externally induced noise may occur for Rx > 1MΩ

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value						Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC	
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 μA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	μA
I_I	R/C Terminal Off State Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	μA
I_{CC}	Active State Supply Current (1)	2.0	V_I = V_{CC} or GND Pin 7 or 15 V_{IN} = V_{CC}/2			45	200		260		320	μA
		4.5				500	600		780		960	μA
		6.0				0.7	1		1.3		1.6	mA

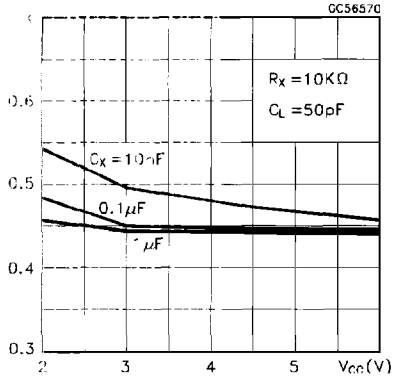
(1): Per Circuit

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

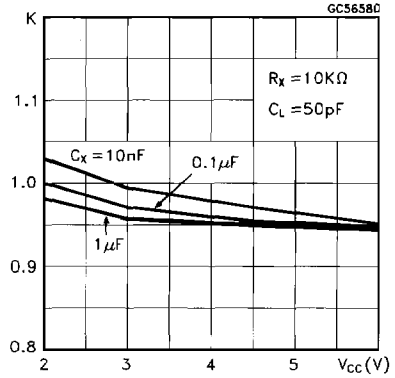
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - Q, $\overline{Q}$)	2.0			102	210		265		315	ns
		4.5			29	42		53		63	
		6.0			22	36		45		54	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ TRIGGER - Q, $\overline{Q}$)	2.0			102	235		295		355	ns
		4.5			31	47		59		71	
		6.0			23	40		50		60	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	2.0			68	160		200		240	ns
		4.5			20	32		40		48	
		6.0			16	27		34		41	
t_{WOUT}	Output Pulse Width (for HC123)	2.0	C_X = 100 pF R_X = 10 KΩ		1.4						µs
		4.5			1.2						
		6.0			1.1						
		2.0	C_X = 0.1 µF R_X = 100 KΩ		4.6						ms
		4.5			4.4						
		6.0			4.3						
t_{WOUT}	Output Pulse Width (for HC123A)	2.0	C_X = 100 pF R_X = 10 KΩ		1.9						µs
		4.5			1.6						
		6.0			1.5						
		2.0	C_X = 0.1 µF R_X = 100 KΩ		9.8						ms
		4.5			9.5						
		6.0			9.4						
Δt_{WOUT}	Output Pulse Width Error Between Circuits in Same Package				±1						%
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width	2.0				75		95		110	ns
		4.5				15		19		22	
		6.0				13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$)	2.0				75		95		110	ns
		4.5				15		19		22	
		6.0				13		16		19	
t_{rr}	Minimum Retrigger Time	2.0	C_X = 100 pF R_X = 1 KΩ		325						ns
		4.5			108						
		6.0			78						
		2.0	C_X = 0.1 µF R_X = 100 KΩ		5						µs
		4.5			1.4						
		6.0			1.2						
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				162						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} * V_{CC} * f_{IN} + I_{CC}$' Duty/100 + Ic/2 (per monostable) (I_{CC}': Active Supply Current) (Duty:%)

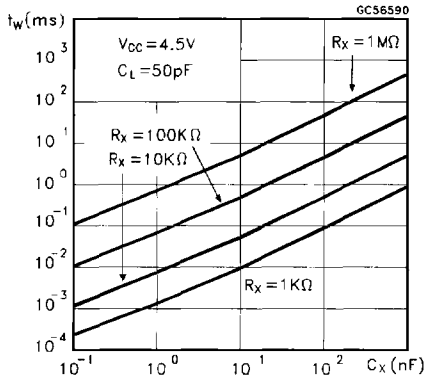
Output Pulse Width Constant Characteristics (for HC123)



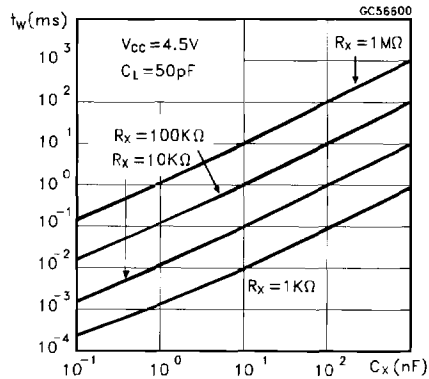
Output Pulse Width Constant Characteristics (for HC123A)



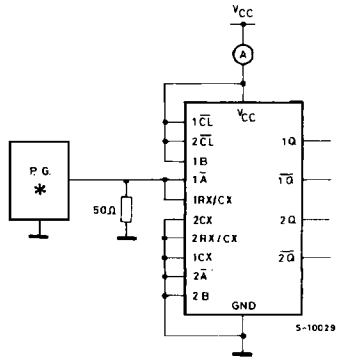
Output Pulse Width Characteristics (for HC123)



Output Pulse Width Characteristics (for HC123A)



TEST CIRCUIT I_{CC} (Opr)



* TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN SASE OF SWITCHING CHARACTERISTICS TESTS.

SWITCHING CHARACTERISTICS TEST WAVEFORM