

DESCRIPTION

The LX5241/42/43 is a multimode SCSI terminator that conforms to the SCSI Parallel Interconnect-2 (SPI-2) specification developed by the T10 standards committee for low voltage differential (LVD) termination, while providing backwards compatibility to the SCSI, SCSI-2, and SPI single-ended specifications. Multimode compatibility permits the use of legacy devices on the bus without hardware alterations. Automatic mode selection is achieved through voltage detection on the diffsense line.

The LX5241/42/43 utilizes Linfinity's UltraMAX technology which delivers the ultimate in SCSI bus performance while saving component cost and board area. Elimination of the external capacitors also mitigates the need for a lengthy capacitor selection process. The individual high bandwidth drivers also maximize channel separation and reduce channel to channel noise and cross talk. The high bandwidth architecture insures ULTRA2 performance while providing a clear migration path to ULTRA3 and beyond.

When the LX5241/42/43 is enabled, the differential sense (DIFFSENSE) pin supplies a voltage between 1.2V and 1.4V. In application,

this pin is tied to the DIFFSENSE input of the corresponding LVD transceivers. This action enables the LVD transceiver function. DIFFSENSE is capable of supplying a maximum of 15mA. Tying the DIFFSENSE pin high places the LX5241/42/43 in a HI Z state indicating the presence of an HVD device. Tying the pin low places the part in a single-ended mode while also signaling the multimode transceiver to operate in a single-ended mode.

Recognizing the needs of portable and configurable peripherals, the LX5241/42/43 have a TTL compatible sleep/disable mode. During this sleep/disable mode, power dissipation is reduced to a meager 15µA while also placing all outputs in a HI Z state. Also during sleep/disable mode, the DIFFSENSE function is disabled and is placed in a HI Z state.

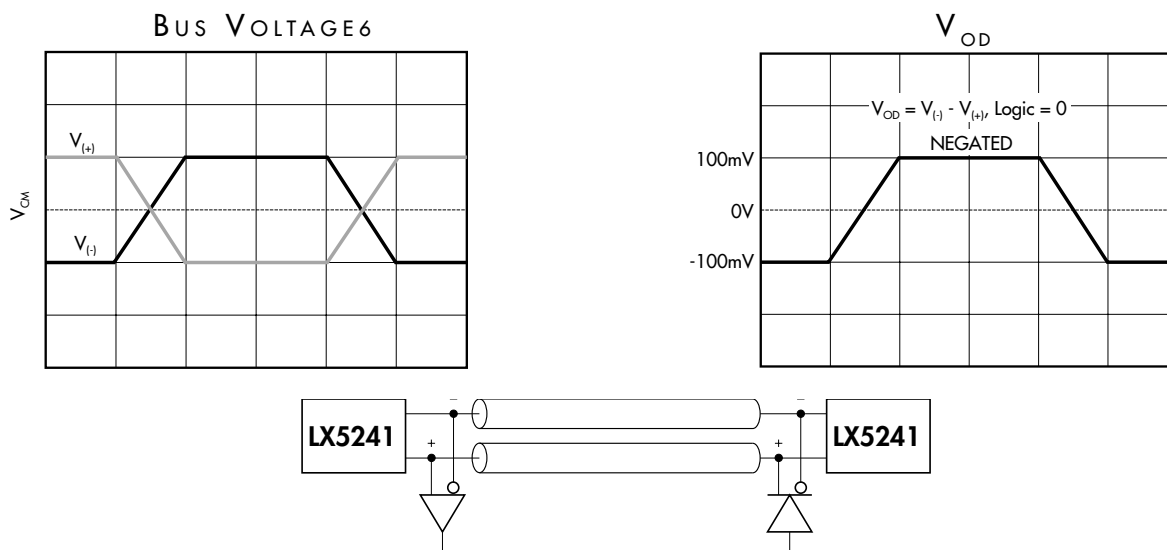
Another key feature of the LX5241/42/43 is the master / slave function. Driving this pin high or floating the pin enables the 1.3V DIFFSENSE reference. Driving the pin low disables the on board DIFFSENSE reference and enables use of an external master reference device.

KEY FEATURES

- Auto-Selectable LVD or Single-Ended Termination
- 3.0pF Maximum Disabled Output Capacitance
- Fast Response, No External Capacitors Required
- Compatible with Active Negation Drivers
- 15µA Supply Current in Disconnect Mode
- Logic Command Disconnects All Termination Lines
- Diffsense Line Driver
- Ground Driver Integrated for Single-Ended Operation
- Current Limit and Thermal Protection
- Hot-Swap Compatible (Single-Ended)
- Compatible with SCSI 1, 2, 3, Fast-20, and the Pending SPI-2 LVD
- See LX5245/5246 for LVD Termination Only
- Pin Compatible With DS2119 and UCC5630

NOTE: For current data & package dimensions, visit our web site: <http://www.linfinit.com>.

PRODUCT HIGHLIGHT



PACKAGE ORDER INFORMATION

| T_A (°C) | DB Plastic SSOP 36-pin | PW Plastic TSSOP 24-pin | PW Plastic TSSOP 28-pin |
|------------|--------------------------|--------------------------|-------------------------|
| 0 to 70 | LX5241CDBK LX5242CDBK | LX5241CPWK LX5242CPWK | LX5243CPWK — |

Note: All surface-mount packages are available in Tape & Reel.
Append the letter "T" to part number. (i.e. LX5241CDBT)

MULTIMODE SCSI TERMINATOR

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ABSOLUTE MAXIMUM RATINGS (Note 1)

| | |
|--|----------------|
| TermPwr Voltage | +7V |
| Operating Junction Temperature | |
| Plastic (DB, PW Packages) | 150°C |
| Storage Temperature Range | -65°C to 150°C |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

THERMAL DATA

DB PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA} **50°C/W**

PW PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA} **100°C/W**

Junction Temperature Calculation: $T_j = T_A + (P_D \times \theta_{JA})$.

The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

MASTER / SLAVE FUNCTION TABLE

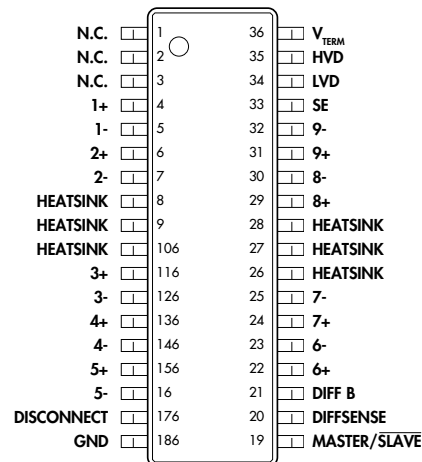
| MASTER / SLAVE | DIFFSENSE Status | |
|----------------|------------------|-------------|
| L* | HI Z | 0mA |
| H | 1.3V | 15mA Source |
| Open (Pull-up) | 1.3V | 15mA Source |

* When in Low state, terminator will detect state of DIFFSENSE line.

DIFFSENSE / POWER UP / POWER DOWN FUNCTION TABLE

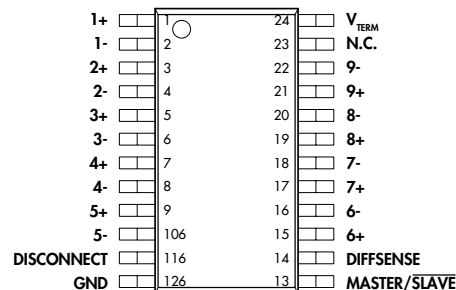
| LX5241/5243 DISCONNECT | LX5242 DISCONNECT | DIFF SENSE | Outputs | | Quiescent Current |
|---------------------------|----------------------|---------------|---------|------|----------------------|
| | | | Status | Type | |
| L | H | L < 0.5V | Enable | S.E. | 7mA |
| L | H | 0.7 - 1.9V | Enable | LVD | 21mA |
| L | H | H > 2.4V | Disable | HI Z | 1mA |
| H Open | L Open | X | Disable | HI Z | 10µA |

PACKAGE PIN OUTS



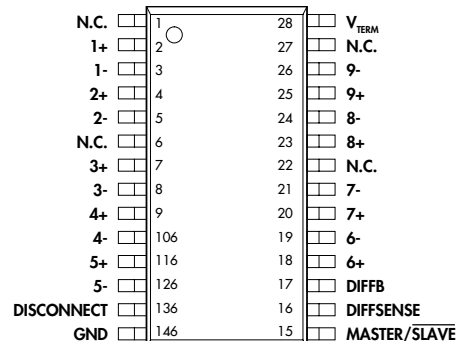
DB PACKAGE (Top View)

LX5241/5242 ("N.C." = No Internal Connection)



PW PACKAGE (Top View)

LX5241/5242 ("N.C." = No Internal Connection)



PW PACKAGE (Top View)

LX5243 ("N.C." = No Internal Connection)

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RECOMMENDED OPERATING CONDITIONS (Note 2)

| Parameter | Symbol | Recommended Operating Conditions | | | Units |
|--|--------|----------------------------------|------|------------|-------|
| | | Min. | Typ. | Max. | |
| Tempwr Voltage | LVD | 3.0 | | 5.25 | V |
| | SE | 3.5 | | 5.25 | V |
| Signal Line Voltage | | 0 | | 5.0 | V |
| Disconnect Input Voltage | | 0 | | V_{TERM} | V |
| Operating Virtual Junction Temperature Range | | | | | |
| LX5241C / 5242C / 5243C | | 0 | | 70 | °C |

Note 2. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperature range of $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, TermPwr = 4.75V. For the LX5241/5243 DISCONNECT = L, for the LX5242 DISCONNECT = H. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

| Parameter | Symbol | Test Conditions | LX5241 / 5242 / 5243 | | | Units |
|---|------------------|---|----------------------|------|-------|---------------|
| | | | Min. | Typ. | Max. | |
| LVD Terminator Section | | | | | | |
| TermPwr Supply Current | LVD I_{CC} | All term lines = Open | | 25 | 30 | mA |
| | | LX5241/5243: DISCONNECT > 2.0V, LX5242: DISCONNECT < 0.8V | | 15 | 35 | μA |
| Common Mode Voltage | V_{CM} | | 1.125 | 1.25 | 1.375 | V |
| Offset Voltage | V_{FSB} | Open circuit between - and + (see Note 3) | 100 | 112 | 125 | mV |
| Differential Terminator Impedance | Z_D | V_{OUT} Differential = -1V to 1V | 100 | 105 | 110 | Ω |
| Common Mode Impedance | Z_{CM} | 0V to 2.5V | 100 | 200 | 300 | Ω |
| Output Capacitance | C_O | LX5241/5243: DISCONNECT > 2.0V, LX5242: DISCONNECT < 0.8V | | 2.5 | | pF |
| Output Leakage | I_{LEAK} | LX5241/5243: DISCONNECT > 2.0V, LX5242: DISCONNECT < 0.8V, $V_{LINE} = 0$ to 4V, $T_A = 25^{\circ}\text{C}$ | | | 2 | μA |
| | | LX5241/5243: DISCONNECT > 2.0V, LX5242: DISCONNECT < 0.8V, $V_{TERM} = 0\text{V}$, $V_{LINE} = 2.7\text{V}$ | | 1 | | μA |
| Mode Change Delay | t_{DF} | DIFFSENSE = 1.4V to 0V | | 115 | | ms |
| DIFFSENSE Section | | | | | | |
| DIFFSENSE Output Voltage | V_{DIFF} | | 1.2 | 1.3 | 1.4 | V |
| DIFFSENSE Output Source Current | I_{DIFF} | $V_{DIFF} = 0\text{V}$ | 5.0 | | 15.0 | mA |
| DIFFSENSE Sink Current | $I_{SINK(DIFF)}$ | $V_{DIFF} = 2.75\text{V}$ | | | 200 | μA |
| DIFFSENSE Output Leakage | $I_{LEAK(DIFF)}$ | LX5241/5243: DISCONNECT > 2.0V, LX5242: DISCONNECT < 0.8V, $T_A = 25^{\circ}\text{C}$ | | | 10 | μA |
| Single-Ended Termination Section | | | | | | |
| Tempwr Supply Current | SE I_{CC} | All term lines = Open, Master/Slave = 0V | | 7 | 10 | mA |
| | | All term lines = 0.2V, Master/Slave = 0V | | 214 | 226 | mA |
| | | LX5241/5243: DISCONNECT > 2.0V, LX5242: DISCONNECT < 0.8V | | 15 | 35 | μA |
| Terminator Output High Volt | V_O | | 2.6 | 2.85 | | V |
| Output Current | I_O | $V_{OUT} = 0.2\text{V}$ | 21 | 23 | 24 | mA |
| Sink Current | I_{SINK} | $V_{OUT} = 4\text{V}$, All lines | 45 | 65 | | mA |
| Output Capacitance | C_O | LX5241/5243: DISCONNECT > 2.0V, LX5242: DISCONNECT < 0.8V | | 2.5 | | pF |
| Leakage Current | I_{LEAK} | LX5241/5243: DISCONNECT > 2.0V, LX5242: DISCONNECT < 0.8V, $V_{OUT} = 0$ to 4V, $T_A = 25^{\circ}\text{C}$ | | | 2 | μA |
| | | LX5241/5243: DISCONNECT > 2.0V, LX5242: DISCONNECT < 0.8V, $V_{TERM} = \text{Open}$, $V_{LINE} = 2.7\text{V}$, $T_A = 25^{\circ}\text{C}$ | | 1 | | μA |

Note 3. Open circuit failsafe voltage.

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ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Test Conditions | LX5241 / 5242 | | | Units |
|---|--------------|-----------------------|-------------------|------|------|--------------------|
| | | | Min. | Typ. | Max. | |
| Single-Ended Termination Section (continued) | | | | | | |
| Ground Driver Impedance | Z_G | $I = 1\text{mA}$ | | | 100 | Ω |
| Thermal Shutdown | | | | 150 | | $^{\circ}\text{C}$ |
| DISCONNECT Section | | | | | | |
| DISCONNECT Thresholds | V_{TH} | | 0.8 | | 2.0 | V |
| Input Current | LX5241/43 | I_{IL} | DISCONNECT = 0V | | 10 | μA |
| | LX5242 | I_{IL} | DISCONNECT = 0V | | 100 | nA |
| | LX5241/43 | I_{IH} | DISCONNECT = 2.4V | | 100 | nA |
| | LX5242 | I_{IH} | DISCONNECT = 2.4V | | 10 | μA |
| MASTER / SLAVE Section | | | | | | |
| MASTER / SLAVE Thresholds | $V_{TH(MS)}$ | | 0.8 | | 2.0 | V |
| Input Current | $I_{IL(MS)}$ | MASTER / SLAVE = 0V | | | 10 | μA |
| | $I_{IH(MS)}$ | MASTER / SLAVE = 2.4V | | 100 | | nA |

BLOCK DIAGRAM

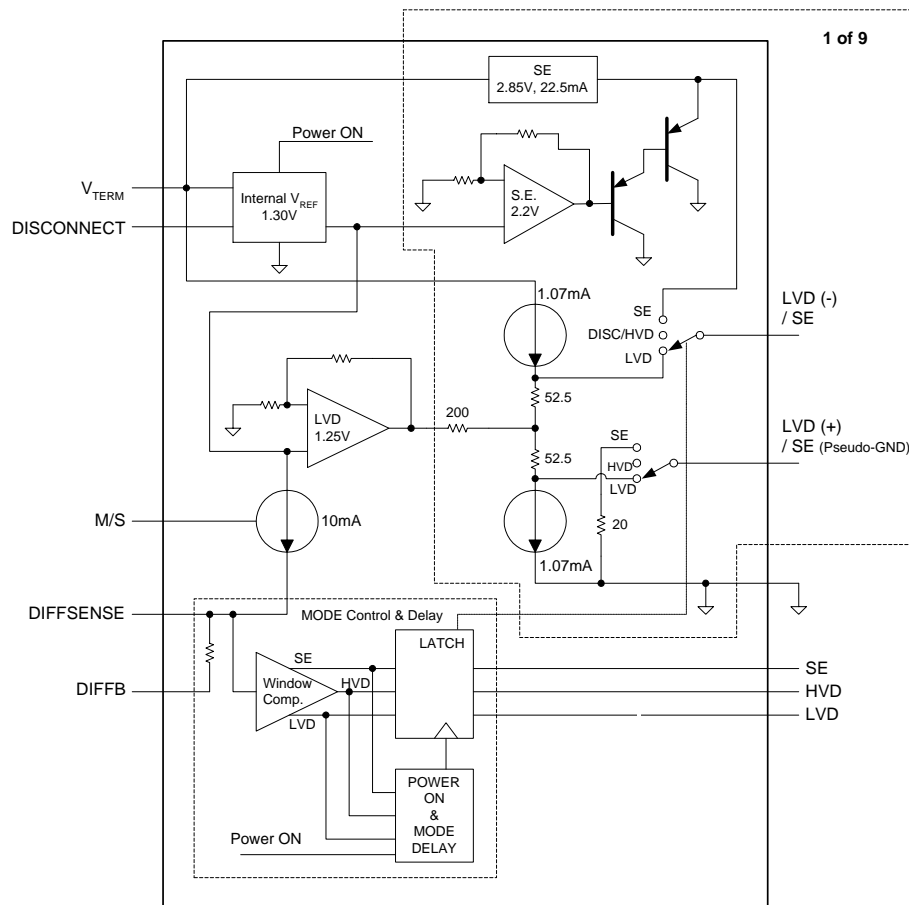


FIGURE 1 — LX5241/5242 Block Diagram

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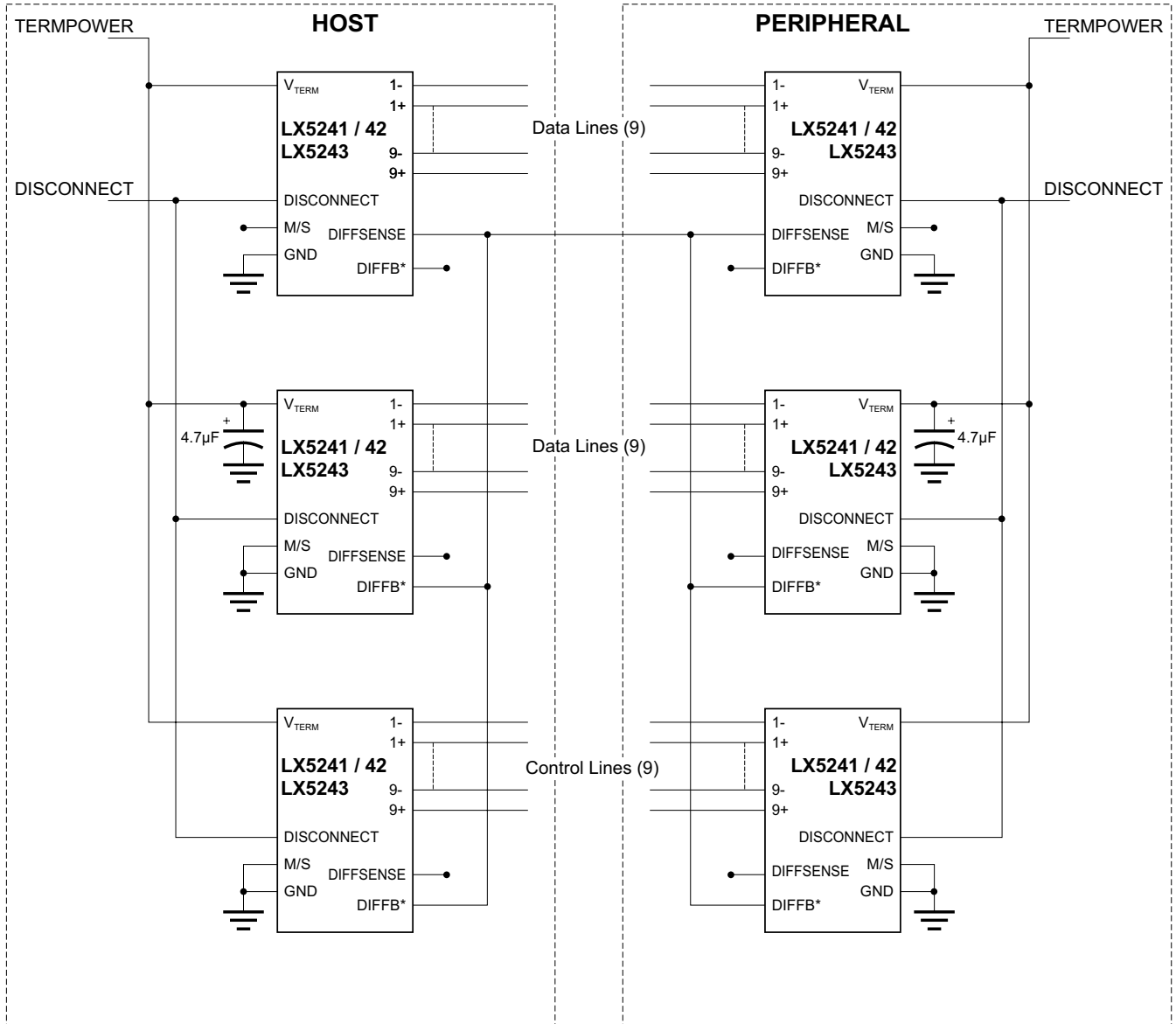
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FUNCTIONAL PIN DESCRIPTION

| Pin Designator | Description |
|-------------------------------------|--|
| 1-, 2-, 3-, 4-, 5-, 6-, 7-, 8-, 9-6 | Negative signal termination lines for LVD mode. Signal termination lines for SE mode. |
| 1+, 2+, 3+, 4+, 5+, 6+, 7+, 8+, 9+ | Positive signal termination lines for LVD mode. Pseudo-ground lines for SE mode. |
| V _{TERM} | Power supply pin for terminator. Connect to SCSI bus TERMPWR. Must be decoupled by one 4.7µF low-ESR capacitor for every three terminator devices. It is absolutely necessary to connect this pin to the decoupling capacitor through a very low impedance (big traces on PCB). Keeping distances very short from the decoupling capacitors to the V _{TERM} pin is also critical. The value of the decoupling capacitor is somewhat layout dependant and some applications may benefit from high-frequency decoupling with 0.1µF capacitors right at V _{TERM} pin. |
| DISCONNECT6 | Enables / disables terminator. See Power Down Function Table for logic levels per device. |
| GND6 | Terminator ground pin. Connect to ground. |
| MASTER / SLAVE6 | Sometimes referred to as M/S pin in this data sheet. Used to select which terminator is the controlling device. MASTER/SLAVE pin High or Open enables the DIFFSENSE output drive. Please see MASTER/SLAVE Function Table. |
| DIFFSENSE6 | This is a dual function pin. It drives the SCSI bus DIFFSENS line. It is also the sense pin to detect the SCSI bus mode (LVD, SE or HVD). DIFFSENSE output drive can be disabled with Low level on the MASTER/SLAVE pin. Please see DIFFSENSE and MASTER/SLAVE Function Tables. Internally connected to DIFFB pin through 20kOhm resistor. |
| DIFFB6 | Internally connected to DIFFSENSE pin through 20kOhm resistor. It can be used as a mode sense pin when the device is a non-controlling terminator (MASTER/SLAVE pin is Low). An RC filter (20kOhm / 0.1µF) is not required on the LX5241/42/43, as it has an internal timer. |
| SE6 | Single-ended output; when High, terminator is operating in SE mode. |
| LVD6 | Low Voltage Differential output. When High, terminator is operating in LVD mode. |
| HVD6 | High Voltage Differential output. When High, terminator is operating in HVD mode. |
| HEATSINK6 | Attached to die mounting pad, but not bonded to GND pin. Pins should be considered a heat sink only, and not a true ground connection. It is recommended that these pins be connected to ground, but can be left floating. |

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APPLICATION SCHEMATIC



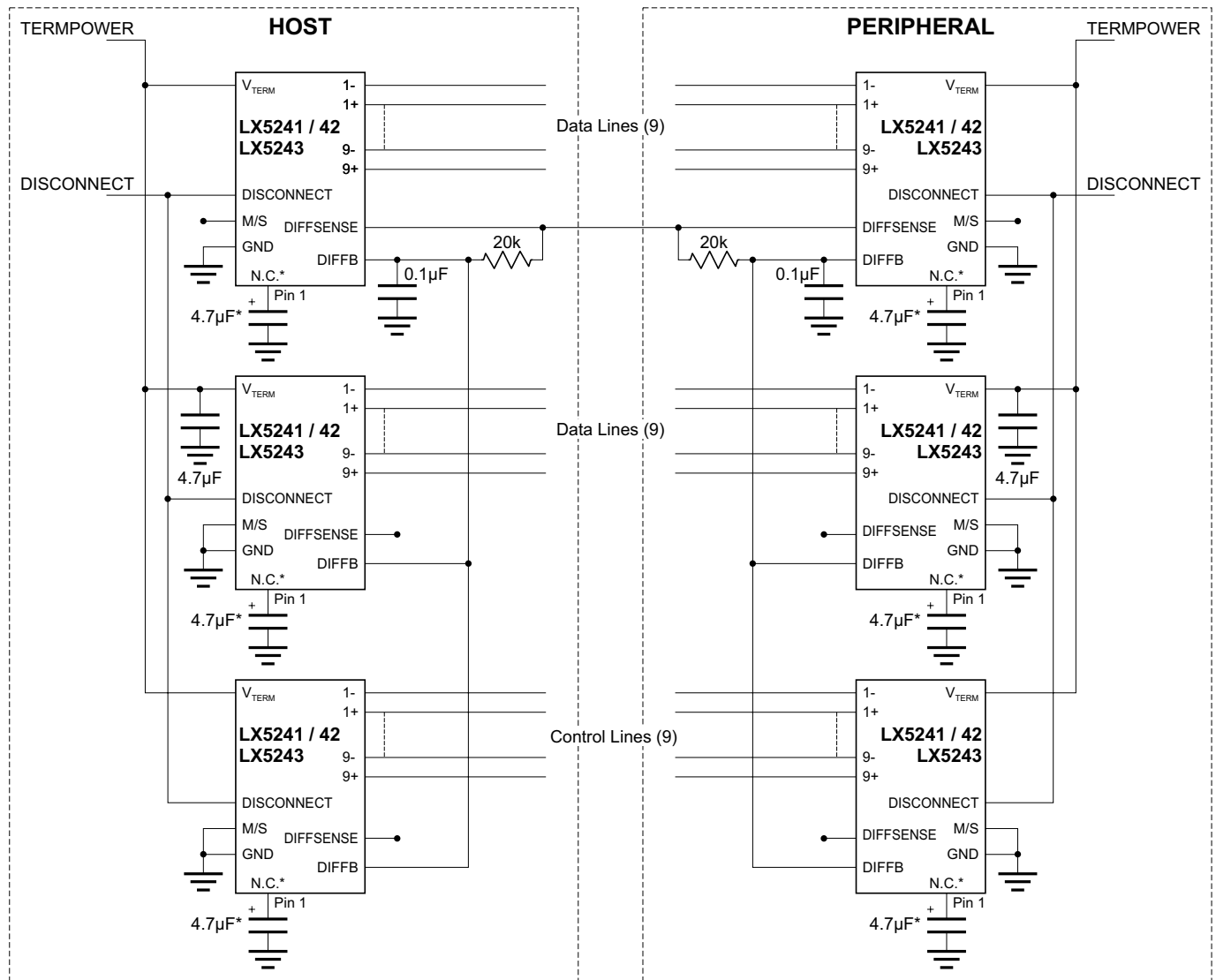
* DIFFB Pin not present on LX5241/5242 CPW Package . Must connect DIFFSENS signal to DIFFSENSE pin on PW package.

FIGURE 2 — Linfinity ONLY Application Schematic

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APPLICATION SCHEMATIC



* The capacitor on Pin 1 can be placed on the LX5241CDB, LX5242CDB or the LX5243CPW to be pin-compatible with other devices. This V_{REG}/REF capacitor is not required.

FIGURE 3 — Suggested Linfinity LX5241/5242/5243 Universal Application Schematic
(Please Reference Manufacturer's Current Data Sheet To Ensure Compatibility)

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