

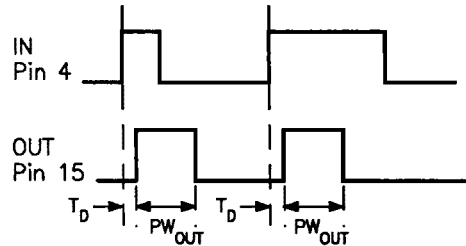
Single & Triple 10K / 10KH ECL Buffered Delay Modules

10K ECL Pulse Width Generator Modules

Electrical Specifications at 25°C

Delay Tolerance (ns)	ECL Buffered Single Delay Modules		ECL Buffered Triple Delay Modules	
	10K Part Number	10KH Part Number	10K Part Number	10KH Part Number
3 ± 0.5	FECL-3	FECLH-3	MECL-3	MECLH-3
4 ± 0.5	FECL-4	FECLH-4	MECL-4	MECLH-4
5 ± 0.5	FECL-5	FECLH-5	MECL-5	MECLH-5
6 ± 0.75	FECL-6	FECLH-6	MECL-6	MECLH-6
7 ± 0.75	FECL-7	FECLH-7	MECL-7	MECLH-7
8 ± 0.8	FECL-8	FECLH-8	MECL-8	MECLH-8
9 ± 1.0	FECL-9	FECLH-9	MECL-9	MECLH-9
10 ± 1.0	FECL-10	FECLH-10	MECL-10	MECLH-10
11 ± 1.0	FECL-11	FECLH-11	MECL-11	MECLH-11
12.5 ± 1.0	FECL-12.5	FECLH-12.5	MECL-12.5	MECLH-12.5
15 ± 1.5	FECL-15	FECLH-15	MECL-15	MECLH-15
20 ± 1.5	FECL-20	FECLH-20	MECL-20	MECLH-20
25 ± 1.5	FECL-25	FECLH-25	MECL-25	MECLH-25
30 ± 2.0	FECL-30	FECLH-30	MECL-30	MECLH-30
40 ± 2.0	FECL-40	FECLH-40	MECL-40	MECLH-40
50 ± 2.5	FECL-50	FECLH-50	MECL-50	MECLH-50
60 ± 3.0	FECL-60	FECLH-60	MECL-60	MECLH-60
75 ± 3.75	FECL-75	FECLH-75	MECL-75	MECLH-75
100 ± 5.0	FECL-100	FECLH-100	MECL-100	MECLH-100

Triggered by the input's rising edge (input pulse width 10 ns, min.), a pulse of specified width will be generated at the output with a propagation delay of 3 ± 1 ns. High-to-low transitions will not trigger the unit. Designed for output duty-cycle less than 50%.



Electrical Specifications at 25°C

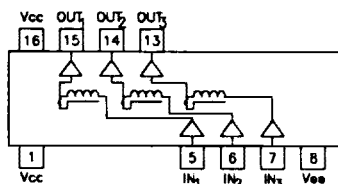
Output Pulse Width (ns)	ECL Buffered Pulse Width Generator Modules	
	Maximum Freq. (MHz)	Part Number
5 ± 1.00	77.0	ECLPWG-5
6 ± 1.00	67.0	ECLPWG-6
7 ± 1.00	59.0	ECLPWG-7
8 ± 1.00	53.0	ECLPWG-8
9 ± 1.00	48.0	ECLPWG-9
10 ± 1.50	43.0	ECLPWG-10
11 ± 1.50	40.0	ECLPWG-11
12 ± 1.50	37.0	ECLPWG-12
15 ± 2.00	31.0	ECLPWG-15
20 ± 2.00	23.0	ECLPWG-20
25 ± 2.00	19.0	ECLPWG-25
30 ± 2.00	15.0	ECLPWG-30
40 ± 2.00	11.0	ECLPWG-40
45 ± 2.25	10.0	ECLPWG-45
50 ± 2.50	9.0	ECLPWG-50
60 ± 3.00	8.0	ECLPWG-60
75 ± 3.75	6.5	ECLPWG-75
100 ± 5.00	5.0	ECLPWG-100

GENERAL: For Operating Specifications and Test Conditions, see Tables IV, V and VIII on page 7 of this catalog. Delays specified for the Leading Edge.

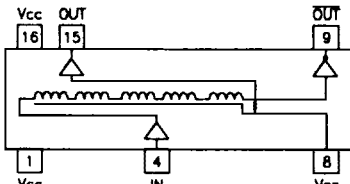
Minimum Input Pulse Width, FECL..... 40% of total delay
 Minimum Input Pulse Width, MECL..... 100% of total delay
 Temperature Coefficient 300ppm/°C typical
 Supply Current, I_{EE}, FECL, ECLPWG 40 mA typ., 65 mA max.
 Supply Current, I_{EE}, MECL..... 85 mA typ., 105 mA max.

MIL-GRADE: These Military Grade delay lines use integrated circuits screened to MIL-STD-883B with an operating temperature range of -55 to +125°C. Part numbers will have the suffix "M": FECL-XXXM, MECL-XXXM, and ECLPWG-XXXM. These MIL devices will have larger package height; consult factory for detailed data sheet.

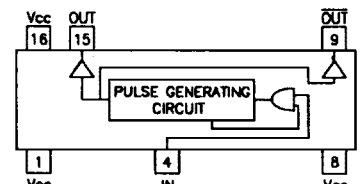
MECL Schematic



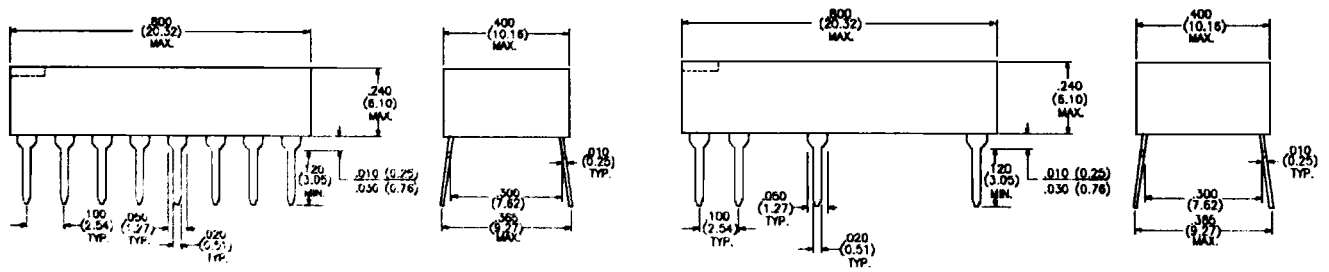
FECL Schematic



ECLPWG Schematic



Physical Dimensions: inches (mm)



VARIATIONS AVAILABLE. FOR INTERMEDIATE VALUES AND/OR CUSTOM DESIGNS PLEASE CONSULT THE FACTORY.

Specifications subject to change without notice.

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