FLASH MEMORY

1. OUTLINE

The FLASH MEMORY CARD series is made up of Flash Memory chips. The FLASH MEMORY CARD can erase data at once by electricity. Memory capacity is from 128K Bytes to 1M Bytes. IE series is 8 bit wide data bus.

2. VARIATION

Part Number	Memory Size	Description
FEC032IEC0	32K Byte	32K × 8 bit CMOS FLASH Memory CARD (RAM CARD Configuration)
FEC064IEC0	64K Byte	64K × 8 bit CMOS FLASH Memory CARD (RAM CARD Configuration)
FEC128IEC0	128K Byte	128K × 8 bit CMOS FLASH Memory CARD (RAM CARD Configuration)
FEC256IEC0	256K Byte	256K × 8 bit CMOS FLASH Memory CARD (RAM CARD Configuration)
FEC512IEC0	512K Byte	512K × 8 bit CMOS FLASH Memory CARD (RAM CARD Configuration)
FEC100IEC0	1M Byte	1M × 8 bit CMOS FLASH Memory CARD (RAM CARD Configuration)
FPC032IEC0	32K Byte	32K × 8 bit CMOS FLASH Memory CARD (ROM CARD Configuration)
FPC064IEC0	64K Byte	64K × 8 bit CMOS FLASH Memory CARD (ROM CARD Configuration)
FPC128IEC0	128K Byte	128K × 8 bit CMOS FLASH Memory CARD (ROM CARD Configuration)
FPC256IEC0	256K Byte	256K × 8 bit CMOS FLASH Memory CARD (ROM CARD Configuration)
FPC512IEC0	512K Byte	512K × 8 bit CMOS FLASH Memory CARD (ROM CARD Configuration)
FPC100IEC0	1M Byte	1M × 8 bit CMOS FLASH Memory CARD (ROM CARD Configuration)

3. SIZE

(1) Size : 54.0 ±0.1 mm wide by 86.0 ±0.2 mm long by 2.4 ±0.15 mm thick
(2) Thickness at the contacts : 1.80 ±0.15 mm
(3) Card Type : 40 pin Card Edge

4. FEATURES

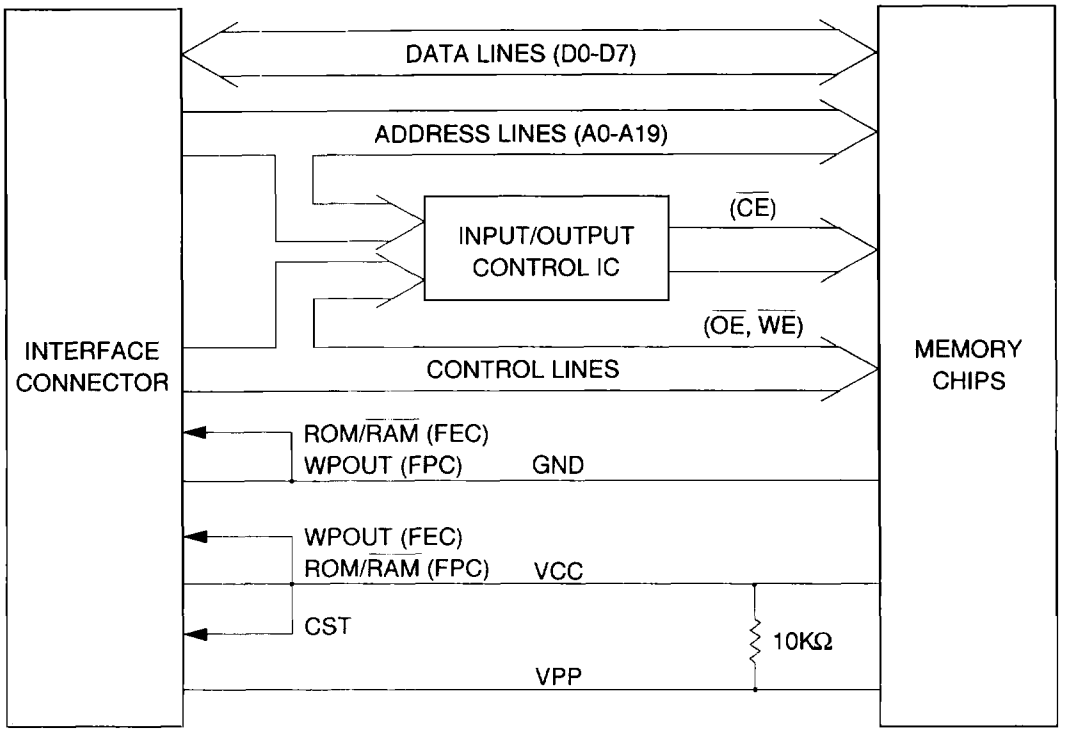
(1) Shutter Mechanism

This mechanism protects the terminals from dirt, static electricity, hand contact, etc. The shutter is opened by tabs on the connector during insertion, and is closed by built in springs when the card is removed from the connector.
(Our connector is required to operate this feature.)

(2) Polarization of the connector to the card

The memory card and our connector have a mechanism to safeguard against incorrect insertion. This mechanism protects the circuits of the unit, the connector, and the card from potential damage.

5. BLOCK DIAGRAM



(1) D0 to D7

Data input/output, 8 bit wide

(2) A0 to A19

Address inputs
Unused address lines should be "no connect".

(3) CE

Card Enable input (Active HIGH)
Memory card operates when CE is "HIGH".

(4) $\overline{OE}$

Output Enable input (Active LOW)
Memory card output data when $\overline{OE}$ is "LOW".

(5) $\overline{WE}$

Write Enable input (Active LOW)
Memory card input data when $\overline{WE}$ is "LOW".

(6) WPOUT*

FEC : This line is connected to VCC line.
FPC : This line is connected to GND line.

(7) CST*

Output line to indicate that the card is accessible or not.

This line is connected to VCC line.

(8) ROM/$\overline{RAM}$*

VCC level indicates ROM: OTP, MASKROM, FLASH MEMORY (FPC)
GND level indicates RAM: SRAM, EEPROM, FLASH MEMORY (FEC)

(9) VPP

Power supply voltage required to write data to the card.
VPP: + 12.00 V
Connected to VCC through a 10K ohm resister.

(10) VCC

Power source : +5 V ±10%

(11) GND

Ground

Note: See the recommended interface circuit.
* Do never use as VCC or GND line.

6. ELECTRICAL CHARACTERISTICS

6–1. ABSOLUT MAXIMUM RATING

Symbol	Description		Maximum Rating	Unit
V_{CC}	V_{CC} Power supply		–0.5 to 7.0	V
V_{PP}	V_{PP} power supply		–0.5 to 14.0	V
V_{IN}	Input Voltage	(1)	–0.5 to V_{CC}+0.5	V
V_{OUT}	Output Voltage		–0.5 to V_{CC}	V
T_{OP}	Operating Temperature		0 to 60	°C
T_{STG}	Storage Temperature		–20 to 60	°C
H_{STG}	Storage humidity	(2)	0 to 65	%
PD	Power dissipation		1	W

Note: (1) V_{IN} should be under 7.0 V.
(2) No dew condition

6–2. CAPACITANCE (Ta = 25°C, f = 1 MHz)

Symbol	Variation	Item	Condition	Min	Typ	Max	Unit
C1	FEC032IEC0 FPC032IEC0	A0 to A14, OE CE	V_{IN} = 0 V	—	14	20	pF
	FEC064IEC0 FPC064IEC0	A0 to A14, OE		—	20	24	pF
		A15, CE		—	14	20	pF
	FEC128IEC0 FPC128IEC0	A0 to A16, OE, WE CE		—	14	20	pF
	FEC256IEC0 FPC256IEC0	A0 to A16, OE, WE		—	20	24	pF
		A17, CE		—	14	20	pF
	FEC512IEC0 FPC512IEC0	A0 to A16, OE, WE		—	40	48	pF
		A17, A18, CE		—	14	20	pF
	FEC100IEC0 FPC100IEC0	A0 to A17, OE, WE		—	40	48	pF
		A18, A19, CE		—	14	20	pF

CAPACITANCE (Ta = 25°C, f = 1 MHz) (6–2. Con't)

Symbol	Variation	Item	Condition	Min	Typ	Max	Unit
C2	FEC032IEC0 FPC032IEC0 FEC128IEC0 FPC128IEC0	D0 to D7	VIN/VOUT = 0 V	—	12	16	pF
	FEC064IEC0 FPC064IEC0 FEC256IEC0 FPC256IEC0			—	24	32	pF
	FEC512IEC0 FPC512IEC0 FEC100IEC0 FPC100IEC0			—	48	64	pF

6–3. DC RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Min	Typ	Max	Unit
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{PP}	Program voltage (READ)	4.75	5.0	5.25	V
V_{PP}	Program voltage (WRITE, ERASE)	11.75	12.00	12.25	V
V_{IH}	High input voltage	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V
V_{IL}	Low input voltage	–0.3	—	$V_{CC} \times 0.1$	V

6–4. DC ELECTRICAL CHARACTERISTICS
(Ta = 0 to 60°C, V_{CC} = 5 V ±10%)

Symbol	Description	Note	Condition	Min	Ttp	Max	Unit
V_{OH}	High level output voltage	1	I_{OH} = –400 uA	2.4	—	—	V
V_{OL}	Low level output voltage	1	I_{OL} = 1.0 mA	—	—	0.4	V
I_{LI}	Input leakage current	2	V_{IN} = 0 V or V_{CC}	–10	—	10	µA
I_{LO}	Output leakage current	1	CE = V_{IL} or OE = V_{IH}, V_{OUT} = 0 V or V_{CC}	–10	—	10	µA
I_{ACT}	Active current	3	CE = V_{CC} –0.4 V OTHER INPUTS = 0.4 V/ V_{CC} –0.4V				
			FEC032IEC0, FPC032IEC0	—	—	40	mA
			FEC064IEC0, FPC064IEC0	—	—	40	mA
			FEC128IEC0, FPC128IEC0	—	—	35	mA
			FEC256IEC0, FPC256IEC0	—	—	35	mA
			FEC512IEC0, FPC512IEC0	—	—	35	mA
			FEC100IEC0, FPC100IEC0	—	—	35	mA
I_{STB}	Standby current	3	CE = 0.4 V OTHER INPUTS = 0.4 V/ V_{CC} –0.4 V				
			FEC032IEC0, FPC032IEC0	—	—	1	mA
			FEC064IEC0, FPC064IEC0	—	—	1	mA
			FEC128IEC0, FPC128IEC0	—	—	1	mA
			FEC256IEC0, FPC256IEC0	—	—	1	mA
			FEC512IEC0, FPC512IEC0	—	—	1	mA
			FEC100IEC0, FPC100IEC0	—	—	1	mA

DC ELECTRICAL CHARACTERISTICS (6–4. Con't)
(Ta = 0 to 60°C, V_{CC} = 5 V ±10%)

Symbol	Description	Note	Condition	Min	Typ	Max	Unit
I_{PP}	Program current (V_{PP} = 13 V)	3	CE = V_{CC} –0.4 V OTHER INPUTS = 0.4 V/ V_{CC} –0.4 V				
			FEC032IEC0, FPC032IEC0	—	—	50	mA
			FEC064IEC0, FPC064IEC0	—	—	50	mA
			FEC128IEC0, FPC128IEC0	—	—	35	mA
			FEC256IEC0, FPC256IEC0	—	—	35	mA
			FEC512IEC0, FPC512IEC0	—	—	35	mA
			FEC100IEC0, FPC100IEC0	—	—	35	mA
I_{EC}	Erase current (V_{PP} = 13 V)	3	CE = V_{CC} –0.4 V OTHER INPUTS = 0.4 V/ V_{CC} –0.4 V				
			FEC032IEC0, FPC032IEC0	—	—	50	mA
			FEC064IEC0, FPC064IEC0	—	—	50	mA
			FEC128IEC0, FPC128IEC0	—	—	35	mA
			FEC256IEC0, FPC256IEC0	—	—	35	mA
			FEC512IEC0, FPC512IEC0	—	—	35	mA
			FEC100IEC0, FPC100IEC0	—	—	35	mA

Notes: 1. D0 to D7
2. A0 to A19, $\overline{OE}$, $\overline{WE}$, CE
3. D0 to D7, CST = No Load

6–5. VPP RESISTANCE
(Ta = 0 to 60°C)

Symbol	Description	Min	Typ	Max	Unit
RVPP	VPP RESISTANCE	9	10	11	KΩ

6–6. OPERATING MODES–1
(CARD TYPE : FEC032IEC0, FPC032IEC0, FEC064IEC0, FPC064IEC0)

Mode	CE	OE	VPP	VCC	D0 to D7	A9/ERA	CST
READ	VIH	VIL	5 V	5 V	DATA OUTPUT	*	HO
DISABLE	VIH	VIH	5 V	5 V	HZ	*	HO
STANDBY	VIL	*	5 V	5 V	HZ	*	HO
PROGRAM	VIH	VIH	12.75	6.25 V	DATA INPUT	*	HO
PGRM INHIB.	VIL	VIH	12.75	6.25 V	HZ	*	HO
PGRM VER.*	VIL	VIL	12.75	6.25 V	DATA OUTPUT	*	HO
CHIP ERASE	VIH	VIH	12.75	5 V	*	12.75 V	HO
ERASE INHIB.	VIL	*	12.75	5 V	HZ	12.75 V	HO

Note: *: Do never "program verify" at FEC064IEC0 and FPC064IEC0

6–7. OPERATING MODES–2
(CARD TYPE : FEC128IEC0, FEC256IEC0, FEC512IEC0, FEC100IEC0, FPC128IEC0, FPC256IEC0, FPC512IEC0, FPC100IEC0)

Mode	CE	OE	WE	VPP	VCC	D0 to D7	CST
READ	VIH	VIL	VIH	5 V	5 V	DATA OUTPUT	HO
DISABLE	VIH	VIH	VIH	5 V	5 V	HZ	HO
STANDBY	VIL	*	*	5 V	5 V	HZ	HO
READ	VIH	VIL	VIH	12 V	5 V	DATA OUTPUT	HO
DISABLE	VIH	VIH	VIH	12 V	5 V	HZ	HO
STANDBY	VIL	*	*	12 V	5 V	HZ	HO
WRITE	VIH	VIH	VIL	12 V	5 V	DATA OUTPUT	HO

Notes: * : VIH or VIL
HZ : High Impedance
HO : Output VCC level

6–8. JEDEC ELECTRIC SIGNATURE MODE

Variation	Manufacturer Code (A0 = VIL)	Device Code (A0 = VIH)
	HEX	HEX
FEC032IEC0 FEC064IEC0 FPC032IEC0 FPC064IEC0	98	A4
FEC128IEC0 FEC256IEC0 FEC512IEC0 FPC128IEC0 FPC256IEC0 FPC512IEC0	89	B4
FEC100IEC0 FPC100IEC0	89	BD

6–9. COMMAND DEFINITIONS
(CARD TYPE : FEC128IEC0, FEC256IEC0, FEC512IEC0, FEC100IEC0, FPC128IEC0, FPC256IEC0, FPC512IEC0, FPC100IEC0)

Command	Bus Cycles req'd	First Bus Cycle			Second Bus Cycle		
		(1) Operation	(2) Address	(3) Data	(1) Operation	(2) Address	(3) Data
Read Memory	1	Write	RA	00H			
Read Identifier Codes (4)	3	Write	*	90H	Read	IA	ID
Set-up Erase /Erase	2	Write	EA	20H	Write	EA	20H
Erase Verify	2	Write	EVA	A0H	Read	EVA	EVD
Set-up Program /Program	2	Write	PA	40H	Write	PA	PD
Program Verify	2	Write	PA	C0H	Read	PA	PVD
Reset (5)	2	Write	*	FFH	Write	*	FFH

Notes: (1) Bus operations are defined in operation mode.

(2) IA = Identifier address : 00H for manufacturer code.
01H for device code.

EA = Address of memory location to be erased.

EVA = Address of memory location to be read during erase verify.

PA = Address of memory location to be programmed.

RA = Address of memory location to be read.

Address are latched on the falling edge of the Write-Enable pulse.

(3) ID = Data read from location IA during device identification.
(Manufacturer = 89H, Device = B4H or H)

EVD = Data read from location EA during erase verify.

PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.

PVD = Data read from location PA during program verify. PA is latched on the program command.

(4) Following the Read inteligent ID command, two read operations access manufacturer and device codes.

(5) The second bus cycle must be followed by the desired command register write.

6–10. AC ELECTRICAL CHARACTERISTICS AT READ (Ta = 0 to 60°C, VCC = 5 V ±10%)

Symbol	Item	Type 1		Type 2		
		Min	Max	Min	Max	Unit
tRC	Read cycle time	220	—	270	—	ns
tACC	Address access time	—	200*	—	250***	ns
tCE	CE access time	—	220	—	270	ns
tOE	OE access time	—	120	—	100	ns
tCOE	CE to output enable time	10	—	10	—	ns
tOEE	OE to output enable time	10	—	10	—	ns
tOD	CE to output disable time	—	120	—	90	ns
tODO	OE to output disable time	—	120	—	90	ns
tOH	Data hold time	0**	—	0****	—	ns

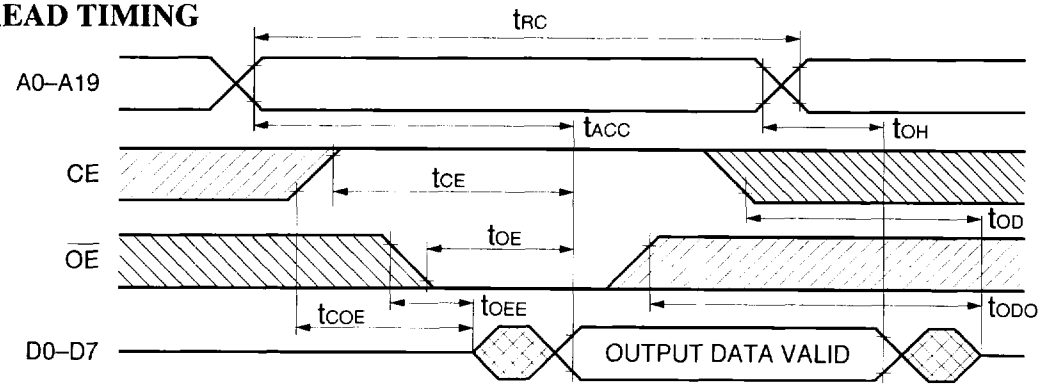
Type 1: FEC128, FEC256, FEC512, FEC100
FPC128, FPC256, FPC512, FPC100
Type 2: FEC032, FEC064
FPC032, FPC064

Note: * : 220 ns at FEC256, FEC512, FEC100, FPC256, FPC512, FPC100
** : 20 ns at FEC256, FEC512, FEC100, FPC256, FPC512, FPC100
*** : 270 ns at FEC064, FPC064
**** : 20 ns at FEC064, FPC064

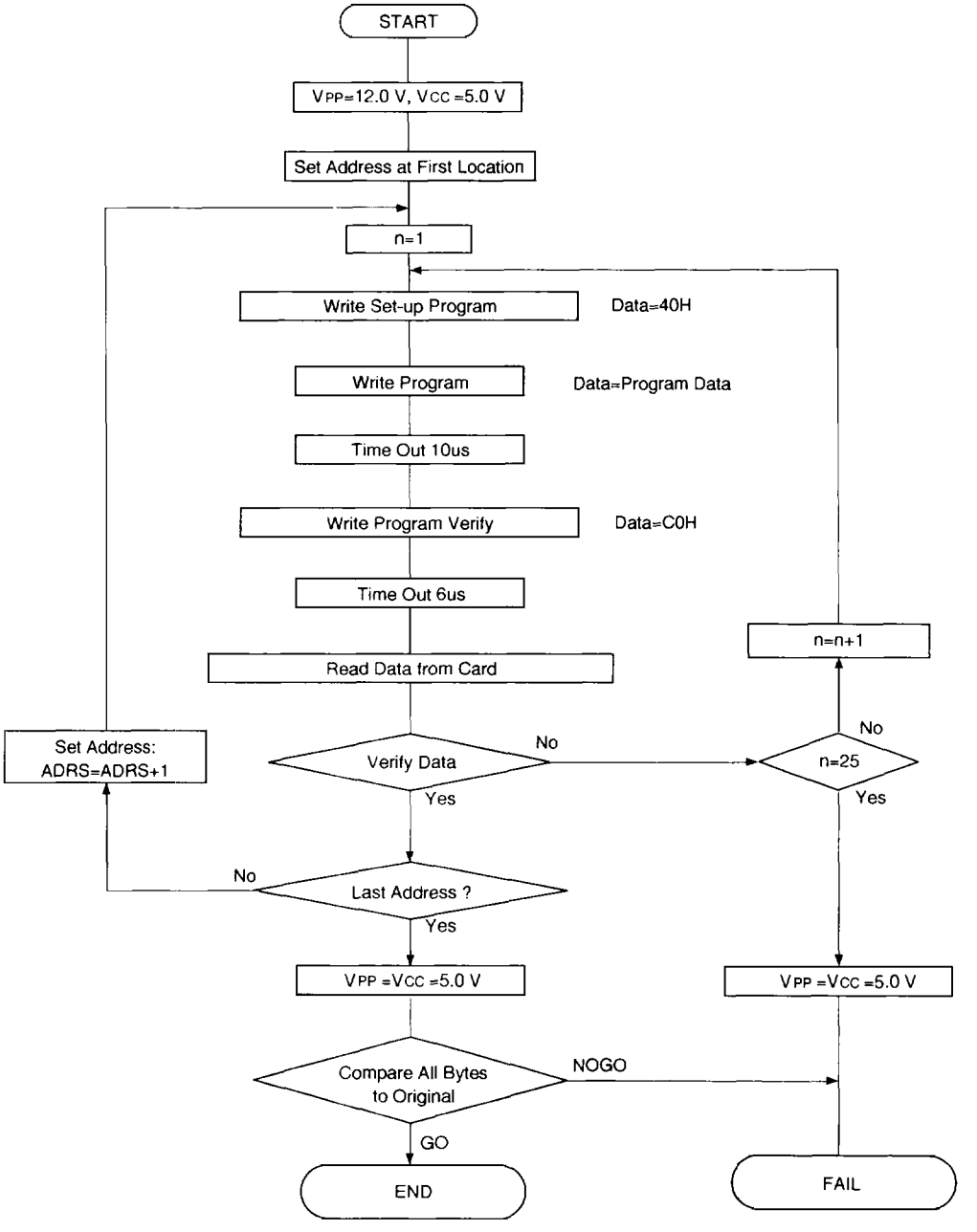
<< AC test conditions >>

Input Rise And Fall Times	20 ns
Input Pulse Levels	0.4 V, 2.4 V
Input Timing Reference Level	0.6 V, 2.2 V
Output Timing Reference Level	0.6 V, 2.2 V
Output Load	100 pF + 1 TTL GATE (include jig)

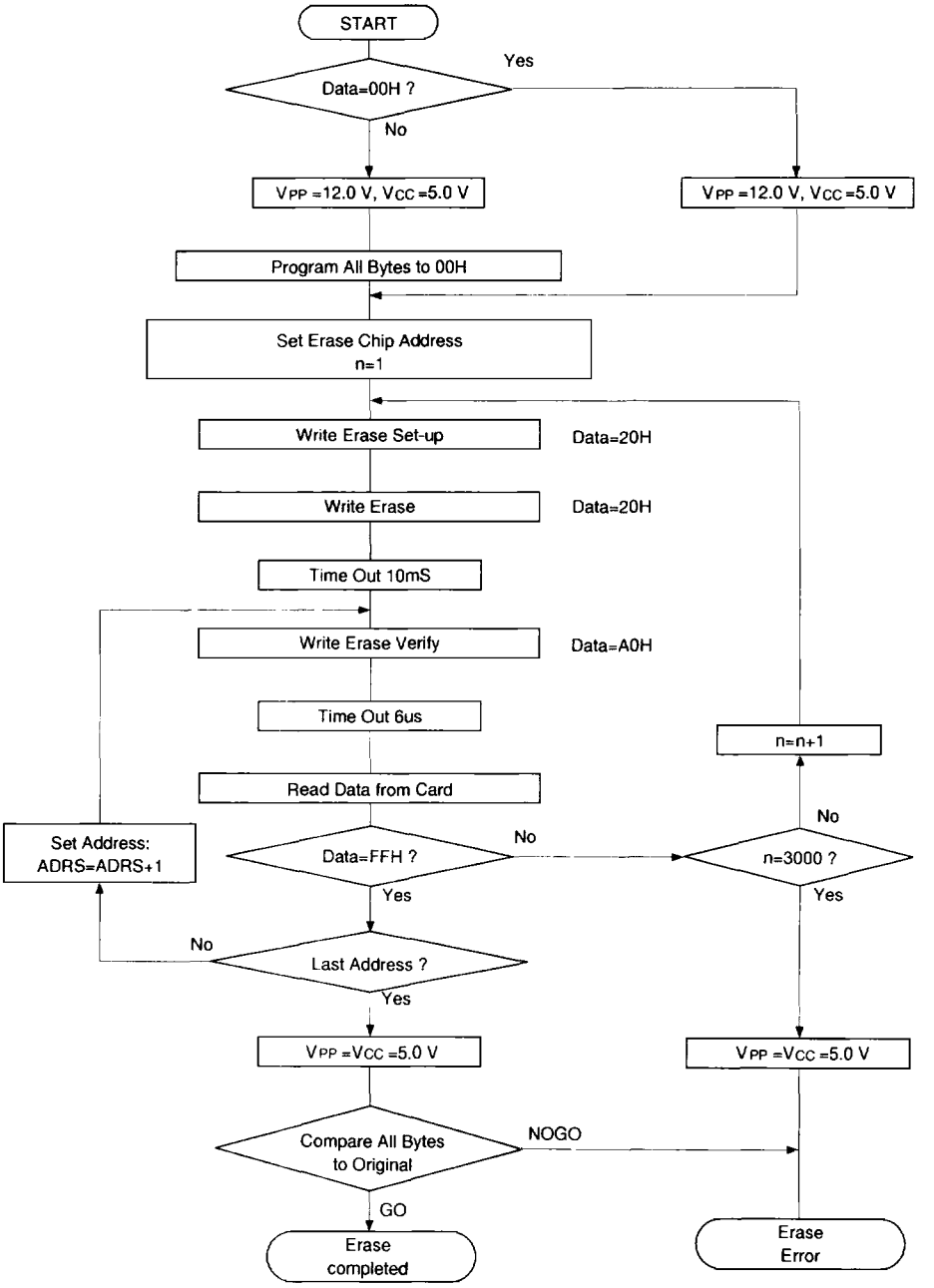
READ TIMING



6–11. PROGRAMMING FLOW CHART : CARD TYPE 1.
(CARD TYPE : FEC128IEC0, FPC128IEC0, FEC256IEC0, FPC256IEC0, FEC512IEC0, FPC512IEC0, FEC100IEC0,FPC100IEC0)



6–12. REASE FLOW CHART : CARD TYPE 1.
(CARD TYPE : FEC128IEC0, FPC128IEC0, FEC256IEC0, FPC256IEC0, FEC512IEC0, FPC512IEC0, FEC100IEC0, FPC100IEC0)



6–13. AC ELECTRICAL CHARACTERISTICS AT WRITE/ERASE : CARD TYPE 1.

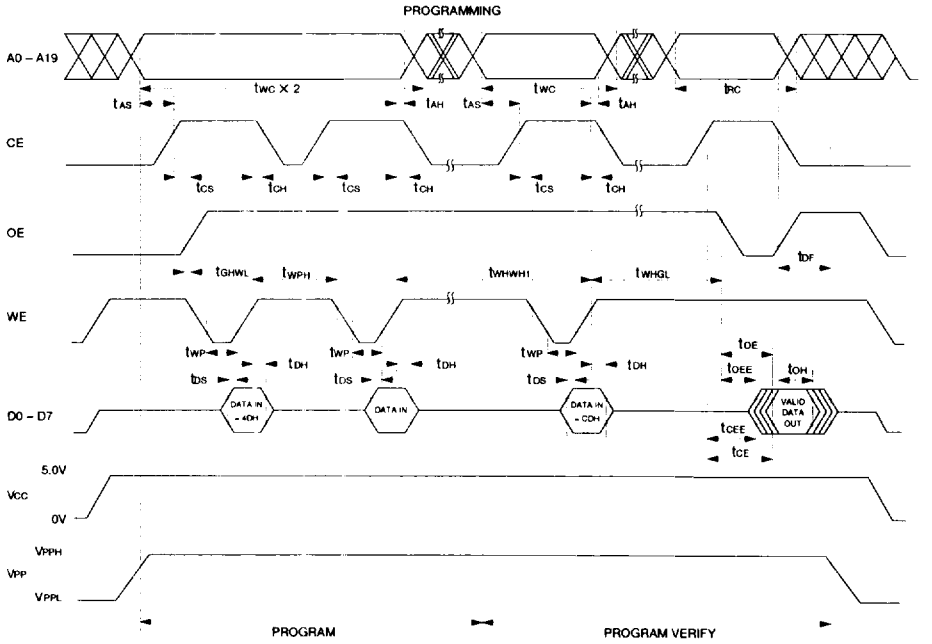
(V_{CC} = 5 ±0.25 V, V_{PP} = 12.0 ±0.25 V, Ta = 25 ±5°C)

Symbol	Item	Min	Max	Unit
t_{AS}	Address set up time	0	—	ns
t_{AH}	Address hold time	75	—	ns
t_{DS}	Data set up time	50	—	ns
t_{DH}	Date hold time	10	—	ns
t_{WC}	Write cycle time	220	—	ns
t_{CS}	CE set up time before write	40	—	ns
t_{CH}	CE hold time	0	—	ns
t_{WP}	Write pulse width	60	—	ns
t_{WHGL}	Write recovery time before read	6	—	µs
t_{GHWL}	Read recovery time before write	0	—	µs
t_{WPH}	Write pulse width high	20	—	ns
t_{WHWH1}	Duration of programming operation	10	25	µs
t_{WHWH2}	Duration of erase operation	9.5	10.5	ms
Erase/Write Cycles		100	—	cycles

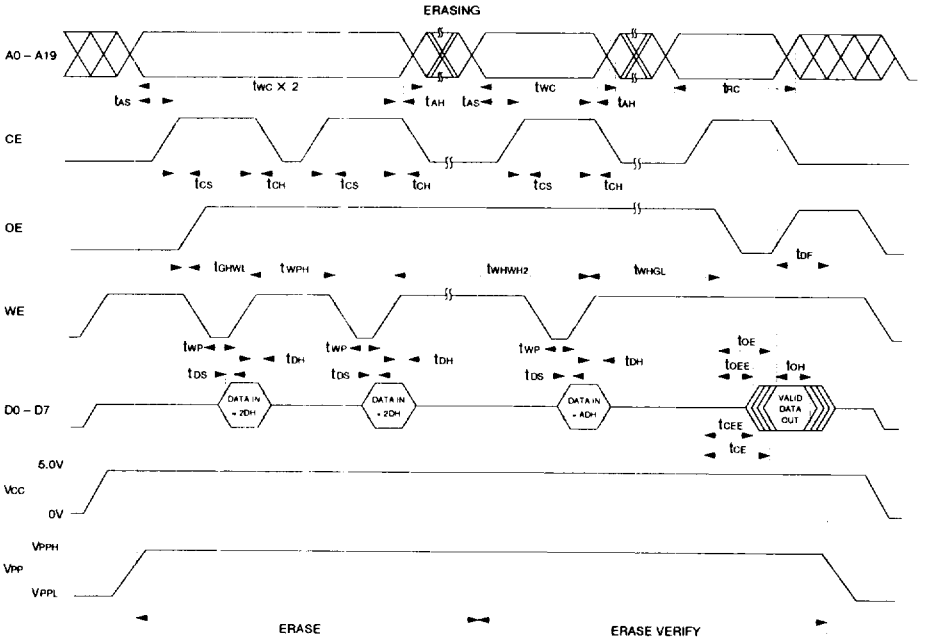
<< AC test conditions >>

Input Rise And Fall Times	20 ns
Input Pulse Levels	0.4 V, 2.4 V
Input Timing Reference Level	0.6 V, 2.2 V
Output Timing Reference Level	0.6 V, 2.2 V
Output Load	100 pF + 1 TTL GATE (include jig)

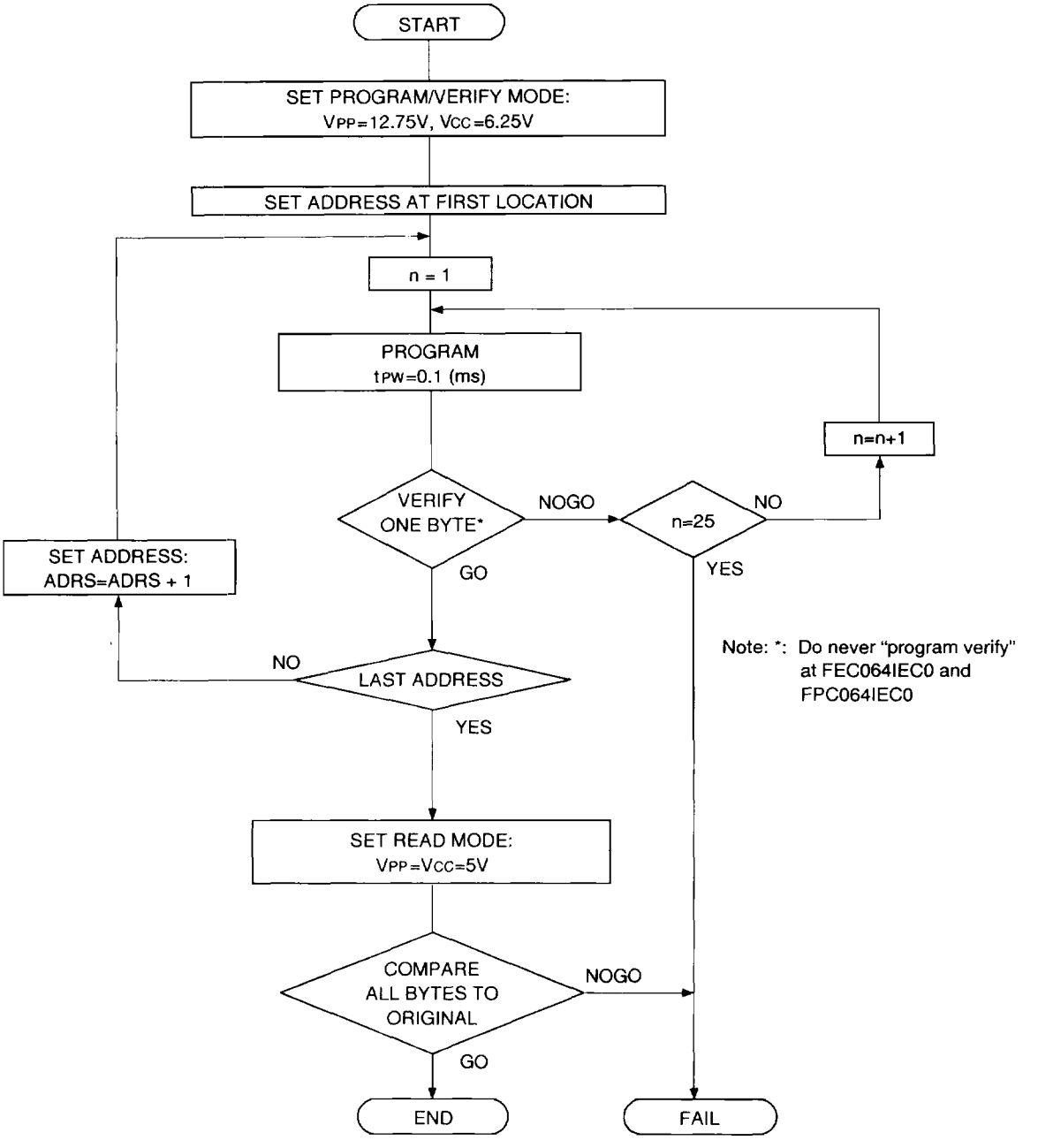
TIMING DIAGRAM AT WRITE (6–13. Con't)



TIMING DIAGRAM AT ERASE (6–13. Con't)



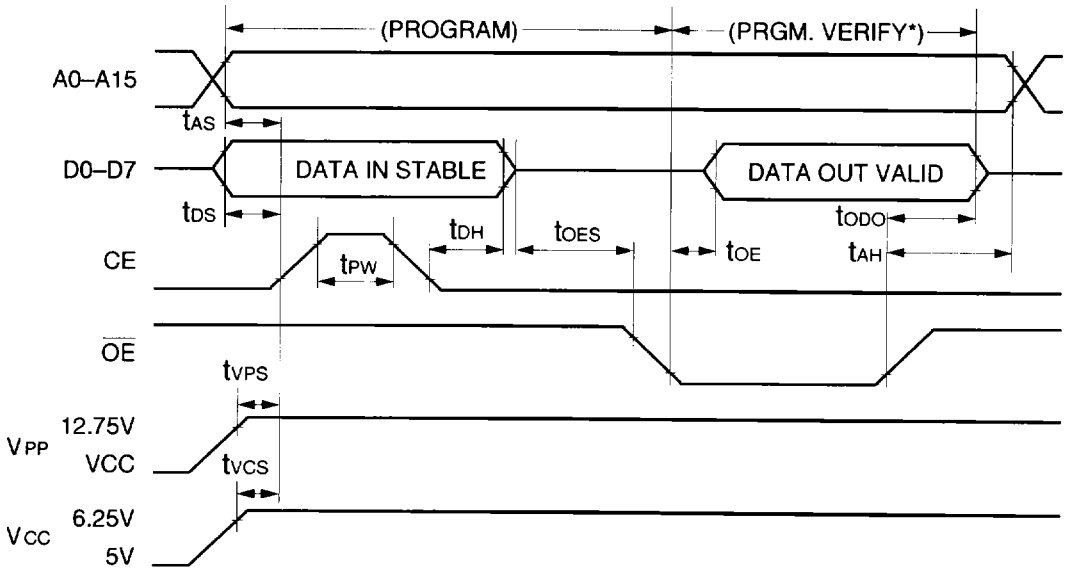
6–14. PROGRAMMING FLOW CHART : CARD TYPE 2 (CARD TYPE : FEC032IEC0, FPC032IEC0, FEC064IEC0, FPC064IEC0)



6–15. AC ELECTRICAL CHARACTERICSTICS AT WRITE : CARD TYPE 2 (V_{CC} = 6.25 ±0.25 V, V_{PP} = 12.75 ±0.25 V, Ta = 25 ±5°C)

Symbol	Item	Min	Typ	Max	Unit
t_{AS}	Address set up time	2	—	—	µs
t_{OES}	OE set up time	2	—	—	µs
t_{DS}	Data set up time	2	—	—	µs
t_{AH}	Address hold time	2	—	—	µs
t_{DH}	Data hold time	2	—	—	µs
t_{VPS}	V_{PP} set up time	2	—	—	µs
t_{VCS}	V_{CC} set up time	2	—	—	µs
t_{PW}	Write pulse width	0.095	0.1	0.105	ms
t_{OE}	OE to output enable time	—	—	100	µs
t_{ODO}	OE disable time	—	—	90	µs

TIMING DIAGRAM

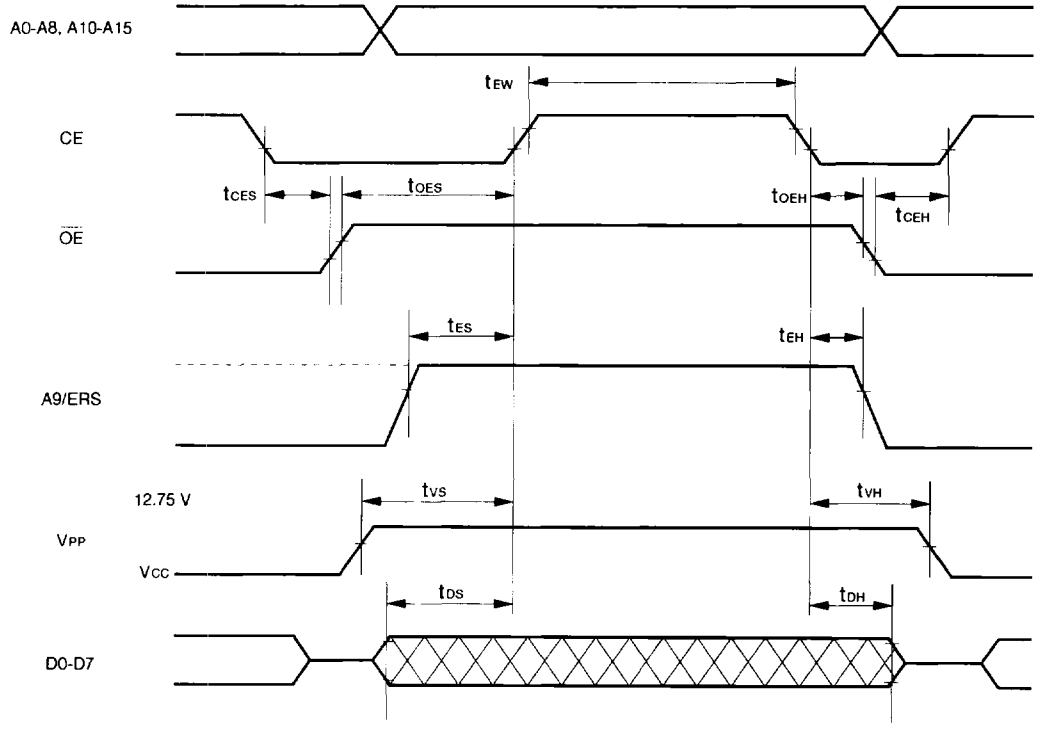


Note: *: Do never "program verify" at FEC064IEC0 and FPC064IEC0

6–16. AC ELECTRICAL CHARACTERICSTICS AT ERASE: CARD TYPE 2. (V_{CC} = 5 ±0.25 V, V_{PP} = 12.75 ±0.25 V, A9/ERA = 12.75 ±0.25 V, Ta = 25 ±5°C)

Symbol	Item	Min	Typ	Max	Unit
t_{CES}	CE set up time	2	—	—	µs
t_{CEH}	CE hold time	2	—	—	µs
t_{DS}	Data set up time	2	—	—	µs
t_{DH}	Data hold time	500	—	—	µs
t_{OES}	OE set up time	2	—	—	µs
t_{OEH}	OE hold time	500	—	—	µs
t_{VS}	V_{PP} set up time	2	—	—	µs
t_{VH}	V_{PP} hold time	500	—	—	µs
t_{EW}	Erase pulse width	0.95	1	1.05	µs
t_{ES}	A9/ERS set up time	2	—	—	µs
t_{EH}	A9/ERS hold time	2	—	—	µs

TIMING DIAGRAM



6–17. PROGRAMMING & ERASE NOTIFICATIONS

(1) The voltage applied to VPP must be later than or at the same time as VCC is applied. Also, VPP should be removed earlier than or at the same time as VCC.

(2) The card should never be inserted or extracted when VPP = 12.0 V is applied, or the card could be damaged.

(3) The voltage level applied to VPP should never be more than maximum ratings.

(4) The voltage level at VPP should never be changed when CE = VIH.

ERASE NOTIFICATIONS

(1) The card's erase block is each chips.

(2) The erase block is as follows.

FEC032IEC0, FPC032IEC0 FEC064IEC0, FPC064IEC0	32 KB
FEC128IEC0, FPC128IEC0 FEC256IEC0, FPC256IEC0 FEC512IEC0, FPC512IEC0	128 KB
FEC100IEC0, FPC100IEC0	256 KB

7. PIN ASSIGNMENT

Pin #	Name	Pin #	Name
1	VCC	21	CE
2	VPP	22	OE
3	A0	23	D0
4	A1	24	D1
5	A2	25	D2
6	A3	26	D3
7	A4	27	D4
8	A5	28	D5
9	A6	29	D6
10	A7	30	D7
11	A8	31	A17*
12	A9	32	A18*
13	A10	33	A19*
14	A11	34	N/C
15	A12	35	N/C
16	A13	36	N/C
17	A14*	37	WPOUT
18	A15*	38	CST
19	A16*	39	ROM/RAM
20	WE**	40	GND

Notes: *A14 : 32KB, 64KB, 128KB, 256KB, 512KB, 1MB
*A15 : 64KB, 128KB, 256KB, 512KB, 1MB
*A16 : 128KB, 256KB, 512KB, 1MB
*A17 : 256KB, 512KB, 1MB
*A18 : 512KB, 1MB
*A19 : 1MB
Unused address lines should be N/C (No Connect).
**WE : N/C at 32KB, 64KB