FAIRCHILD
A Schlumberger Company

F6801/F6803
Single-Chip Microcomputer

Advance Product Information

Microprocessor Product

Description

The Fairchild F6801/F6803 is an 8-bit single-chip microcomputer unit (MCU) which significantly enhances the capabilities of the F6800 family. It includes an upgraded F6800 microprocessor unit (MPU) with upward-source and object-code compatibility. The F6801/F6803 MCU can function as a monolithic microcomputer or can be expanded to a 64K byte address space. Features of the F6801/F6803 MCU include:

- **Enhanced F6800 Instruction Set (see table 1)**
- **8 x 8 Multiply Instruction**
- **Serial Communications Interface (SCI)**
- **16-bit Three-Function Programmable Timer**
- **Bus Compatibility with the F6800 Family**
- **2048 Bytes of ROM (F6801 Only)**
- **128 Bytes of RAM**
- **64 Bytes of RAM, Retainable During Powerdown**
- **29 Parallel I/O and Two Handshake Control Lines**
- **Internal Clock Generator With Divide-by-Four Output**
- **Interrupt Capability**
- **TTL compatible**
- **40-Pin Ceramic or Plastic Package**
- **+5V Power Supply**

The F6801/F6803 MCU can be configured to function in a wide variety of applications. This flexibility is provided by its ability to be hardware-programmed into eight different operating modes (see table 2). The operating mode controls the configuration of 18 of the 40 MCU pins, available on-chip resources, memory map, location of interrupt vectors, and type of external bus. Configuration of the remaining 22 pins is not dependent on the operating mode.

The F6803 can be considered an F6801 that operates in Modes 2 and 3 only (either internal RAM with no ROM, or no internal RAM or ROM, respectively).

Connection Diagram

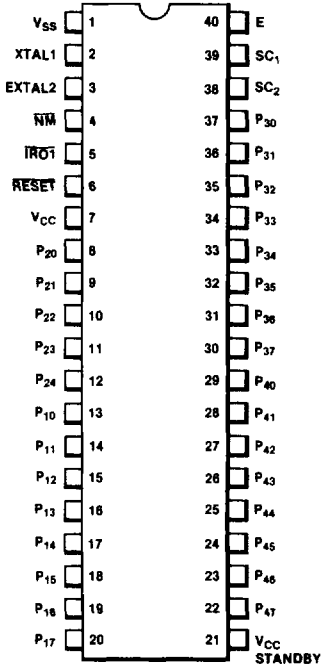

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Figure 1 Block Diagram

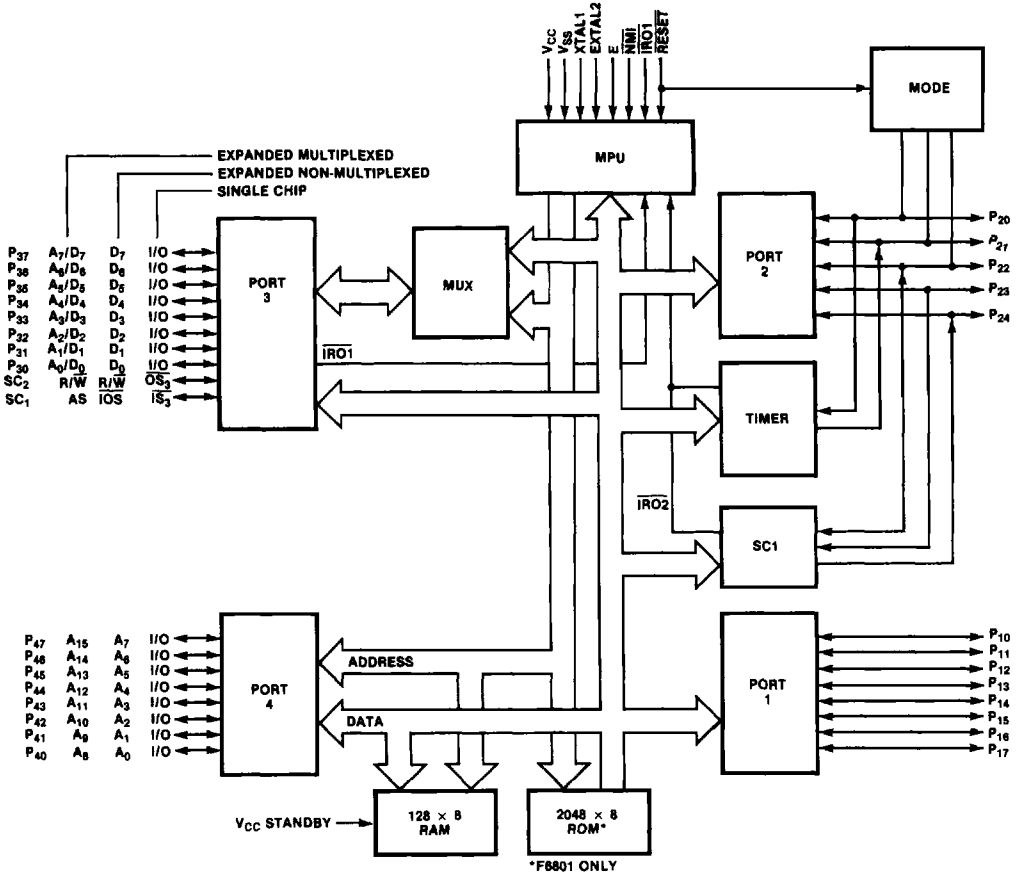

Figure 2 Programming Model

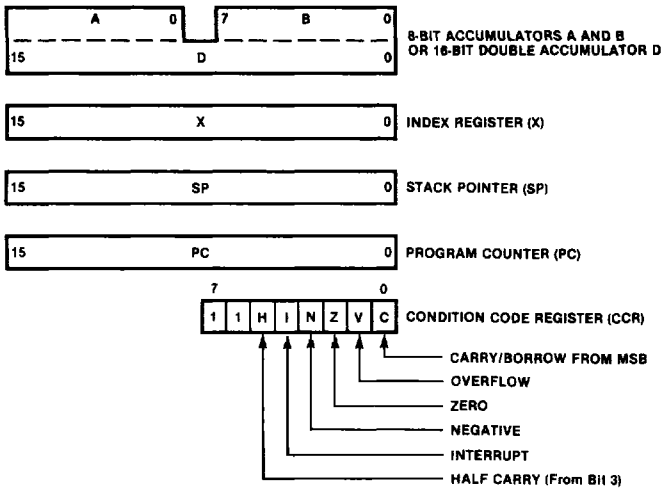

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Table 1 New Instructions

Instruction	Description
ABX	Unsigned addition of Accumulator B to Index Register
ADDD	Adds (without carry) the double accumulator to memory and leaves the sum in the double accumulator
ASLD *or* LSLD	Shifts the double accumulator left (towards MSB) one bit, the LSB is cleared and the MSB is shifted into the C-bit
BHS	Branch If Higher or Same, unsigned conditional branch (same as BCC)
BLO	Branch if Lower. Unsigned conditional branch (same as BCS)
BRN	Branch Never
JSR	Additional addressing mode direct
LDD	Loads double accumulator from memory
LSL	Shifts memory or accumulator left(towards MSB) one bit, the LSB is cleared and the MSB ia shifted into the C-bit (same as ASL)
LSRD	Shifts the double accumulator right (towards LjSB) one bit, the MSB is cleared and the LSB is shifted into the C-bit
MUL	Unsigned multiply, multiplies the two accumulators and leaves the product in the double accumulator
PSHX	Pushes the Index Register to stack
PULX	Pulls the Index Register from stack
STD	Stores the double accumulator to memory
SUBD	Subtracts memory from the double accumulator and leaves the difference in the double accumulator
CPX	Internal processing modified to permit its use with any conditional branch instruction

Table 2 Summary of F6801/F6803 Operating Modes

Common to all Modes: Reserved Register Area Port 1 Port 2 Programmable Timer Serial Communications Interface
Single Chip Mode 7 128 bytes o RAMk, 2048 bytes of ROM Port 3 is a parallel I/O port with two control lines Port 4 is a parallel I/O port SC1 is Input Strobe 3 (IS3) SC2 is Output Strobe 3 (OS3)
Expanded Non-Multiplexed Mode 5 128 bytes of RAM, 2048 bytes of ROM 256 bytes of external memory space Port 3 is an 8-bit data bus Port 4 is an input port/address bus SC1 is Input/Output Select (IOS) SC2 is Read/Write (R/W)
Expanded Multiplexed Modes 1, 2, 3 6 Sour memory space options (64K address space) (1) No internal RAM or ROM (Mode 3) (2) Internal RAM, no ROM (Mode 2) (3) Internal RAM and ROM (Mode 1) (4) Internal RAM, ROM with partial address bus (Mode 6) Port 3 is a multiplexed address/data bus Port 4 is an address bus (inputs/address in Mode 6) SC1 is Address Strobe (AS) SC2 is Read/Write (R/W)
Test Modes 0 and 4 Expanded Multiplexed Test Mode 0 May be used to test RAM and ROM Single Chip and Non-Multiplexed Test Mode 4 (1) May be changed to Mode 5 without going through reset (2) May be used to test Ports 3 and 4 as I/O ports

5

Table 3 - Instruction Execution Times in E-Cycles

	Addressing Mode					
	Immediate	Direct	Extended	Indexed	Inherent	Relative
ABA	•	•	•	•	2	•
ABX	•	•	•	•	3	•
ADC	2	3	4	4	•	•
ADD	2	3	4	4	•	•
ADDD	4	5	6	6	•	•
AND	2	3	4	4	•	•
ASL	•	•	6	6	2	•
ASLD	•	•	•	•	3	•
ASR	•	•	6	6	2	•
BCC	•	•	•	•	•	3
BCS	•	•	•	•	•	3
BEQ	•	•	•	•	•	3
BGE	•	•	•	•	•	3
BGT	•	•	•	•	•	3
BHI	•	•	•	•	•	3
BHS	•	•	•	•	•	3
BIT	2	3	4	4	•	•
BLE	•	•	•	•	•	3
BLO	•	•	•	•	•	3
BLS	•	•	•	•	•	3
BLT	•	•	•	•	•	3
BMI	•	•	•	•	•	3
BNE	•	•	•	•	•	3
BPL	•	•	•	•	•	3
BRA	•	•	•	•	•	3
BRN	•	•	•	•	•	3
BSR	•	•	•	•	•	6
BVC	•	•	•	•	•	3
BVS	•	•	•	•	•	3
CBA	•	•	•	•	2	•
CLC	•	•	•	•	2	•
CLI	•	•	•	•	2	•
CLR	•	•	6	6	2	•
CLV	•	•	•	•	2	•
CMP	2	3	4	4	•	•
COM	•	•	6	6	2	•
CPX	4	5	6	6	•	•
DAA	•	•	•	•	2	•
DEC	•	•	6	6	2	•
DES	•	•	•	•	3	•
DEX	•	•	•	•	3	•
EOR	2	3	4	4	•	•
INC	•	•	6	6	•	•
INS	•	•	•	•	3	•

	Addressing Mode					
	Immediate	Direct	Extended	Indexed	Inherent	Relative
INX	•	•	•	•	3	•
JMP	•	•	3	3	•	•
JSR	•	5	6	6	•	•
LDA	2	3	4	4	•	•
LDD	3	4	5	5	•	•
LDS	3	4	5	5	•	•
LDX	3	4	5	5	•	•
LSL	•	•	6	6	2	•
LSLD	•	•	•	•	3	•
LSR	•	•	6	6	2	•
LSRD	•	•	•	•	3	•
MUL	•	•	•	•	10	•
NEG	•	•	6	6	2	•
NOP	•	•	•	•	2	•
ORA	2	3	4	4	•	•
PSH	•	•	•	•	3	•
PSHX	•	•	•	•	4	•
PUL	•	•	•	•	4	•
PULX	•	•	•	•	5	•
ROL	•	•	6	6	2	•
ROR	•	•	6	6	2	•
RTI	•	•	•	•	10	•
RTS	•	•	•	•	5	•
SBA	•	•	•	•	2	•
SBC	2	3	4	4	•	•
SEC	•	•	•	•	2	•
SEI	•	•	•	•	2	•
SEV	•	•	•	•	2	•
STA	•	3	4	4	•	•
STD	•	4	5	5	•	•
STS	•	4	5	5	•	•
STX	•	4	5	5	•	•
SUB	2	3	4	4	•	•
SUBD	4	5	6	6	•	•
SI	•	•	•	•	12	•
TAB	•	•	•	•	2	•
TAP	•	•	•	•	2	•
TBA	•	•	•	•	2	•
TPA	•	•	•	•	2	•
TST	•	•	6	6	2	•
TSX	•	•	•	•	3	•
TXS	•	•	•	•	3	•
WAI	•	•	•	•	9	•