

EB01

FEATURES

- COMPATIBLE WITH PWM FREQUENCIES UP TO 30KHZ
- 50V TO 500 V MOTOR SUPPLY
- 20A CONTINUOUS OUTPUT CURRENT
- HCMOS COMPATIBLE SCHMITT TRIGGER LOGIC INPUTS
- SEPARATE EMITTER OUTPUTS FOR NEGATIVE RAIL CURRENT SENSE
- SLEEP MODE
- WIDE RANGE FOR GATE DRIVE AND LOGIC SUPPLIES



24-pin DIP
PACKAGE STYLE CK

APPLICATIONS

HIGH POWER CIRCUITS FOR DIGITAL CONTROL OF:

- THREE AXIS MOTION USING BRUSH TYPE MOTORS
- THREE PHASE BRUSHLESS DC MOTOR DRIVE
- THREE PHASE AC MOTOR DRIVE
- THREE PHASE STEP MOTOR DRIVE

DESCRIPTION

The EB01 consists of three independent IGBT half bridges with drivers. The drivers may be interfaced with CMOS or HCMOS level logic.

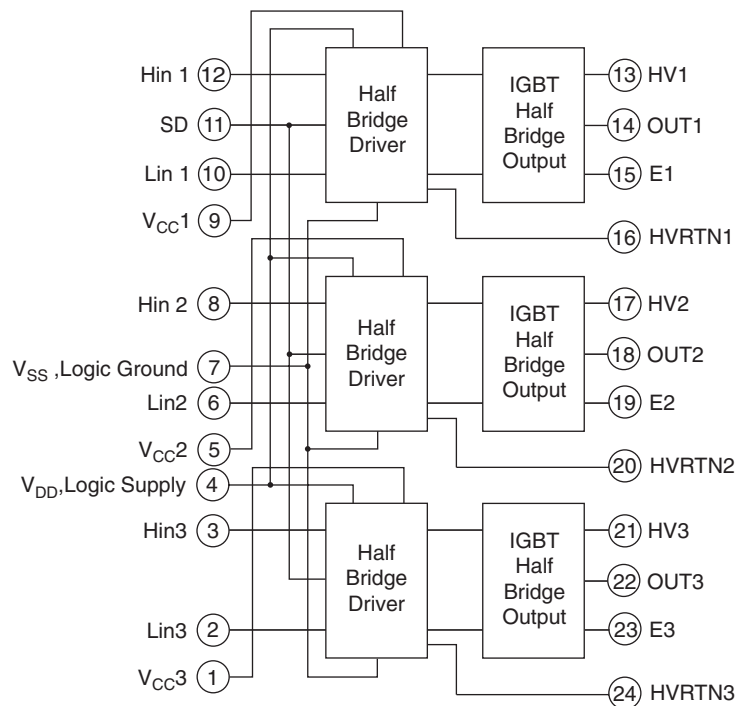


FIGURE 1. BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

HIGH VOLTAGE SUPPLY, HV ⁵	500V
OUTPUT CURRENT, peak ¹	28A
OUTPUT CURRENT, continuous	20A
DRIVER SUPPLY VOLTAGE, V _{cc}	20V
LOGIC SUPPLY VOLTAGE, V _{dd}	20V
LOGIC INPUT VOLTAGE	-0.3V to V _{dd} + 0.3V
POWER DISSIPATION, internal ²	179 Watts
THERMAL RESISTANCE TO CASE ³	2.1°C/Watt
TEMPERATURE, pin solder, 10s	300°C
TEMPERATURE, junction ⁴	150°C
TEMPERATURE RANGE, storage	-65 to +150°C
OPERATING TEMPERATURE, case	-25 to +85°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POSITIVE OUTPUT VOLTAGE	I _{OUT} =20A; V _{cc} =10.8V, V _{dd} =5V; HV=500V, Fpwm=30kHz, L=100 μH	497.3		502.7	Volts
NEGATIVE OUTPUT VOLTAGE	"	-2.7		2.7	Volts
POSITIVE EDGE DELAY	"			1000	n-second
RISETIME	"			500	n-second
NEGATIVE EDGE DELAY	"			1000	n-second
FALLTIME	"			500	n-second
PWM FREQUENCY	Set by external circuitry			30	kHz
INPUT IMPEDANCE	Set by internal resistors	50			k-ohm

INPUT AND OUTPUT SIGNALS

PIN	SYMBOL	FUNCTION	PIN	SYMBOL	FUNCTION
1	V _{cc3}	Gate supply 3	13	HV1	High Voltage supply 1
2	Lin3	Low drive logic in 3	14	OUT1	Section 1 output
3	Hin3	High drive logic in 3	15	E1	Section 1 emitter
4	V _{dd}	Logic supply	16	HVRTN1	Section 1 return
5	V _{cc2}	Gate supply 2	17	HV2	High voltage supply 2
6	Lin2	Low drive logic in 2	18	OUT 2	Section 2 output
7	V _{ss}	Logic ground	19	E2	Section 2 emitter
8	Hin2	High drive logic in 2	20	HVRTN2	Section 2 return
9	V _{cc1}	Gate supply 1	21	HV3	High voltage supply 3
10	Lin1	Low drive logic in 1	22	OUT 3	Section 3 output
11	SD	Shut down logic in	23	E3	Section 3 emitter
12	Hin1	High drive logic in 1	24	HVRTN 3	Section 3 return

- NOTES: 1. Guaranteed but not tested.
 2. Total package power dissipation at 25°C case temperature with three outputs active.
 3. Each IGBT.
 4. Long term operation at the maximum junction temperature will result in reduced product life. Lower internal temperature by reducing internal dissipation or using better heatsinking to achieve high MTTF.
 5. Derate the High Voltage Supply V_s by -0.133% per °C below 25°C.

INPUT

A logic level input independently controls each IGBT in the half bridge. A logic level high turns on the IGBT; a logic level low turns it off. A common shutdown input turns off all IGBTs when high.

All inputs are Schmitt triggers with the upper threshold at 2/3V_{dd} and the lower threshold at 1/3 V_{dd}. This comfortably interfaces with CMOS or HCMOS provided that the V_{dd} for the logic family and the EB01 are the same.

TTL families may be used if a pull-up to the logic supply is added to the TTL gates driving the EBO1, and V_{dd} for the EB01 is the same supply as the logic supply for the TTL family.

An open signal connector pulls the shut down input high and all other inputs low, insuring that all outputs are off.

However, input impedance is 50k on all inputs; therefore, if one input is open circuited a high radiated noise level could spuriously turn on an IGBT.

OUTPUT

Each output section consists of a switching mode IGBT half bridge. Separate HV supply, emitter, and HV return lines are provided for each section.

The IGBTs are conservatively rated to carry 20A. At 20A the saturation voltage is 2.7V maximum.

Each IGBT has a high-speed diode connected in anti-parallel. When switching an inductive load this diode will conduct, and the drop at 20A will be 2.7V maximum.

POWER SUPPLY REQUIREMENTS

SUPPLY	VOLTAGE	MAX CURRENT
HV1	50V to 500V	20A, continuous, 28A peak
HV2	50V to 500V	20A, continuous, 28A peak
HV3	50V to 500V	20A, continuous, 28A peak
V _{cc1}	10V to 20V	10mA
V _{cc2}	10V to 20V	10mA
V _{cc3}	10V to 20V	10mA
V _{dd}	4.5 to 20V	10mA

HV1, HV2, and HV3 may be used independently, or may be one supply. Also V_{cc1}, V_{cc2}, and V_{cc3} may be used independently or tied together. The V_{dd} supply must be compatible with the input logic. If a high voltage logic such as CMOS is used it may be tied with the V_{cc} supplies. HCMOS requires a 5V±10% supply

SPECIAL CONSIDERATIONS

GENERAL

The EB01 is designed to give the user maximum flexibility in a digital or DSP based motion control system. Thermal, overvoltage, overcurrent, and crossfire protection circuits are part of the user's design.

Users should read Application Note 1, "General Operating Considerations;" and Application Note 30, "PWM Basics" for much useful information in applying this part. These Application Notes are in the "Power Integrated Circuits Data Book" and on line at www.apexmicrotech.com.

GROUNDING AND BYPASSING

As in any high power PWM system, grounding and bypassing are one of the keys to success. The EB01 is capable of generating 20 kW pulses with 100 n-second rise and fall times. If improperly grounded or bypassed this can cause horrible conducted and radiated EMI.

In order to reduce conducted EMI, the EB01 provides a separate power ground, named HVRTN, for each high voltage supply. These grounds are electrically isolated from the logic ground (V_{ss}) and each other. This isolation eliminates high current ground loops. However, more than 5V offset between the grounds will destroy the EB01. Apex recommends back to back high current diodes between logic and power grounds; this will maintain isolation but keep offset at a safe level. All grounds should tie together at one common point in the system.

In order to reduce radiated EMI, Apex recommends a 400 µF or larger capacitor between HV and HVRTN. This capacitor should be a switching power grade electrolytic capacitor with ESR rated at 20 kHz. This capacitor should be placed physically as close to the EB01 as possible.

However, such a capacitor will typically have a few hundred milli-ohms or so ESR. Therefore, each section must also be bypassed with a low ESR 1µF or larger ceramic capacitor.

In order to minimize radiated noise it is necessary to minimize the area of the loop containing high frequency

current. (The size of the antenna.) Therefore the 1µF ceramic capacitors should bypass each HV to its return right at the pins the EB01.

SHOOT THROUGH PROTECTION

IGBTs have a relatively short turn on delay, and a long turn off delay. Unlike most semiconductor devices the turn off delay cannot be improved very much by drive circuit design. Therefore, if the turn on input to an IGBT in a half bridge circuit is applied simultaneously with the turn off input to the other IGBT in that half bridge, there will be a time when both IGBTs are simultaneously on. This will short the power rails through the IGBTs, causing excessive power dissipation and very high EMI.

To avoid the shoot through condition the turn on of one IGBT must be delayed long enough for the other in the same half bridge to have completely turned off.

A delay of at least 1.5 µ-seconds is required for the EB01. This delay must be provided after turning off Lin before Hin of the same half bridge may be turned on; likewise it must be provided after turning off Hin before Lin of the same half bridge may be turned on.

PROTECTION CIRCUITS

The EB01 does not include protection circuits.

However, there is a shut down input which will turn off all IGBTs when at logic "1". This input may be used with user designed temperature sensing and current sensing circuits to shut down the IGBTs in the event of a detected unsafe condition. This is recommended since the IGBTs may be turned off this way even if the normal input logic or DSP programming is faulty.

START-UP REQUIREMENTS

In order for an IGBT to be turned on, the corresponding logic input signal must make its positive transition after SD has been low for at least 1 µ-second.

The lower rail IGBT in the half bridge must be turned on for at least 2 µ-seconds to charge the bootstrap capacitor before the top rail IGBT can be turned on. This must be done no more than 330 µ-seconds prior to turning on the top rail IGBT. However, if the load pulls the output to ground, the positive rail IGBT can be turned on without first briefly turning on the negative rail IGBT.

An internal floating supply is used to enhance the operation of the bootstrap bias circuit. This allows the top rail IGBTs to be held on indefinitely once turned on.

HEATSINK

The EB01 should be provided with sufficient heatsink to dissipate 179 watts while holding a case temperature of 25°C when operating at 500V, 20A, 30kHz and 3 sections simultaneously providing maximum current.

The dissipation is composed of conduction losses ($I_{out} \times V_{sat}$) up to 54 watts per half bridge and switching losses of about 4 watts per half bridge. The conduction losses are proportional to I_{out} ; switching losses are proportional to HV supply voltage and to switching frequency.