SONY

CXK77910ATM/AYM -17

131,072-word by 9-bit High Speed Synchronous Static RAM

Description

The CXK77910ATM/AYM is a high speed CMOS synchronous static RAM with common I/O pins, organized as 131,072-word by 9-bit. This synchronous SRAM integrates input registers, high speed SRAM and output registers onto a single monolithic IC. All input signals are latched at the positive edge of an external clock (CLK). The RAM data from the previous cycle is presented at the positive edge of the subsequent clock cycle. Write operation is initiated by the positive edge of CLK and is internally self-timed. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals. 100MHz operation is obtained from a single 5V power supply.

Function

There are three possible user transactions with the STRAM. (Read operation, write operation and deselect operation.)

The read operation requires $\overline{WE}$ = "HIGH" and $\overline{OE}$ = $\overline{CE}$ = "LOW" on the positive edge of CLK.

The memory location pointed to by the contents of the Address registers is read internally and the contents of the location are captured in the Data-out registers on the next positive edge of CLK. The state of Data-out will reflect the contents of the Data-out registers.

The write operation requires $\overline{CE}$ = $\overline{WE}$ = "LOW" on the positive edge of CLK. The memory location pointed to by the contents of the Address registers is written with the contents of the Data-in registers. The write operation is entirely self-timed, eliminating critical timing edges.

The deselect cycle requires $\overline{CE}$ = "HIGH" or $\overline{OE}$ = $\overline{WE}$ = "HIGH" on the positive edge of CLK. Write operation and internal read operation are disabled during the clock cycle. The data outputs are forced to a high impedance state during the next clock cycle. During the deselect cycle by $\overline{CE}$ = "HIGH", STRAM turns to power down mode.

CXK77910ATM
44 pin TSOP(II)(Plastic)

CXK77910AYM
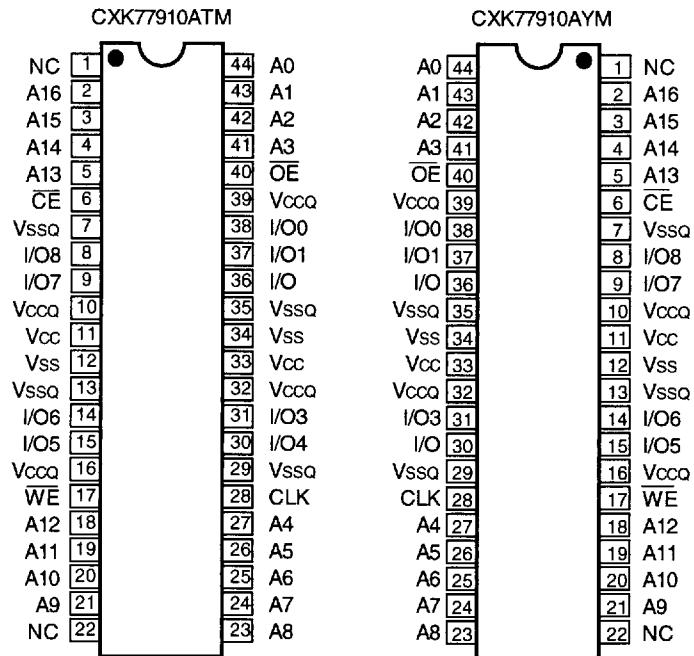44 pin TSOP(II)(Plastic)
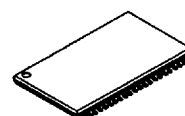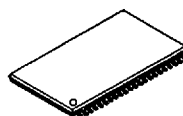
Structure

Silicon gate CMOS IC

Features

- Fast cycle time: (Cycle) (Frequency)
  CXK77910ATM/AYM-17   16.6ns   60MHz
- Fast clock to data valid
  CXK77910ATM/AYM-17   8.5ns
- High speed, low power consumption
- Single +5V power supply: 5V ± 5%
- Separate output power supply: 3.15V to 5.25V
- Inputs and outputs are TTL compatible
  (3.3V I/O compatible)
- Common data input and output
- All inputs and outputs are registered on a single clock edge
- Self-timed write cycle
- Package line-up
  CXK77910ATM/AYM
  400mil 44 pin TSOP II with 0.8mm pitch

E94924A52-ST

8382383 0010160 174

Pin Configuration (Top View)

CXK77910ATM

NC	1	44	A0
A16	2	43	A1
A15	3	42	A2
A14	4	41	A3
A13	5	40	$\overline{OE}$
$\overline{CE}$	6	39	Vccq
Vssq	7	38	I/O0
I/O8	8	37	I/O1
I/O7	9	36	I/O
Vccq	10	35	Vssq
Vcc	11	34	Vss
Vss	12	33	Vcc
Vssq	13	32	Vccq
I/O6	14	31	I/O3
I/O5	15	30	I/O4
Vccq	16	29	Vssq
$\overline{WE}$	17	28	CLK
A12	18	27	A4
A11	19	26	A5
A10	20	25	A6
A9	21	24	A7
NC	22	23	A8

CXK77910AYM

A0	44	1	NC
A1	43	2	A16
A2	42	3	A15
A3	41	4	A14
$\overline{OE}$	40	5	A13
Vccq	39	6	$\overline{CE}$
I/O0	38	7	Vssq
I/O1	37	8	I/O8
I/O	36	9	I/O7
Vssq	35	10	Vccq
Vss	34	11	Vcc
Vcc	33	12	Vss
Vccq	32	13	Vssq
I/O3	31	14	I/O6
I/O	30	15	I/O5
Vssq	29	16	Vccq
CLK	28	17	$\overline{WE}$
A4	27	18	A12
A5	26	19	A11
A6	25	20	A10
A7	24	21	A9
A8	23	22	NC

Pin Description (1)

Symbol	Description
A0 to A16	Address input
I/O0 to I/O8	Data input/output
CLK	Clock
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vccq	Output power supply
Vcc	+5V power supply
Vss/Vssq	Ground

Block Diagram
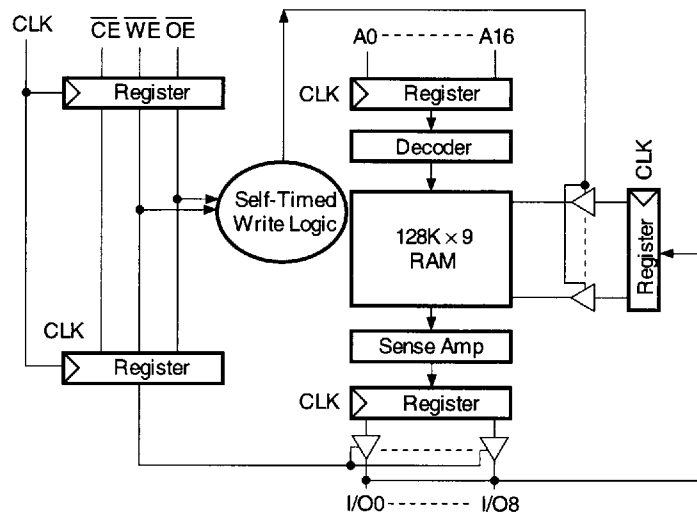
Pin Description (2)

CLK (Clock, positive edge triggered)
All timing is controlled by the rising or positive edge of CLK. All synchronous input and output signals are registered on the positive edge of CLK with set-up and hold times referenced to that edge. Since only one edge of CLK is referenced, the duty cycle of CLK is not critical.

A0 to A16 (Address)
The Address inputs are decoded on-chip to select one of 131,072 words. The state of the Address inputs is registered into the Address register on the positive edge of CLK. The Address inputs must be valid during every positive edge with all set-up and hold times referenced to that edge.

I/O0 to I/O8 (Data input/output)
I/O terminals are three-state and data input/output common. The state is defined by the Control block (refer to the truth table on page 4).
The data inputs for write operation must be valid during every positive edge of CLK with all set-up and hold times referenced to that edge. The data outputs are triggered by the positive edge of CLK and the contents of the Output-Registers are presented.

$\overline{\text{WE}}$ (Synchronous Write Enable, active low)
$\overline{\text{WE}}$ is used to indicate whether a read or write operation is to be performed. $\overline{\text{WE}}$ is "LOW" to perform a write operation. $\overline{\text{WE}}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge. The internal timing required to store data into the memory array is self-timed.

$\overline{\text{CE}}$ (Synchronous Chip Enable, active low)
$\overline{\text{CE}}$ is used to select the Synchronous SRAM when low (or deselect when high). When selected, the Synchronous SRAM will perform a read or write operation (refer to the truth table on page 4). The state of $\overline{\text{CE}}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

**$\overline{\text{OE}}$ (Synchronous Output Enable, active low)**
$\overline{\text{OE}}$ is used to indicate that a read operation is to be performed. If the Synchronous SRAM is selected, the $\overline{\text{OE}}$ is low to perform a read operation (refer to the truth table on page 4). The state of $\overline{\text{OE}}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

Absolute Maximum Ratings   (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5 to Vcc +0.5	V
Output voltage	Vo	−0.5 to Vcc +0.5	V
Allowable power dissipation	P_D	1	W
Operating temperature	Topr	0 to 70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature · time	Tsolder	235 · 10	°C · sec

Truth Table

CLK	$\overline{CE}$ (tn)	$\overline{WE}$ (tn)	$\overline{OE}$ (tn)	Mode	I/O to 8	Vcc Current
⌐	H	×	×	Deselect	Hi-Z	I_{SB}
⌐	L	H	H	Read	Hi-Z	Icc
⌐	L	H	L	Read	Data out*	Icc
⌐	L	L	×	Write	Data in	Icc

×: "H" or "L"

* Data come out on the next positive edge of CLK.

DC recommended Operating Conditions   (Ta = 25°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.75	5.0	5.25	V
Output supply voltage	Vccq	3.15	—	5.25	V
Input high voltage	V_{IH}	2.2	—	Vcc + 0.3	V
Input low voltage	V_{IL}	−0.3*	—	0.8	V

* V_{IL} = −3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics   (Vcc = 5V ± 5%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to Vcc	−1	1	μA
Output leakage current	I_{LO}	Vo = GND to Vcc $\overline{OE}$ = V_{IH}	−1	1	
Average operating current	I_{CC}	Duty = 100% I_{OUT} = 0mA	—	150	mA
Standby current	I_{SB}	$\overline{CE} \geq V_{IH}$ Cycle = Min. Duty = 100%	—	130	
Output high voltage	V_{OH}	I_{OH} = −2.0mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 4.0mA	—	0.4	

I/O capacitance   (Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	5	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note) These parameters are sampled and are not 100% tested.
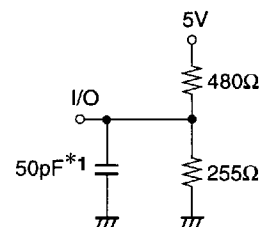
AC characteristics
• AC test conditions   (Vcc = 5V ± 5%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 3ns
Input fall time	tf = 3ns
Input/output reference level	1.5V
Output load conditions	Fig. 1
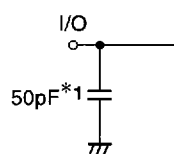
Output Load (1)   Output Load (2) *2

*1 Including scope and jig capacitance.

*2 For t$_{CKHQZ}$, t$_{CKHQX}$.

Fig. 1

- **Read cycle ($\overline{WE}$ = "H")**

Item	Symbol	-17		Unit
		Min.	Max.	
Read cycle time	t_{CKHCKH}	16.6	—	ns
Clock high pulse width	t_{CKHCKL}	5	—	
Clock low pulse width	t_{CKLCKH}	5	—	
Clock to data valid	t_{CKHQV}	—	8.5	
Address setup to clock high	t_{AVCKH}	3	—	
Address hold from clock high	t_{CKHAX}	1	—	
Chip enable setup to clock high	t_{CEVCKH}	3	—	
Chip enable hold from clock high	t_{CKHCEX}	1	—	
Output enable setup to clock high	t_{OEVCKH}	3	—	
Output enable hold from clock high	t_{CKHOEX}	1	—	
Clock high to output low-Z	t_{CKHQX}*	3	—	
Clock high to output high-Z	t_{CKHQZ}*	—	8	

* Transition is measured ±200mV from steady voltage with specfified loading in Fig. 1-(2).
  This parameter is sampled and is not 100% tested.

- **Write cycle**

| Item	Symbol	-17		Unit
		Min.	Max.	
Write cycle time	t_{CKHCKH}	16.6	—	ns
Clock high pulse width	t_{CKHCKL}	5	—	
Clock low pulse width	t_{CKLCKH}	5	—	
Address setup to clock high	t_{AVCKH}	3	—	
Address hold from clock high	t_{CKHAX}	1	—	
Chip enable setup to clock high	t_{CEVCKH}	3	—	
Chip enable hold from clock high	t_{CKHCEX}	1	—	
Write enable setup to clock high	t_{WEVCKH}	3	—	
Write enable hold from clock high	t_{CKHWEX}	1	—	
Input data setup to clock high	t_{DVCKH}	3	—	
Input data hold from clock high	t_{CKHDX}	1	—	

Timing Waveform
• Read cycle
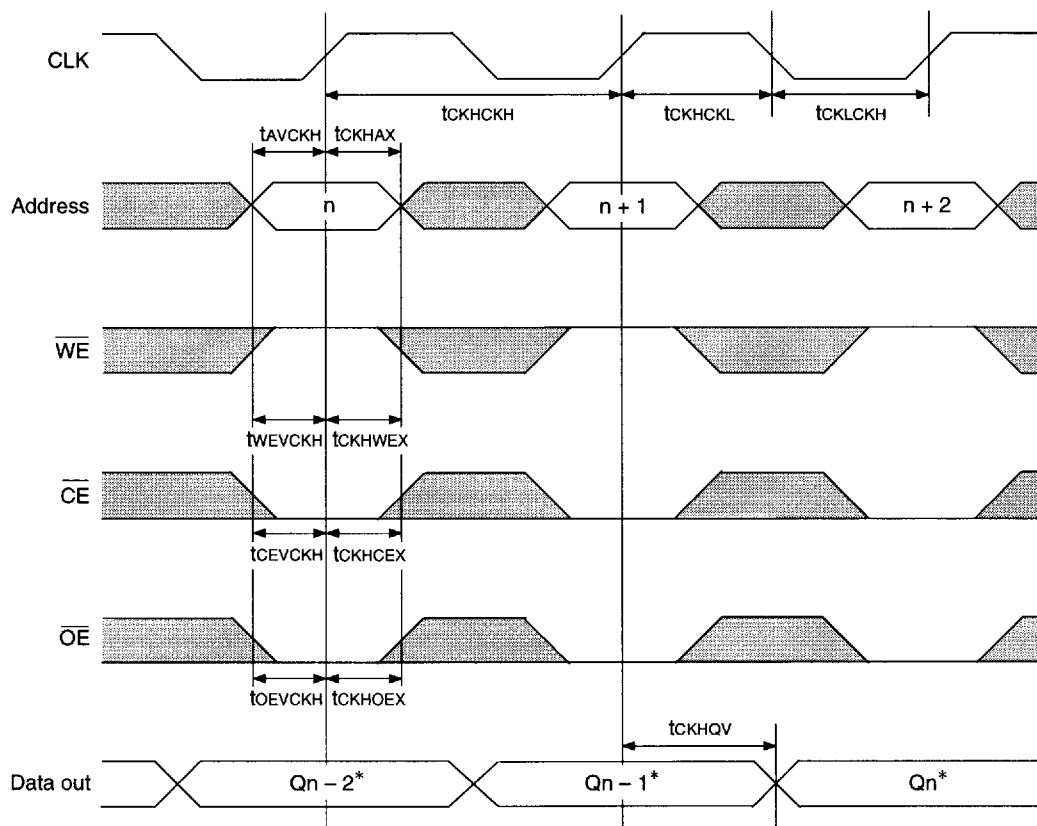
* Valid data from CLK high is the data from the previous cycle

• **Write cucle: $\overline{\text{OE}}$ = V$_{\text{IH}}$ or V$_{\text{IL}}$**
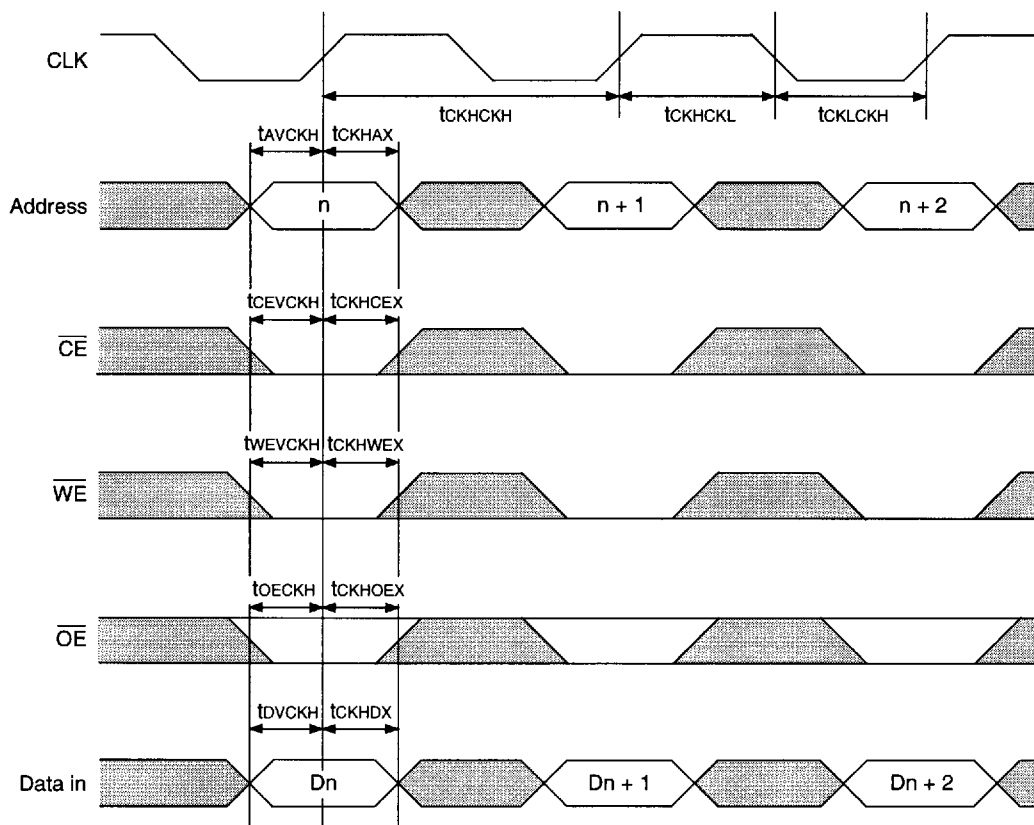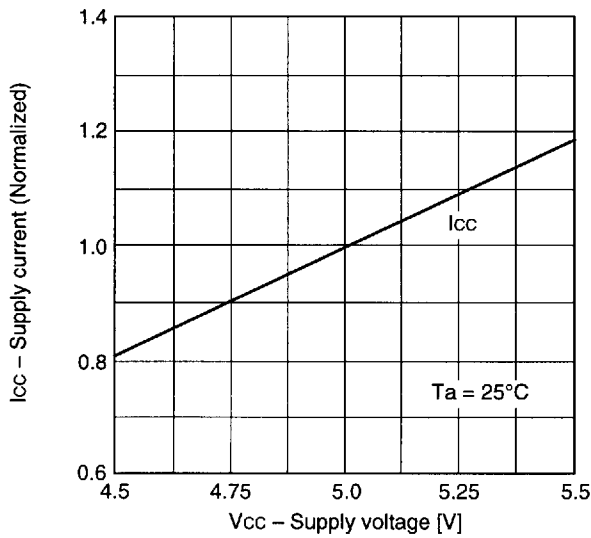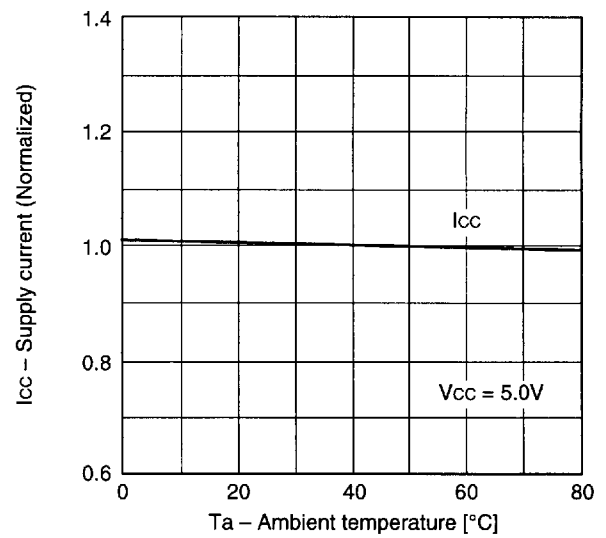
• Read/Write cycle
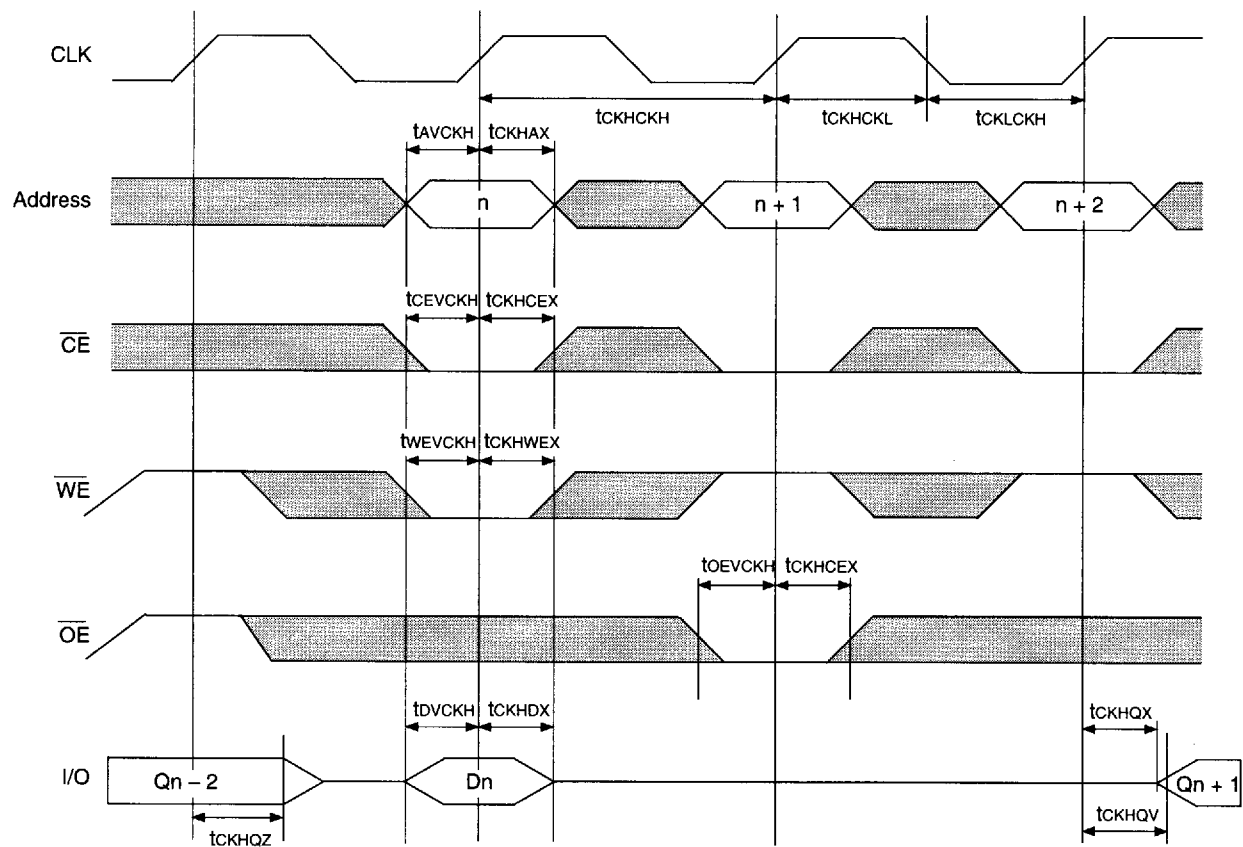
Example of Representative Characteristics
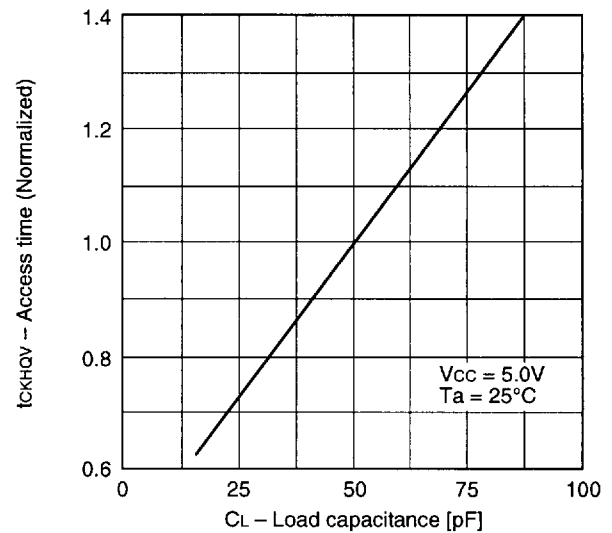
Supply current vs. Supply voltage

Icc – Supply current (Normalized)

Icc

Ta = 25°C

Vcc – Supply voltage [V]

Supply current vs. Ambient temperature

Icc – Supply current (Normalized)

Icc

Vcc = 5.0V

Ta – Ambient temperature [°C]

Supply current vs. Frequency

Icc – Supply current (Normalized)

Read, Write

Vcc = 5.0V
Ta = 25°C

Frequency (1/tCKHCKH) [MHz]
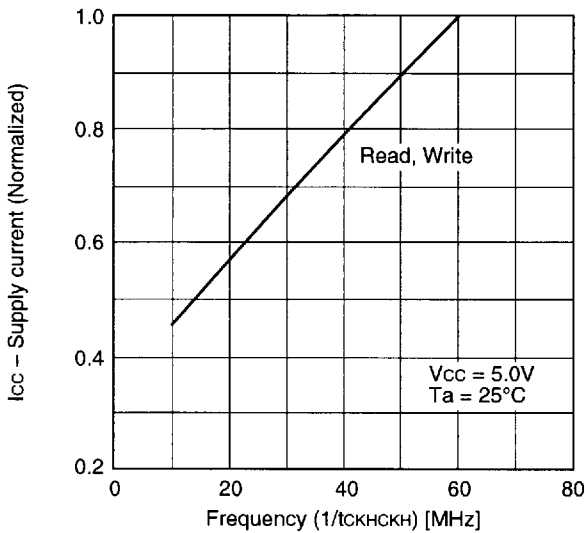
Access time vs. Load capacitance

tCKHQV – Access time (Normalized)

Vcc = 5.0V
Ta = 25°C

CL – Load capacitance [pF]

Cycle time (minimum)/Access time vs. Supply voltage

tCKHCKH – Cycle time,
tCKHQV – Access time (Normalized)

tCKHQV

tCKHCKH

Ta = 25°C

Vcc – Supply voltage [V]
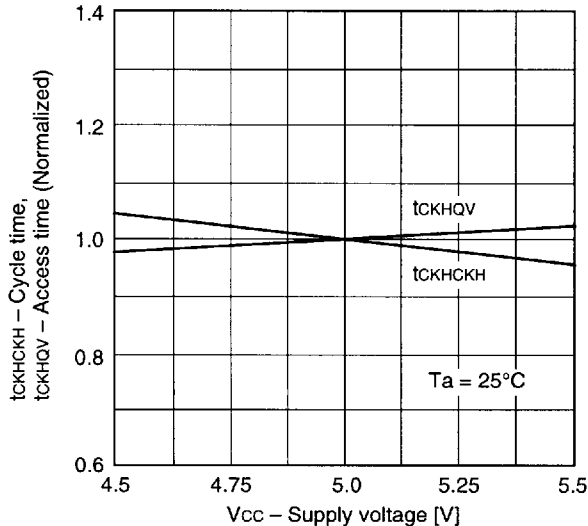
Cycle time (minimum)/Access time vs. Ambient temperature

tCKHCKH – Cycle time,
tCKHQV – Access time (Normalized)

tCKHCKH

tCKHQV

Vcc = 5.0V

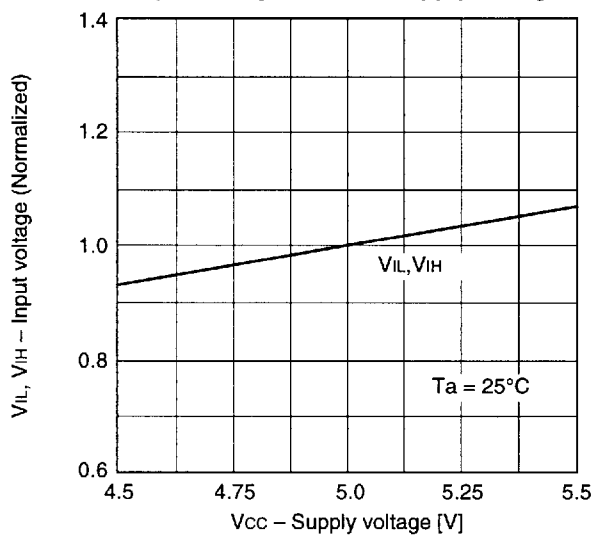Ta – Ambient temperature [°C]
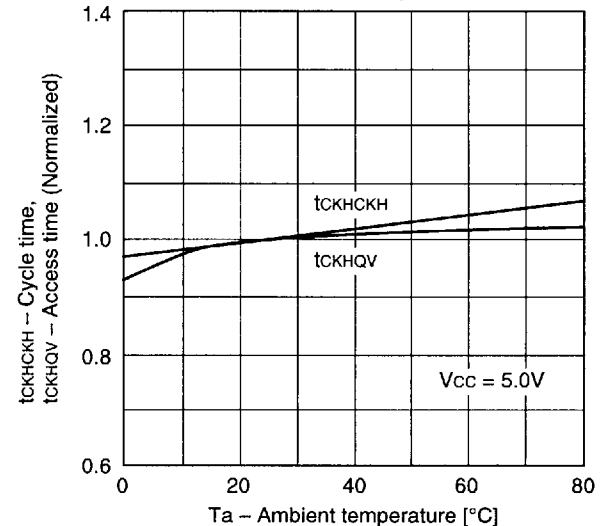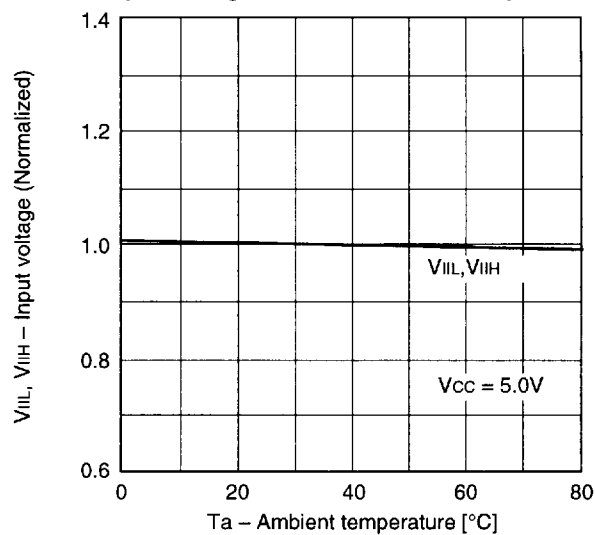
Standby current vs. Supply voltage
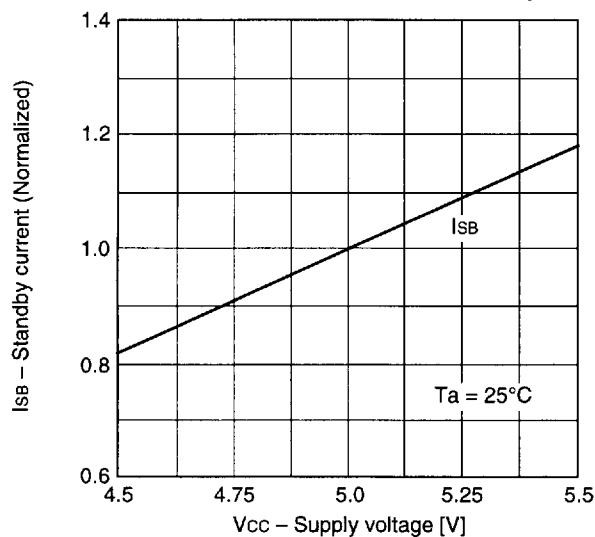
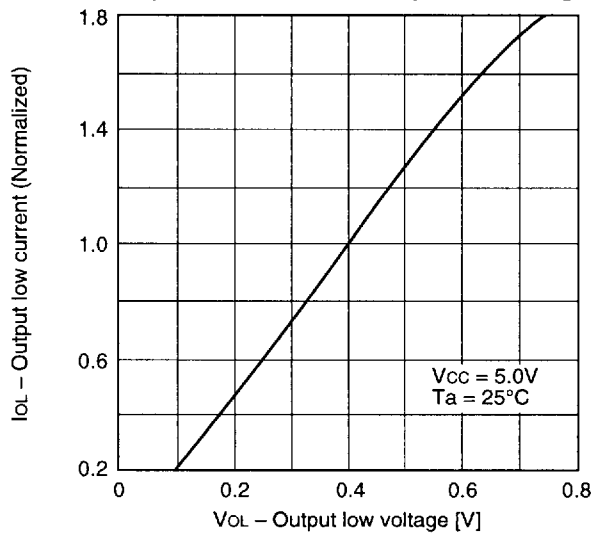## Standby current vs. Ambient temperature
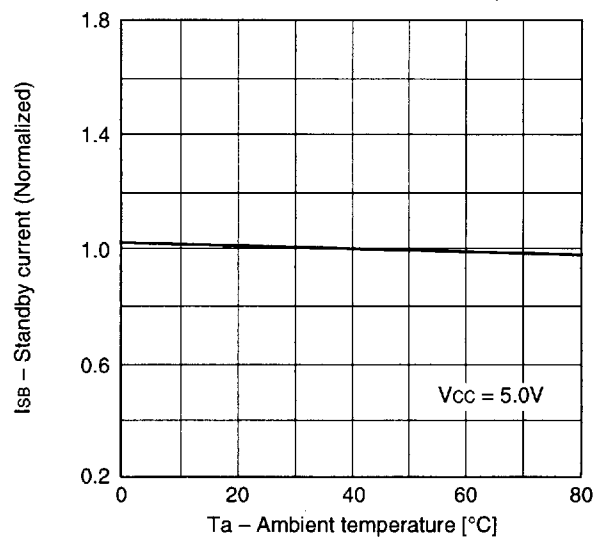
Input voltage level vs. Supply voltage
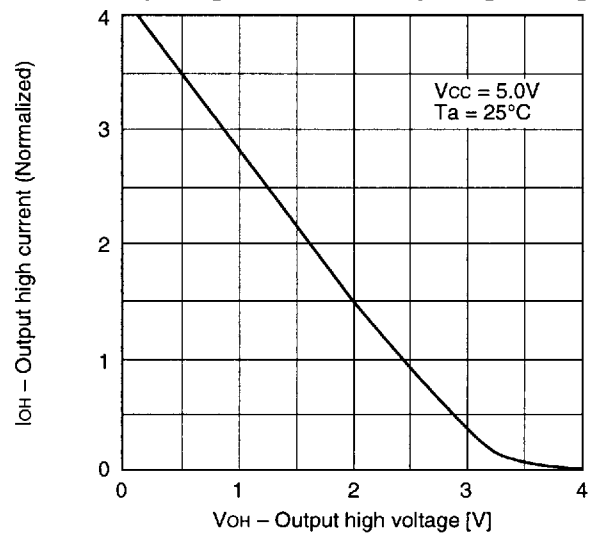

Input voltage level vs. Ambient temperature
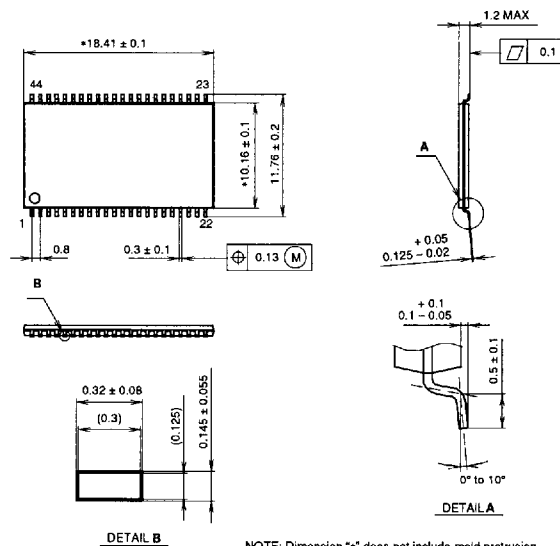

Output low current vs. Output low voltage

Output high current vs. Output high voltage

Package Outline   Unit: mm

CXK77910ATM

44PIN TSOP (II) (PLASTIC) 400mil

DETAIL B

DETAIL A

NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	TSOP (II) -44P-L01
EIAJ CODE	TSOP (II) 044-P-0400-A
JEDEC CODE	———

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g

CXK77910AYM

44PIN TSOP (II) (PLASTIC) 400mil

DETAIL B

DETAIL A

NOTE: Dimension "*" does not include mold protrusion.
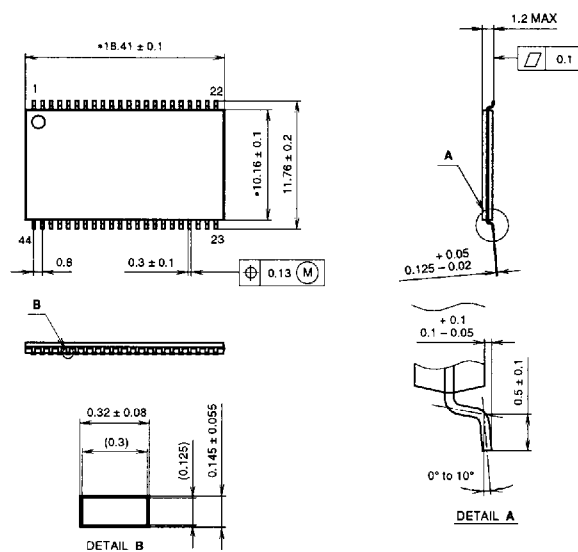
PACKAGE STRUCTURE

SONY CODE	TSOP (II) -44P-L01R
EIAJ CODE	TSOP (II) 044-P-0400-B
JEDEC CODE	———

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g

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