Octal dual supply translating transceiver (3-State) 74LVC4245A

FEATURES

- Wide supply voltage range
  - 3 Volt port: 1.5 to 3.6 V
  - 5 Volt port: 1.5 to 5.5 V
- In accordance with JEDEC standard no. 8-1A
- Control inputs accept voltages up to 5.5 V
- CMOS lower power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC4245A is a high-performance, low-power, low-voltage, Si-gate CMOS device and is superior to most advanced CMOS compatible TTL families.

The 74LVC4245A is an octal dual supply translating transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V bus and 5 V bus in a mixed 3 V/5 V supply environment.

The 74LVC4245A features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. ($\overline{OE}$) controls the outputs so that the buses are effectively isolated.

In suspend mode, when V_{CCA} is zero, there will be no current flow from one supply to the other supply. The A-outputs must be set 3-State and the voltage on the A bus must be smaller than V_{diode} (typ. 0.7 V). $V_{CCA} \geq V_{CCB}$ (except in suspend mode).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nB nB to nA	C_L = 50 pF; V_{CCA} = 5.0 V V_{CCB} = 3.3 V	 4.0 4.0	ns
$C_{I/O}$	Input/output capacitance		10	pF
C_{PDA}	A port nA to nB A port nB to NA	V_I = GND to V_{CC}[1]	7.8 27.9	pF
C_{PDB}	B port nA to nB B port nB to NA		26 10.4	

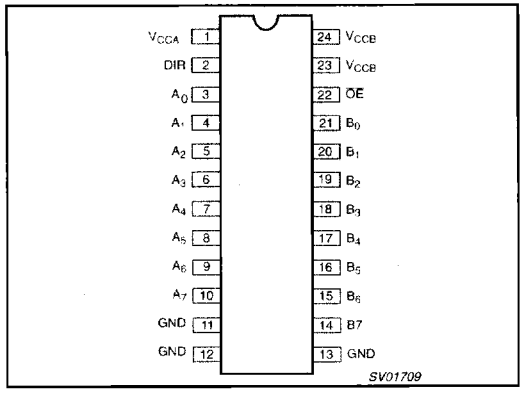
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +125°C	74LVC4245A D	74LVC4245A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +125°C	74LVC4245A DB	74LVC4245A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +125°C	74LVC4245A PW	74LVC4245A DH	SOT355-1

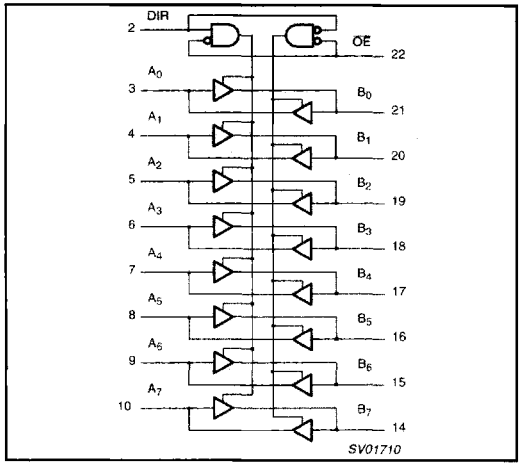
PIN CONFIGURATION



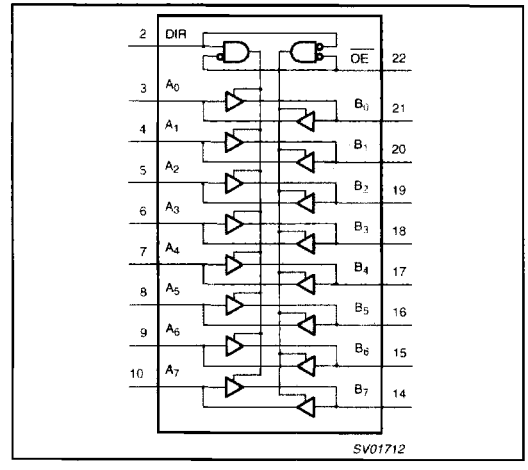
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	V_{CCA}	Positive supply voltage (5 V bus)
2	DIR	Direction control
2, 4, 5, 6, 7, 8, 9, 10	A_0 to A_7	Data inputs/outputs
11, 12, 13	GND	Ground (0 V)
14, 15, 16, 17, 18, 19, 20, 21	B_7 to B_0	Data inputs/outputs
22	$\overline{OE}$	Output enable input (active LOW)
23, 24	V_{CCB}	Positive supply voltage (3 V bus)

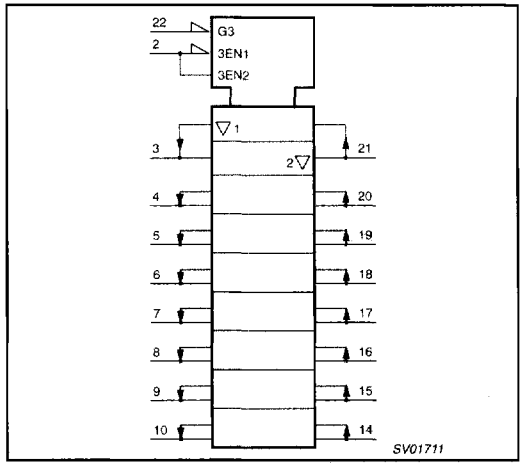
LOGIC SYMBOL



FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUTS	
$\overline{OE}$	DIR	A_n	B_N
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CCA}	DC supply voltage 5V port	$V_{CCA} \geq V_{CCB}$; Waveform 4	1.5	5.5	V
V_{CCB}	DC supply voltage 3V port	$V_{CCA} \geq V_{CCB}$; Waveform 4	1.5	3.6	V
V_I	DC input voltage range (control inputs)		0	5.5	V
$V_{I/O}$	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC input voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		−40	+85	°C
t_r, t_f	Input rise and fall times	V_{CCB} = 2.7 to 3.0V V_{CCB} = 3.0 to 3.6V V_{CCA} = 3.0 to 4.5V V_{CCA} = 4.5 to 5.5V	0 0 0 0	20 10 20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CCA}	DC supply voltage 5V port		−0.5 to +6.5	V
V_{CCB}	DC supply voltage 3V port		−0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +6.5	V
$V_{I/O}$	DC output voltage; output HIGH or LOW	Note 2	−0.5 to V_{CC} +0.5	V
	DC input voltage; output 3-State	Note 2	−0.5 to 6.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−60 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage (3V port)	$V_{CCA/B}$ = 2.7 to 3.6V		2.0			V
	HIGH level Input voltage (5V port)	$V_{CCA/B}$ = 4.5 to 5.5V		2.0			V
V_{IL}	LOW level Input voltage (3V port)	$V_{CCA/B}$ = 2.7 to 3.6V				0.8	V
	LOW level Input voltage (5V port)	$V_{CCA/B}$ = 4.5 to 5.5V				0.8	V
V_{OH}	HIGH level output voltage (3V port)	$V_{CCA/B}$ = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA		V_{CC} – 0.5			V
		$V_{CCA/B}$ = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100mA		V_{CC} – 0.2	V_{CC}		
		$V_{CCA/B}$ = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24µA		V_{CC} – 1.0			
	HIGH level output voltage (5V port)	$V_{CCA/B}$ = 4.5V; V_I = V_{IH} or V_{IL}; I_O = –12mA		V_{CC} – 0.5			V
		$V_{CCA/B}$ = 4.5V; V_I = V_{IH} or V_{IL}; I_O = –100µA		V_{CC} – 0.2	V_{CC}		
		$V_{CCA/B}$ = 4.5V; V_I = V_{IH} or V_{IL}; I_O = –24mA		V_{CC} – 0.8			
V_{OL}	LOW level output voltage (3V port)	$V_{CCA/B}$ = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA				0.40	V
		$V_{CCA/B}$ = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100mA				0.20	
		$V_{CCA/B}$ = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24µA				0.55	
	LOW level output voltage (5V port)	$V_{CCA/B}$ = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 12mA				0.40	V
		$V_{CCA/B}$ = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100mA				0.20	
		$V_{CCA/B}$ = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 24µA				0.55	
I_I	Input leakage current (control inputs)	$V_{CCA/B}$ = 3.6V; V_I = 5.5V or GND	Not for I/O pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins (3V port)	$V_{CCA/B}$ = 3.6V; V_I = V_{CC} or GND			±0.1	±15	µA
	Input current for common I/O pins (5V port)	$V_{CCA/B}$ = 5.5V; V_I = V_{CC} or GND			±0.1	±15	µA
I_{OZ}	3-State output OFF-state current (3V port)	$V_{CCA/B}$ = 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			0.1	±5	µA
	3-State output OFF-state current (5V port)	$V_{CCA/B}$ = 5.5V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			0.1	±5	µA
I_{CC}	Quiescent supply current (3V port)	$V_{CCA/B}$ = 3.6V; V_I = V_{CC} or GND; I_O = 0			0.1	10	µA
	Quiescent supply current (5V port)	$V_{CCA/B}$ = 5.5V; V_I = V_{CC} or GND; I_O = 0			0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin (3V port)	$V_{CCA/B}$ = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0			5	500	µA
	Additional quiescent supply current per input pin (5V port)	$V_{CCA/B}$ = 4.5V to 5.5V; V_I = V_{CC} –2.1V; I_O = 0			5	500	µA

NOTES:

1. All typical values are measured at V_{CCA} = 5.0V, V_{CCB} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS									UNIT
			V_{CCA} = 5 V ± 0.5 V			V_{CCB} = 3.3 V ± 0.3 V			V_{CCB} = 2.7 V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}/t_{PLH}	Propagation delay A_n to B_n	Figures 1, 3	1.5	4.5	7.0	1.5	4.0	6.5*	1.5	4.5	7.0	ns
			1.5	4.0*	6.5							
t_{PHL}/t_{PLH}	Propagation delay B_n to A_n	Figures 1, 3	1.5	4.5	7.0	1.5	4.0	6.5*	1.5	4.5*	7.0	ns
			1.5	4.0*	6.5							
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to A_n	Figures 2, 3	1.5	7.0	11.0	1.5	6.2	10	1.5	7.0	11.0	ns
			1.5	6.2*	10							
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to B_n	Figures 2, 3	1.5	5.7	8.7	1.5	5.0	8.1	1.5	5.7	8.7	ns
			1.5	5.0	8.1							
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n	Figures 2, 3	1.5	5.7	8.0	1.5	5.3*	7.5	1.5	5.7	8.0	ns
			1.5	5.3*	7.5							
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to B_n	Figures 2, 3	1.5	6.2	8.5	1.5	5.8	7.8	1.5	6.2	8.5	ns
			1.5	5.8*	7.8							

NOTE:

All typical values are measured at $T_{amb} = 25°C$.

* Typical values are measured at $V_{CCA} = 5.0$ V and $V_{CCB} = 3.3$ V.

AC WAVEFORMS

$V_M = 1.5$ V at 2.7 V $\leq V_{CC} \leq 3.6$ V

$V_M = 0.5 \times V_{CCA}$ at $V_{CCA} \geq 4.5$ V

$V_x = V_{OL} + 0.3$ V at $V_{CC} \leq 3.6$ V

$V_x = V_{OL} + 0.1 \times (V_{CC} - V_{OL})$ at $V_{CCA} \geq 4.5$ V

$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 3.6$ V

$V_Y = V_{OH} - 0.1 \times (V_{OH} - GND)$ at $V_{CCA} \geq 4.5$ V

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

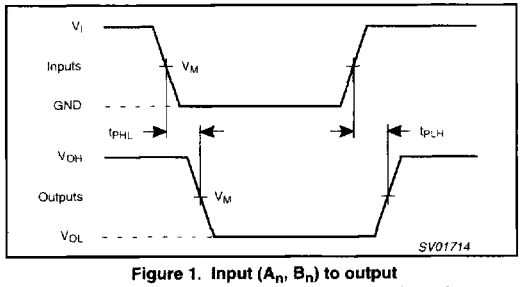


Figure 1. Input (A_n, B_n) to output (B_n, A_n) propagation delays and output transition times.

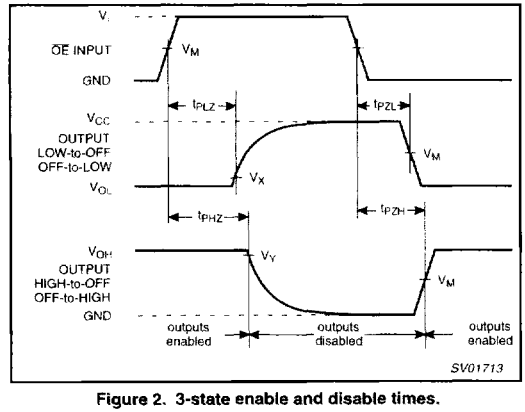


Figure 2. 3-state enable and disable times.

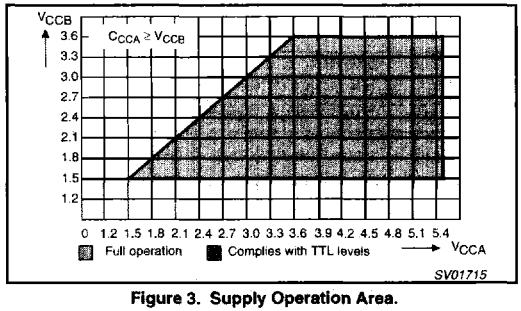


Figure 3. Supply Operation Area.

TEST CIRCUIT

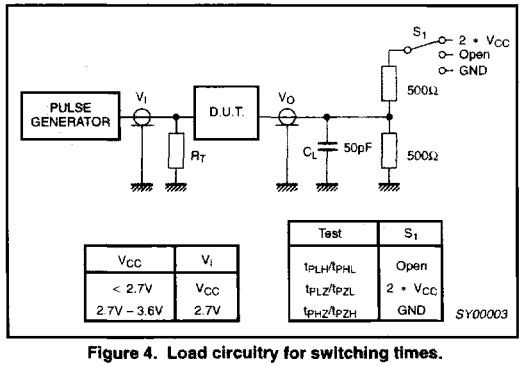


Figure 4. Load circuitry for switching times.