HARRIS

2N6800

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

August 1991

Features

- 3A, 400V
- $r_{DS(on)} = 1\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

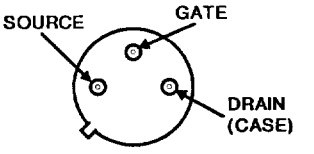
Description

The 2N6800 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The 2N6800 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

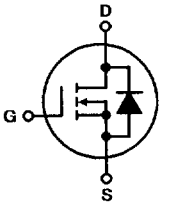
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6800	UNITS
Drain-Source Voltage	V_{DS}	400*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400*	V
Continuous Drain Current			
T_C = +25°C	I_D	3*	A
T_C = +100°C	I_D	2*	A
Pulsed Drain Current	I_{DM}	14*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	3*	A
Pulse Source Current	I_{SM}	14*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	25*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.20*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	14	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **1904.1**

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	400*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 400V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 320V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	–	–	3.0*	V	V_{GS} = 10V, I_D = 3.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	–	0.8	1.0*	Ω	V_{GS} = 10V, I_D = 2.0A, T_A = 25°C
		–	–	2.4*	Ω	V_{GS} = 10V, I_D = 2.0A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.70*	–	1.4*	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	2.0*	3.5	6.0*	S(℧)	V_{DS} = 5V, I_D = 2.0A
C_{iss}	Input Capacitance	350*	700	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	50*	150	300*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	20*	40	80*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	30*	ns	V_{DD} ≅ 176V, I_D = 2.0A, Z_o = 50Ω
t_r	Rise Time	–	–	35*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	55*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	35*	ns	of operating temperature.)
SOA	Safe Operating Area	25	–	–	W	V_{DS} = 200V, I_D = 125 mA, See Fig. 16.
		25	–	–	W	V_{DS} = 8.3V, I_D = 3.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	600	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	4.0	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

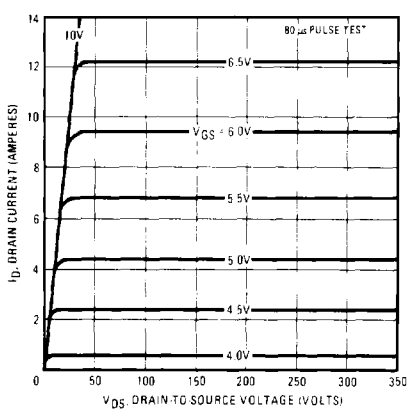


Fig. 1 - Typical output characteristics.

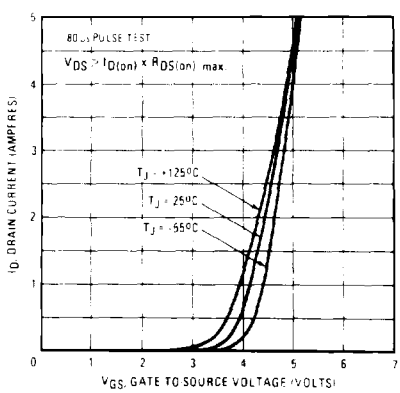


Fig. 2 - Typical transfer characteristics.

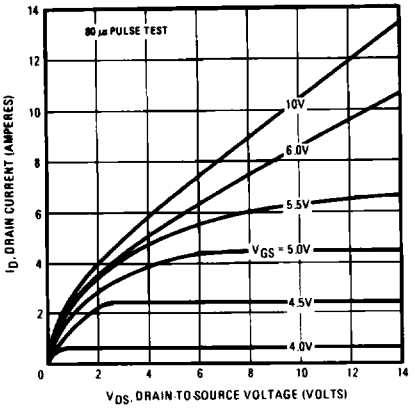


Fig. 3 - Typical saturation characteristics.

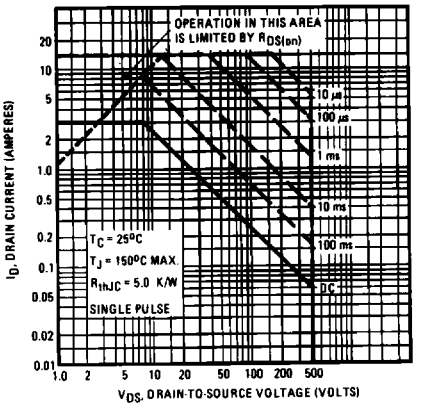


Fig. 4 - Maximum safe operating area.

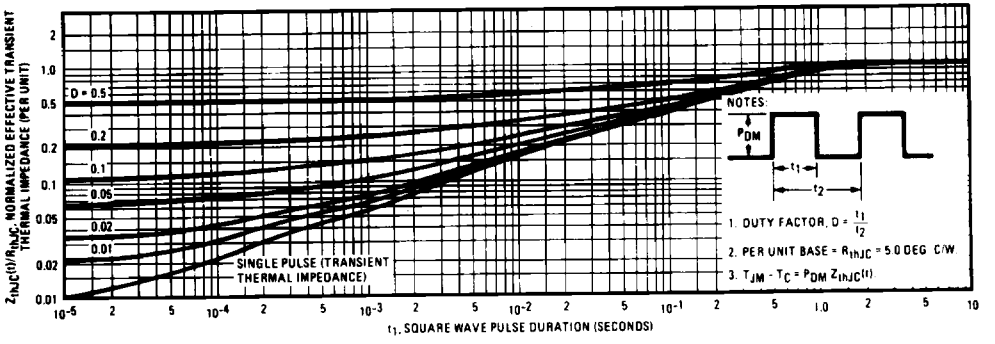


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

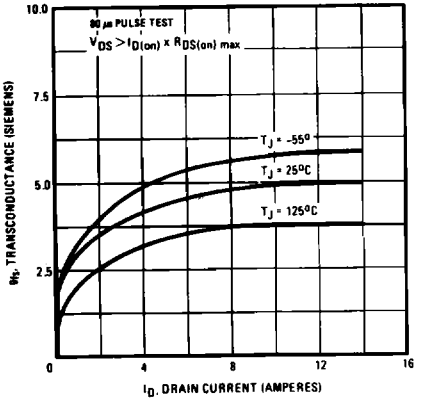


Fig. 6 - Typical transconductance versus drain current.

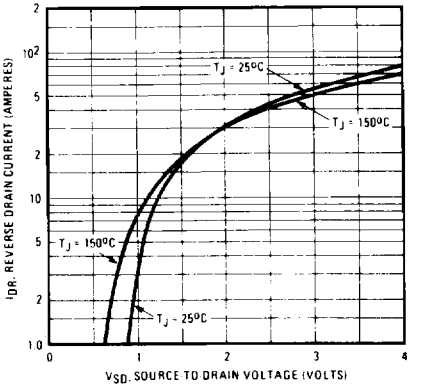


Fig. 7 - Typical source-drain diode forward voltage.

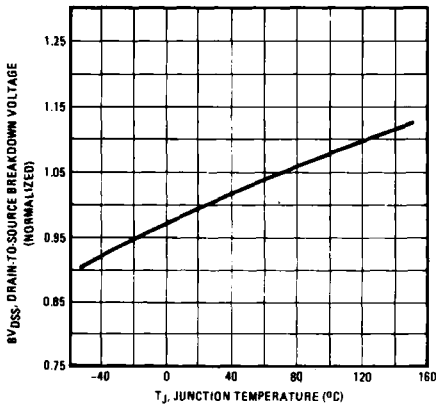


Fig. 8 - Breakdown voltage versus temperature.

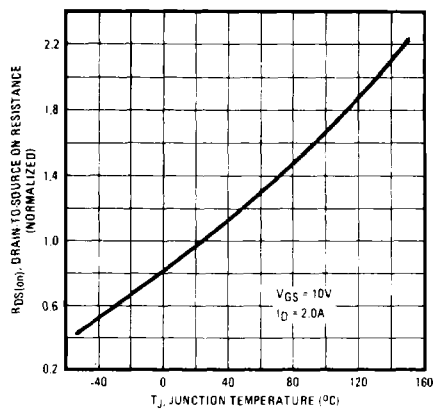


Fig. 9 - Typical normalized on-resistance versus temperature.

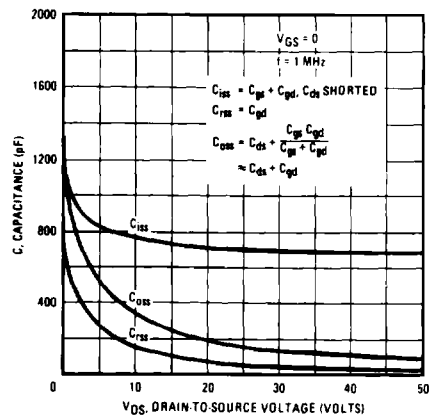


Fig. 10 - Typical capacitance versus drain-to-source voltage.

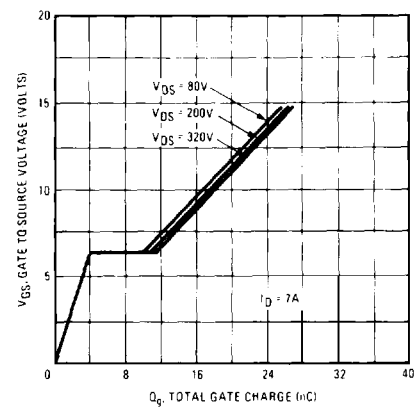


Fig. 11 - Typical gate charge versus gate-to-source voltage.

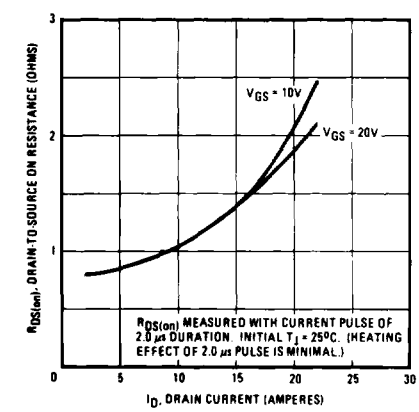


Fig. 12 - Typical on-resistance versus drain current.

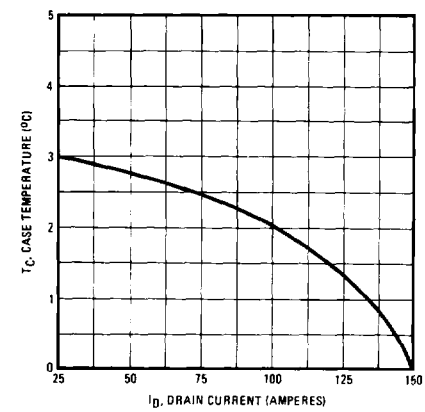


Fig. 13 - Maximum drain current versus case temperature.

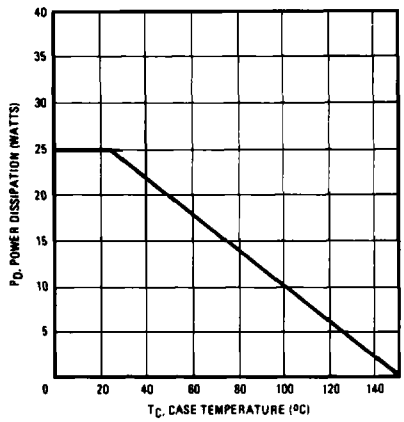


Fig. 14 - Power versus temperature derating curve.

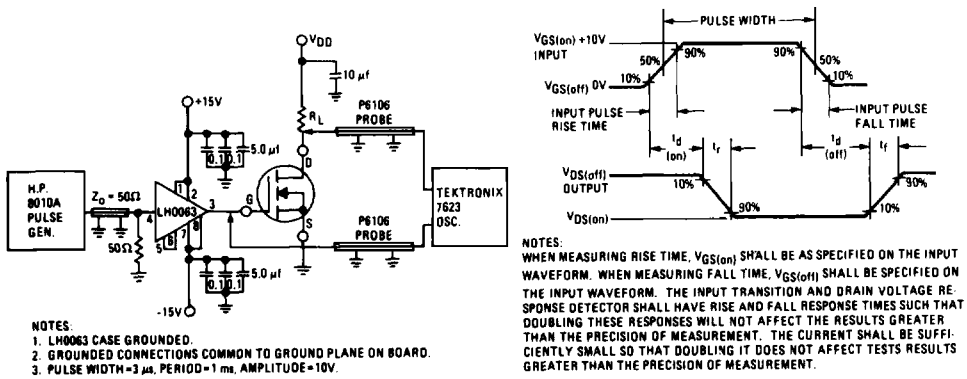


Fig. 15 - Switching time test circuit.

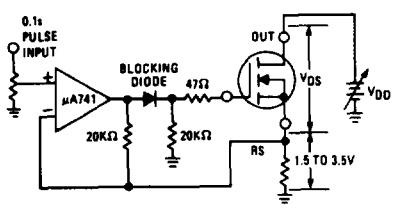


Fig. 16 - Safe operating test circuit.