

32,768 WORD x 8 Bit CMOS Static RAM (Industrial Temperature Range Operation)

FEATURES

- Industrial Temperature Range : -40 to 85° C
- Fast Access Time: 70, 100ns(max.)
- Low Power Dissipation
 - Standby (CMOS) : 275 μ W(max.)
 - Operating : 110mW(max.)
- Single 5V $\pm$ 10% power supply
- TTL compatible inputs and outputs
- Fully Static Operation
 - No clock or refresh required
- Three State Output
- Low Data Retention Voltage: 2V(Min.)
- Jedec Standard Pin Configuration
 - KM62256BLPI : 28-DIP-600B
 - KM62256BLGI : 28-SOP-450

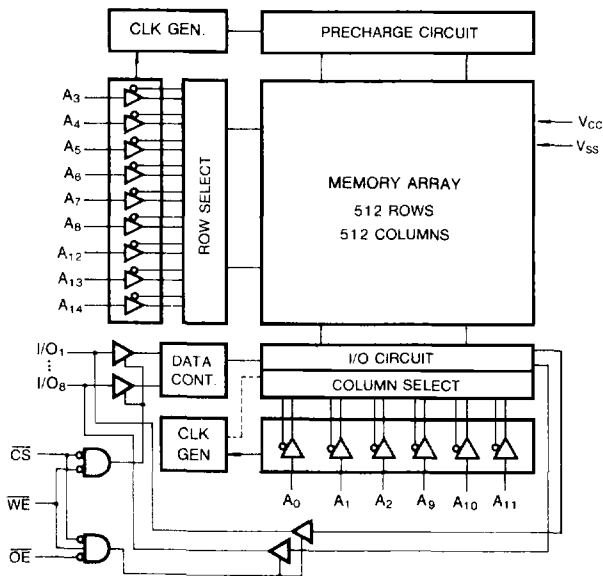
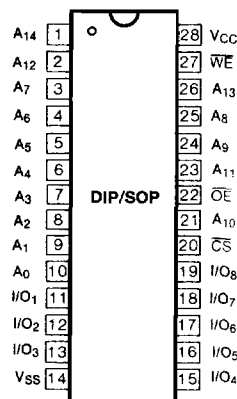
GENERAL DESCRIPTION

The KM62256BLI/BLI-L is a 262,144-bit high speed Static Random Access Memory organized as 32,768 words by 8 bits.

The device is fabricated using Samsung's advanced CMOS technology.

The KM62256BLI/BLI-L has been designed for high speed and low power applications. It is particularly well suited for battery back-up memory application.

And -40 to 85° C operating temperature range makes it ideal for industrial use.

FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION (Top Views)


Pin Name	Pin Function
A ₀ -A ₁₄	Address Inputs
WE	Write Enable
CS	Chip Select I
OE	Output Enable
I/O ₁ ~I/O ₈	Data Inputs/Outputs
V _{CC}	Power(+5V)
V _{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to 7.0	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-0.5 to 7.0	V
Power Dissipation	P _D	1.0	W
Storage Temperature	T _{STG}	-65 to + 150	°C
Operating Temperature	T _A	-40 to 85	°C
Soldering Temperature and Time	T _{SOLDER}	260°C, 10sec(Lead only)	—

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=-40 to 85°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	---	V _{CC} +0.5	V
Input Low Voltage	V _{IL}	-0.5	---	0.8	V

* V_{IL}(min.)=-3.0V for ≤ 50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=-40 to 85°C, V_{CC}=5V ± 10%, unless otherwise specified)

Item	Symbol	Test Condition	Min	Typ*	Max	Unit
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1		1	μA
Output Leakage Current	I _{LO}	$\overline{CS}=V_{IN}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{I/O} =V _{SS} to V _{CC}	-1		1	μA
Operating Power Supply Current	I _{CC}	$\overline{CS}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} , I _{I/O} =0mA		7	20	mA
Average Operating Current	I _{CC1}	Cycle Time=1μs, $\overline{CS} \leq 0.2V$, V _{IL} ≤ 0.2V V _{IH} ≥ V _{CC} -0.2V, I _{I/O} =0mA			10	mA
	I _{CC2}	$\overline{CS}=V_{IL}$, Min Cycle, 100% Duty I _{I/O} =0mA			70	mA
Standby Power Supply Current	I _{SB}	$\overline{CS}=V_{IH}$			2	mA
	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, V _{IN} ≥ V _{CC} -0.2V	L-Ver		100	μA
		or V _{IN} ≤ 0.2V	LL-Ver		20	μA
Output Low Voltage	V _{OL}	I _{OL} =2.1mA			0.4	V
Output High Voltage	V _{OH}	I _{OH} =-1.0mA	2.2			V

* Typ : V_{CC}=5V, T_A=25°C

CAPACITANCE (f=1MHz, TA=25 C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	6	pF
Input/Output Capacitance	Ci/O	Vi/O=0V	-	8	pF

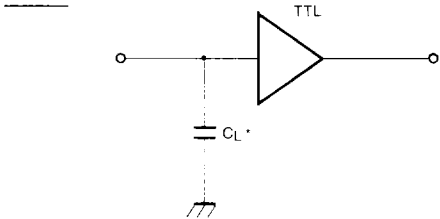
* Note : Capacitance is sampled and not 100% tested.

TEST CONDITIONS (TA=-40 to 85°C, Vcc=5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	CL=100pF+1TTL Load

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TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM62256BLI-7 KM62256BLGI-7		KM62256BLI-10 KM62256BLGI-10		Unit
		Min	Max	Min	Max	
Read Cycle Time	trc	70		100		ns
Address Access Time	tAA		70		100	ns
Chip Select to Output	tCO		70		100	ns
Output Enable to Valid Output	tOE		35		50	ns
Chip Select to Low-Z Output	tLZ	10		10		ns
Output Enable to Low-Z Output	tOLZ	5		5		ns
Chip Deselect to High-Z Output	tHZ	0	30	0	35	ns
Output Disable to High-Z Output	tOHZ	0	30	0	35	ns
Output Hold from Address Change	tOH	5		10		ns

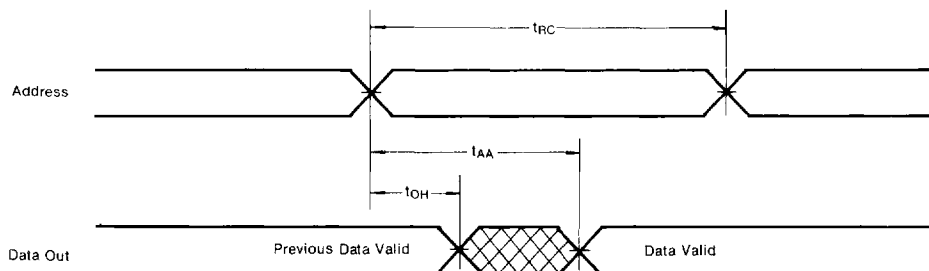
WRITE CYCLE

Parameter	Symbol	KM62256BLI-7		KM62256BLI-10		Unit
		Min	Max	Min	Max	
Write Cycle Time	t _{WC}	70		100		ns
Chip Select to End of Write	t _{CW}	60		80		ns
Address Set-up Time	t _{AS}	0		0		ns
Address Valid to End of Write	t _{AW}	60		80		ns
Write Pulse Width	t _{WP}	50		60		ns
Write Recovery Time	t _{WR}	0		0		ns
Write to Output High-Z	t _{WHZ}	0	25	0	35	ns
Data to Write Time Overlap	t _{DW}	30		50		ns
Data Hold from Write Time	t _{DH}	0		0		ns
End Write to Output Low-Z	t _{OW}	5		10		ns

TIMING DIAGRAMS

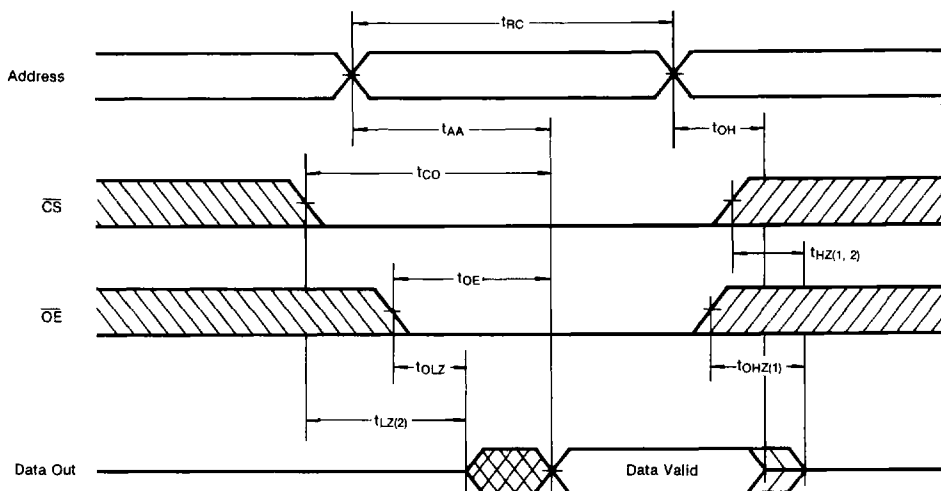
TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}=\overline{OE}$, V_{IL} , $\overline{WE}=V_{IH}$)



TIMING WAVEFORM OF READ CYCLE (2)

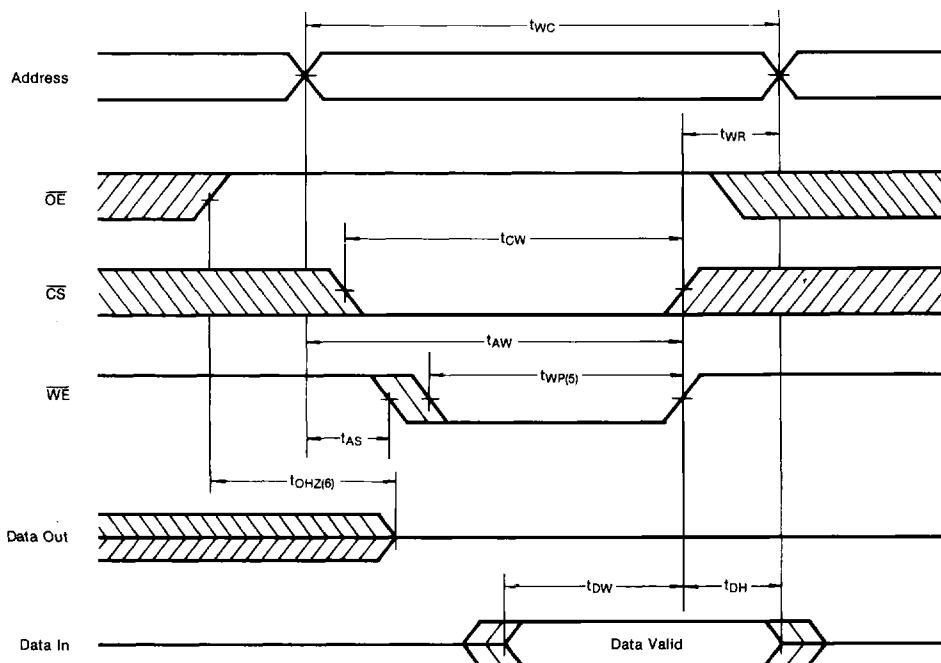
($\overline{WE} = V_{IH}$) (Note 1, 2, 3, 4)

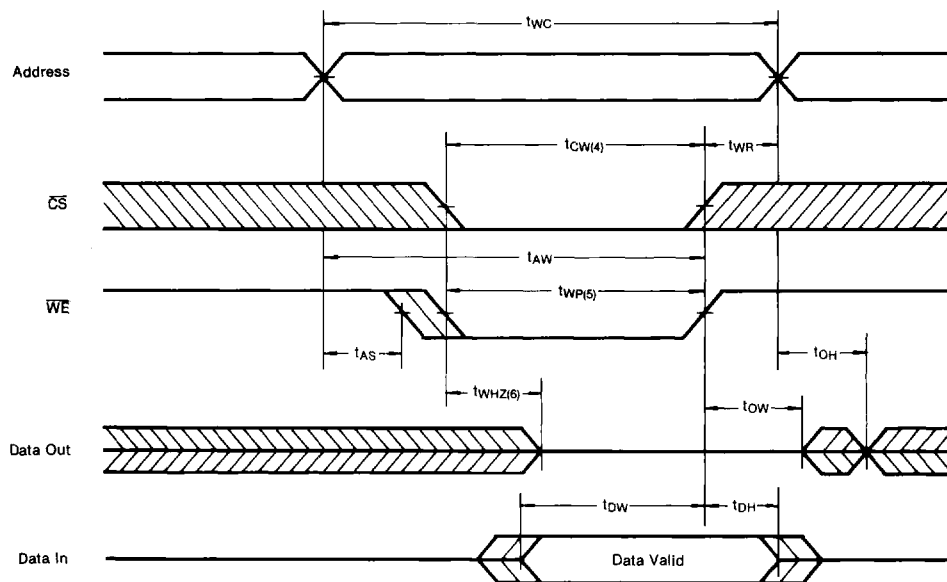


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TIMING WAVEFORM OF WRITE CYCLE (3)

($\overline{OE}$ Clocked) (Note 5, 6, 7, 8)



TIMING WAVEFORM OF WRITE CYCLE (4)($\overline{OE}$ Low Fixed) (Note 5, 6, 7, 8, 9)**Notes**

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} level.
2. At any given temperature and voltage condition t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.
5. A write occurs during the overlap (t_{WR}) of a low $\overline{CS}$ and $\overline{WE}$.
6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
7. $\overline{CS}$ or $\overline{WE}$ must be high during address transition state.
8. If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.
9. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).

FUNCTIONAL DESCRIPTION

C $\overline{S}$	WE	O $\overline{E}$	Mode	I/O Pin	Vcc Current
H	X*	X	Power down	High-Z	I _{SB} , I _{SB1}
L	H	H	Output disable	High-Z	I _{CC}
L	H	L	Read	DOUT	I _{CC}
L	L	X	Write	DIN	I _{CC}

* X means Don't Care

DATA RETENTION CHARACTERISTICS (TA=-40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for Data Retention	VDR	$\overline{CS}1 \geq V_{CC}-0.2V$	2.0		5.5	V
Data Retention Current	IDR	$V_{CC} \geq 3.0V$ $\overline{CS} \geq V_{CC}-0.2V$	L	-	50	μA
			LL	-	10	μA
Data Retention Set-up Time	tSDR	See Data Retention	0			ns
Recovery Time	tRDR	Waveforms(below)	t _{RC} *			ns

* Read Cycle Time

