

Formerly Available As FSF254R4, Radiation Hardened, SEGR Resistant, N-Channel Power MOSFETs

The Discrete Products Operation of Fairchild has developed a series of Radiation Hardened MOSFETs specifically designed for commercial and military space applications. Enhanced Power MOSFET immunity to Single Event Effects (SEE), Single Event Gate Rupture (SEGR) in particular, is combined with 100K RADS of total dose hardness to provide devices which are ideally suited to harsh space environments. The dose rate and neutron tolerance necessary for military applications have not been sacrificed.

The Fairchild portfolio of SEGR resistant radiation hardened MOSFETs includes N-Channel and P-Channel devices in a variety of voltage, current and on-resistance ratings. Numerous packaging options are also available.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to be radiation tolerant. The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

Also available at other radiation and screening levels. See us on the web, Fairchild' home page: www.fairchildsemi.com. Contact your local Fairchild Sales Office for additional information.

Ordering Information

PART NUMBER	PACKAGE	BRAND
JANSR2N7407	TO-254AA	JANSR2N7407

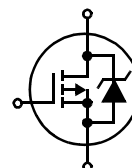
Die Family TA17658.

MIL-PRF-19500/634.

Features

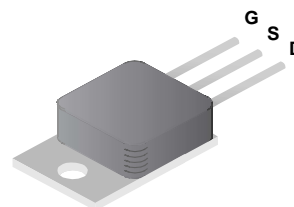
- 18A, 250V, $r_{DS(ON)} = 0.170\Omega$
- Total Dose
 - Meets Pre-RAD Specifications to 100K RAD (Si)
- Single Event
 - Safe Operating Area Curve for Single Event Effects
 - SEE Immunity for LET of 36MeV/mg/cm^2 with V_{DS} up to 80% of Rated Breakdown and V_{GS} of 10V Off-Bias
- Dose Rate
 - Typically Survives $3\text{E}9$ RAD (Si)/s at 80% BV_{DSS}
 - Typically Survives $2\text{E}12$ if Current Limited to I_{DM}
- Photo Current
 - 15nA Per-RAD(Si)/s Typically
- Neutron
 - Maintain Pre-RAD Specifications for $1\text{E}13$ Neutrons/ cm^2
- Usable to $1\text{E}14$ Neutrons/ cm^2

Symbol



Packaging

TO-254AA



CAUTION: Beryllia Warning per MIL-S-19500 refer to package specifications.

JANSR2N7407

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	JANSR2N7407	UNITS
Drain to Source Voltage V_{DS}	250	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) V_{DGR}	250	V
Continuous Drain Current		
$T_C = 25^\circ\text{C}$ I_D	18	A
$T_C = 100^\circ\text{C}$ I_D	12	A
Pulsed Drain Current I_{DM}	54	A
Gate to Source Voltage V_{GS}	± 20	V
Maximum Power Dissipation		
$T_C = 25^\circ\text{C}$ P_T	125	W
$T_C = 100^\circ\text{C}$ P_T	50	W
Linear Derating Factor	1.00	W/ $^\circ\text{C}$
Single Pulsed Avalanche Current, $L = 100\mu\text{H}$, (See Test Figure) I_{AS}	54	A
Continuous Source Current (Body Diode) I_S	18	A
Pulsed Source Current (Body Diode) I_{SM}	54	A
Operating and Storage Temperature T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Lead Temperature (During Soldering) T_L	300	$^\circ\text{C}$
(Distance $>0.063\text{in}$ (1.6mm) from Case, 10s Max)		
Weight (Typical)	9.3	g

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 1\text{mA}$, $V_{GS} = 0\text{V}$	250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 1\text{mA}$	$T_C = -55^\circ\text{C}$	-	5.0	V
			$T_C = 25^\circ\text{C}$	1.5	4.0	V
			$T_C = 125^\circ\text{C}$	0.5	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 200\text{V}$, $V_{GS} = 0\text{V}$	$T_C = 25^\circ\text{C}$	-	25	μA
			$T_C = 125^\circ\text{C}$	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	$T_C = 25^\circ\text{C}$	-	100	nA
			$T_C = 125^\circ\text{C}$	-	200	nA
Drain to Source On-State Voltage	$V_{DS(ON)}$	$V_{GS} = 12\text{V}$, $I_D = 18\text{A}$	-	-	3.21	V
Drain to Source On Resistance	$r_{DS(ON)12}$	$I_D = 12\text{A}$, $V_{GS} = 12\text{V}$	$T_C = 25^\circ\text{C}$	-	0.120	Ω
			$T_C = 125^\circ\text{C}$	-	0.306	Ω
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 125\text{V}$, $I_D = 18\text{A}$, $R_L = 6.94\Omega$, $V_{GS} = 12\text{V}$, $R_{GS} = 2.35\Omega$	-	-	130	ns
Rise Time	t_r		-	-	160	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	160	ns
Fall Time	t_f		-	-	65	ns
Total Gate Charge (Not on slash sheet)	$Q_g(TOT)$	$V_{GS} = 0\text{V}$ to 20V	$V_{DD} = 125\text{V}$, $I_D = 18\text{A}$	-	230	nC
Gate Charge at 12V	$Q_g(12)$	$V_{GS} = 0\text{V}$ to 12V		120	150	nC
Threshold Gate Charge (Not on slash sheet)	$Q_g(TH)$	$V_{GS} = 0\text{V}$ to 2V		-	7.6	nC
Gate Charge Source	Q_{gs}			22	28	nC
Gate Charge Drain	Q_{gd}			56	71	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	1.00	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	48	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 18A$	0.6	-	1.8	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 18A$, $dI_{SD}/dt = 100A/\mu s$	-	-	690	ns

Electrical Specifications up to 100K R A $D_C = 25^\circ C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Drain to Source Breakdown Volts (Note 3)	BV_{DSS}	$V_{GS} = 0$, $I_D = 1mA$	250	-	V
Gate to Source Threshold Volts (Note 3)	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 1mA$	1.5	4.0	V
Gate to Body Leakage (Notes 2, 3)	I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	-	100	nA
Zero Gate Leakage (Note 3)	I_{DSS}	$V_{GS} = 0$, $V_{DS} = 200V$	-	25	μA
Drain to Source On-State Volts (Notes 1, 3)	$V_{DS(ON)}$	$V_{GS} = 12V$, $I_D = 18A$	-	3.21	V
Drain to Source On Resistance (Notes 1, 3)	$r_{DS(ON)12}$	$V_{GS} = 12V$, $I_D = 12A$	-	0.170	Ω

NOTES:

1. Pulse test, 300 μs Max.
2. Absolute value.
3. Insitu Gamma bias must be sampled for both $V_{GS} = 12V$, $V_{DS} = 0V$ and $V_{GS} = 0V$, $V_{DS} = 80\% BV_{DSS}$.

Single Event Effects (SEB, SEGR) Note 4

TEST	SYMBOL	ENVIRONMENT (NOTE 5)			APPLIED V_{GS} BIAS (V)	(NOTE 6) MAXIMUM V_{DS} BIAS (V)
		ION SPECIES	TYPICAL LET (MeV/mg/cm)	TYPICAL RANGE (μ)		
Single Event Effects Safe Operating Area	SEESOAS	Ni	26	43	-20	250
		Br	37	36	-5	250
		Br	37	36	-10	200
		Br	37	36	-15	125
		Br	37	36	-20	50

NOTES:

4. Testing conducted at Brookhaven National Labs; sponsored by Naval Surface Warfare Center (NSWC), Crane, IN.
5. Fluence = 1E5 ions/cm² (typical), $T_C = 25^\circ C$.
6. Does not exhibit Single Event Burnout (SEB) or Single Event Gate Rupture (SEGR).

Typical Performance Curves Unless Otherwise Specified

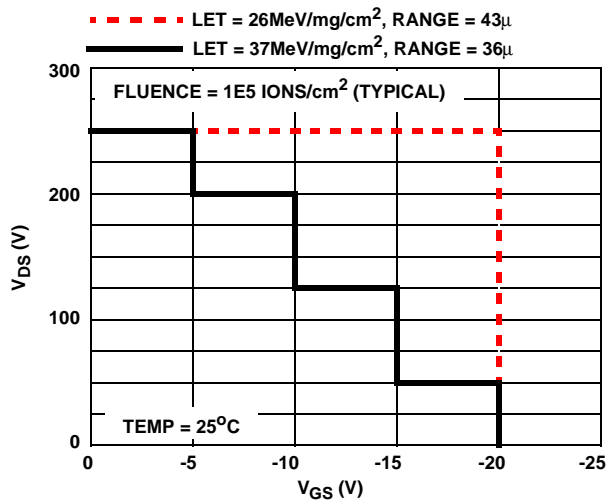
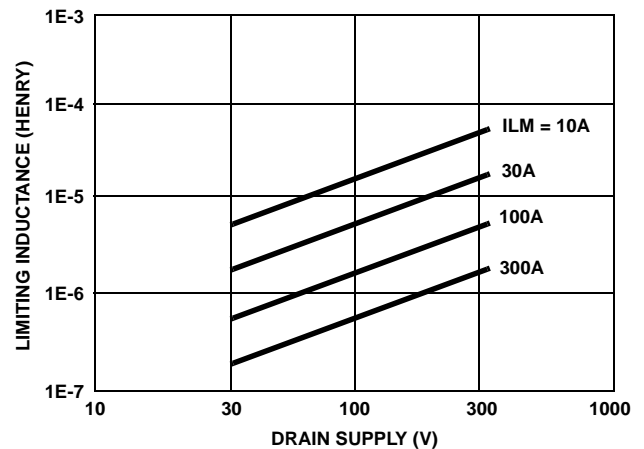


FIGURE 1. SINGLE EVENT EFFECTS SAFE OPERATING AREA

FIGURE 2. DRAIN INDUCTANCE REQUIRED TO LIMIT GAMMA DOT CURRENT TO I_{AS}

Typical Performance Curves Unless Otherwise Specified (Continued)

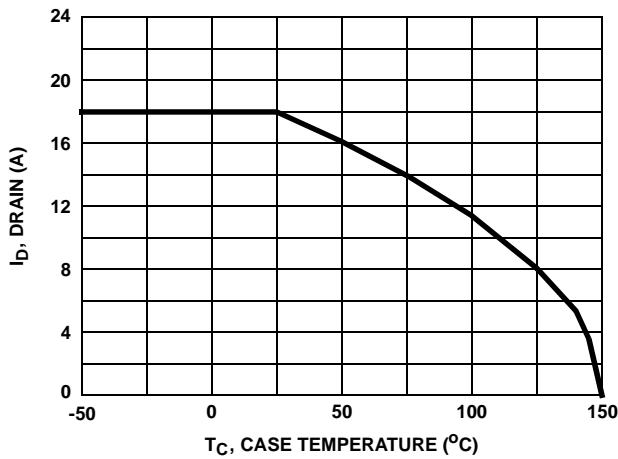


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

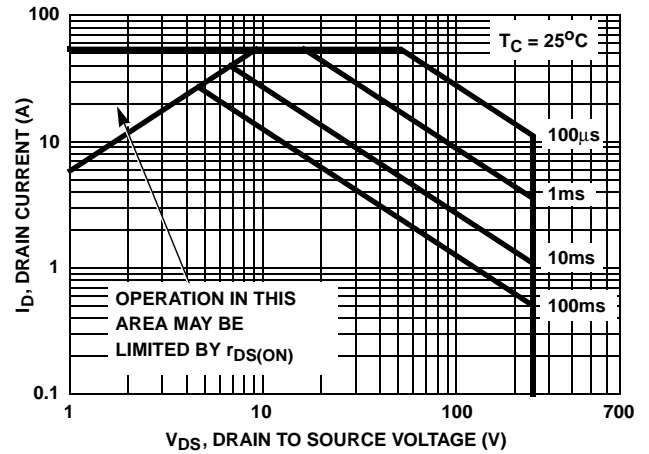


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

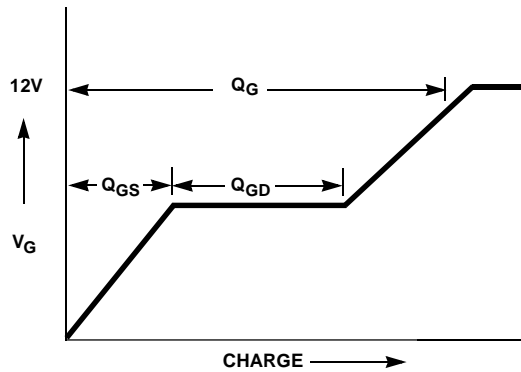


FIGURE 5. BASIC GATE CHARGE WAVEFORM

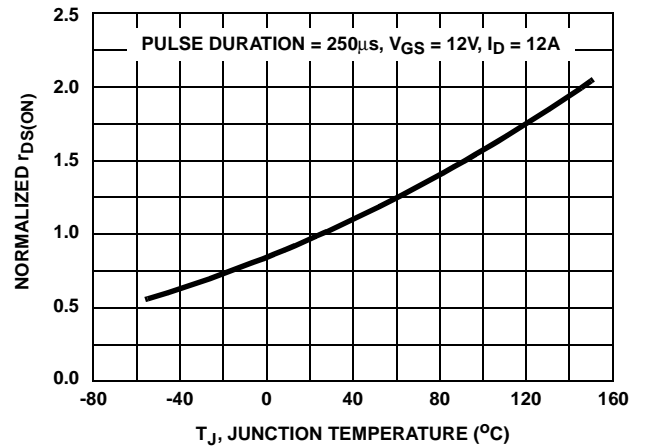


FIGURE 6. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

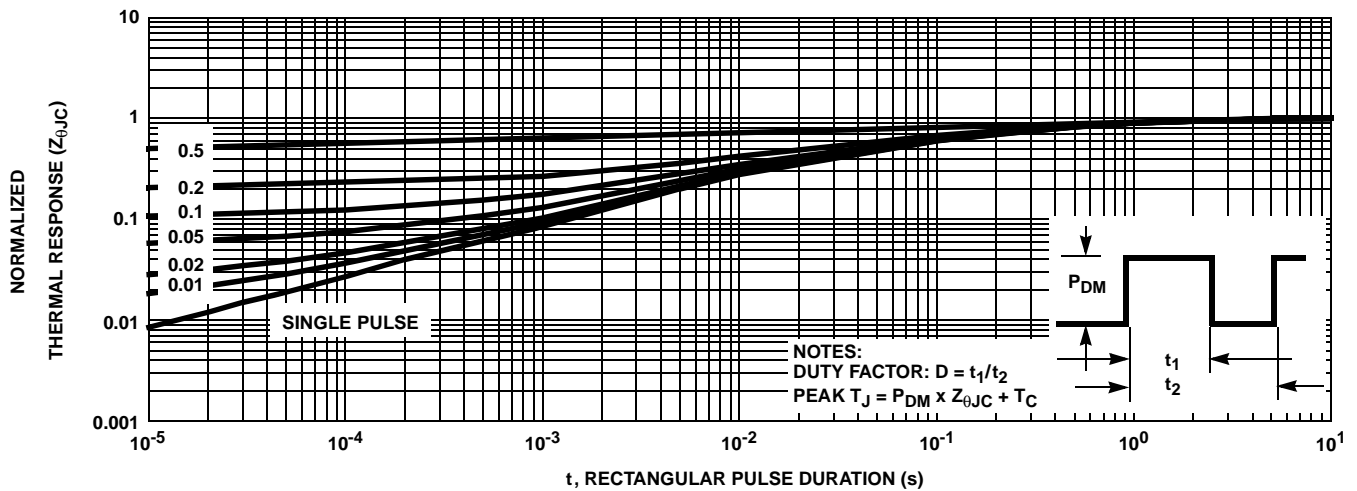


FIGURE 7. NORMALIZED MAXIMUM TRANSIENT THERMAL RESPONSE

Typical Performance Curves Unless Otherwise Specified (Continued)

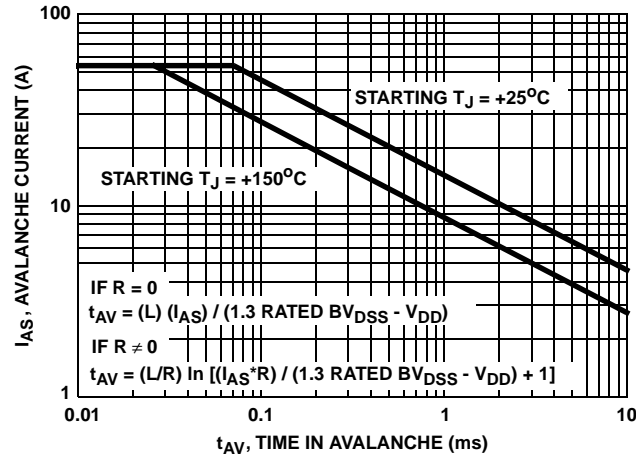


FIGURE 8. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

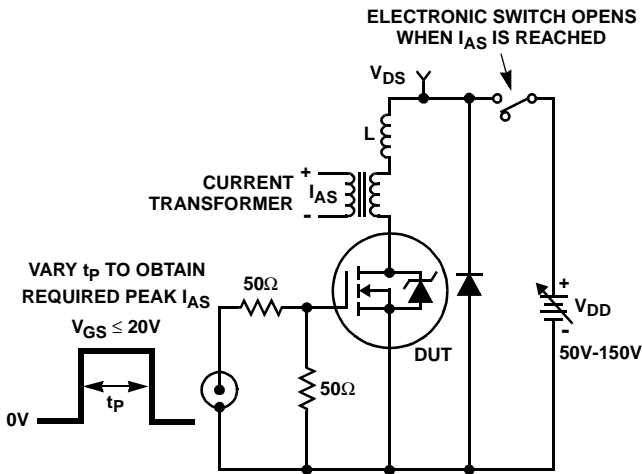


FIGURE 9. UNCLAMPED ENERGY TEST CIRCUIT

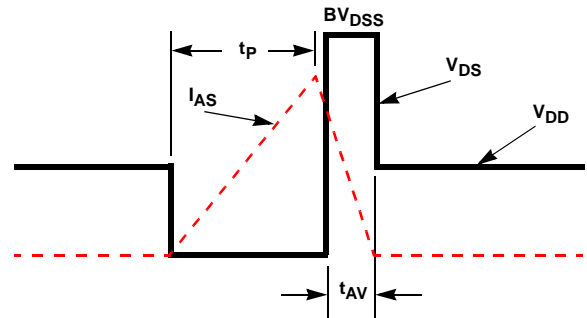


FIGURE 10. UNCLAMPED ENERGY WAVEFORMS

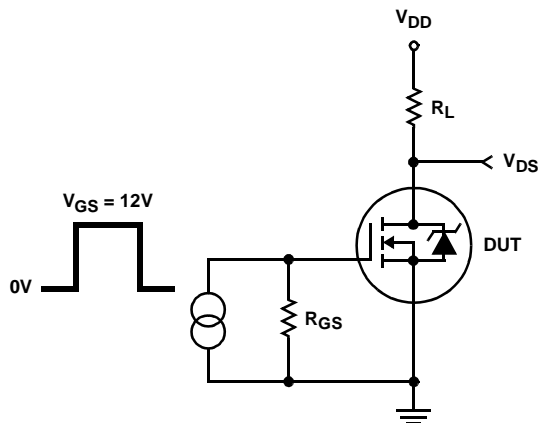


FIGURE 11. RESISTIVE SWITCHING TEST CIRCUIT

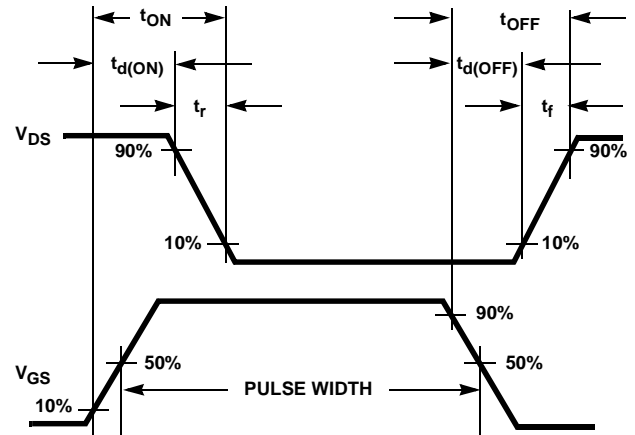


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

Screening Information

Screening is performed in accordance with the latest revision in effect of MIL-S-19500, (Screening Information Table).

Delta Tests and Limits (JANS) $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	± 20 (Note 7)	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\%$ Rated Value	± 25 (Note 7)	μA
Drain to Source On Resistance	$r_{DS(ON)}$	$T_C = 125^{\circ}\text{C}$ at Rated I_D	$\pm 20\%$ (Note 8)	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	$I_D = 1.0\text{mA}$	$\pm 20\%$ (Note 8)	V

NOTES:

7. Or 100% of Initial Reading (whichever is greater).
8. Of Initial Reading.

Screening Information

TEST	JANS
Gate Stress	$V_{GS} = 30\text{V}$, $t = 250\mu\text{s}$
Pind	Required
Pre Burn-In Tests (Note 9)	MIL-S-19500 Group A, Subgroup 2 (All Static Tests at 25°C)
Steady State Gate Bias (Gate Stress)	MIL-STD-750, Method 1042, Condition B $V_{GS} = 80\%$ of Rated Value, $T_A = 150^{\circ}\text{C}$, Time = 48 hours
Interim Electrical Tests (Note 9)	All Delta Parameters Listed in the Delta Tests and Limits Table
Steady State Reverse Bias (Drain Stress)	MIL-STD-750, Method 1042, Condition A $V_{DS} = 80\%$ of Rated Value, $T_A = 150^{\circ}\text{C}$, Time = 240 hours
PDA	5%
Final Electrical Tests (Note 9)	MIL-S-19500, Group A, Subgroups 2 and 3

NOTE:

9. Test limits are identical pre and post burn-in.

Additional Screening Tests

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safe Operating Area	SOA	$V_{DS} = 200\text{V}$, $t = 10\text{ms}$	1.35	A
Unclamped Inductive Switching	I_{AS}	$V_{GS(PEAK)} = 15\text{V}$, $L = 0.1\text{mH}$	54	A
Thermal Response	ΔV_{SD}	$t_H = 100\text{ms}$; $V_H = 25\text{V}$; $I_H = 4\text{A}$	136	mV
Thermal Impedance	ΔV_{SD}	$t_H = 500\text{ms}$; $V_H = 25\text{V}$; $I_H = 4\text{A}$	187	mV

Rad Hard Data Packages - Fairchild Power Transistors

1. JANS Rad Hard - Standard Data Package

- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report
- E. Preconditioning - Attributes Data Sheet
 - Hi-Rel Lot Traveler
 - HTRB - Hi Temp Gate Stress Post
Reverse Bias Data and Delta Data
 - HTRB - Hi Temp Drain Stress Post
Reverse Bias Delta Data
- F. Group A - Attributes Data Sheet
- G. Group B - Attributes Data Sheet
- H. Group C - Attributes Data Sheet
- I. Group D - Attributes Data Sheet

2. JANS Rad Hard - Optional Data Package

- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report
- E. Preconditioning - Attributes Data Sheet
 - Hi-Rel Lot Traveler
 - HTRB - Hi Temp Gate Stress Post
Reverse Bias Data and Delta Data
 - HTRB - Hi Temp Drain Stress Post
Reverse Bias Delta Data
 - X-Ray and X-Ray Report
- F. Group A - Attributes Data Sheet
 - Hi-Rel Lot Traveler
 - Subgroups A2, A3, A4, A5 and A7 Data
- G. Group B - Attributes Data Sheet
 - Hi-Rel Lot Traveler
 - Subgroups B1, B3, B4, B5 and B6 Data
- H. Group C - Attributes Data Sheet
 - Hi-Rel Lot Traveler
 - Subgroups C1, C2, C3 and C6 Data
- I. Group D - Attributes Data Sheet
 - Hi-Rel Lot Traveler
 - Pre and Post Radiation Data

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DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOMETM	HiSeC™	PowerTrench®	SuperSOT™-8	
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E ² CMOS™	LittleFET™	QST™	TinyLogic™	
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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