



Description

The GM71V(S)65163A/AL is the new generation dynamic RAM organized 4,196,304 words by 16 bits. The GM71V(S)65163A/AL utilizes advanced CMOS Silicon Gate Process Technology as well as advanced circuit techniques for wide operating margins, both internally and to the system user. System oriented features include single power supply of $3.3V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

The GM71V(S)65163A/AL offers Extended Data Out(EDO) Mode as a high speed access mode.

Features

- 4,196,304 Words x 16 Bit
- Extended Data Out (EDO) Mode Capability
- Fast Access Time & Cycle Time

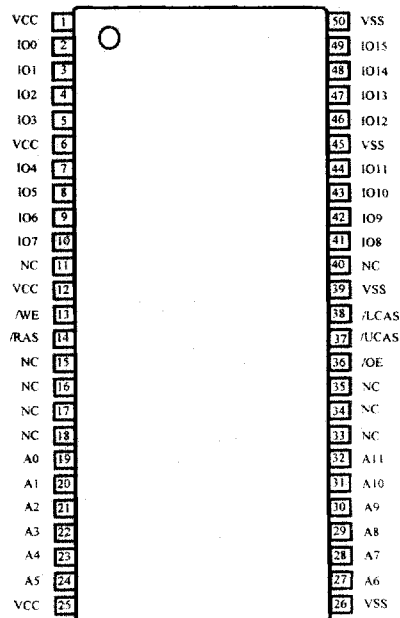
(Unit: ns)

	t_{RAC}	t_{AA}	t_{CAC}	t_{RC}	t_{HPC}
GM71V(S)65163A/AL-5	50	25	13	90	20
GM71V(S)65163A/AL-6	60	30	15	110	25

- Power dissipation
 - Active : 720mW/648mW(MAX)
 - Standby : 1.8 mW (CMOS level : MAX)
0.54mW (L-Version : MAX)
- EDO page mode capability
- Access time : 50ns/60ns (max)
- Refresh cycles
 - RAS only Refresh
 - 4096 cycles/64 μ s (GM71V65163A)
 - 4096 cycles/128 μ s (GM71VS65163AL)(L_Version)
 - CBR & Hidden Refresh
 - 4096 cycles/64 μ s (GM71V65163A)
 - 4096 cycles/128 μ s (GM71VS65163AL)(L_Version)
- 4 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh
 - Self refresh (L-Version)
- Single Power Supply of $3.3V \pm 10\%$ with a built-in VBB generator
- Battery Back Up Operation (L-Version)

Pin Configuration

50 SOJ / TSOP II



(Top View)

Pin Description

Pin	Function	Pin	Function
A0-A11	Address Inputs	$\overline{WE}$	Write Enable
A0-A11	Refresh Address Inputs	I/O0 - I/O15	Data Input / Output
$\overline{RAS}$	Row Address Strobe	V _{CC}	Power (+3.3V)
$\overline{UCAS}, \overline{LCAS}$	Column Address Strobe	V _{SS}	Ground
$\overline{OE}$	Output Enable	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71V(S)65163A/ALJ-5 GM71V(S)65163A/ALJ-6	50 _{ns} 60 _{ns}	400 Mil 50 Pin Plastic SOJ
GM71V(S)65163A/ALT-5 GM71V(S)65163A/ALT-6	50 _{ns} 60 _{ns}	400 Mil 50 Pin Plastic TSOP II

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T _{STG}	Storage Temperature (Plastic)	-55 to 125	℃
V _I	Voltage on any Pin Relative to V _{SS}	-0.5 to V _{CC} + 0.5 (MAX ; 4.6V)	V
V _{CC}	Voltage on V _{CC} Relative to V _{SS}	-0.5 to 4.6	V
I _{OUT}	Short Circuit Output Current	50	mA
P _T	Power Dissipation	1.0	W

*Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions (T_A = 0 ~ 70℃)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V _{CC}	Supply Voltage	3.0	3.3	3.6	V	1,2
V _{SS}	Supply Voltage	0	0	0	V	2
V _{IH}	Input High Voltage	2.0	-	V _{CC} +0.3	V	1
V _{IL}	Input Low Voltage	-0.3	-	0.8	V	1
T _A	Ambient Temperature under Bias	0	-	70	℃	

DC Electrical Characteristics: ($V_{CC} = 3.3V \pm 10\%$, $T_A = 0 \sim 70^\circ C$)

Symbol	Parameter	Min	Max	Unit	Note
V_{OH}	Output Level Output Level Voltage ($I_{OUT} = -2mA$)	2.4	V_{CC}	V	
V_{OL}	Output Level Output Level Voltage ($I_{OUT} = 2mA$)	0	0.4	V	
$ICC1$	Operating Current ($t_{RC} = t_{RC \min}$)	50ns	-	200	mA 1,2
		60ns	-	180	
$ICC2$	Standby Current (TTL interface) Power Supply Standby Current ($RAS, UCAS, LCAS = V_{IH}, DOUT = High-Z$)	-	2	mA	
$ICC3$	RAS-Only Refresh Current ($t_{RC} = t_{RC \min}$)	50ns	-	200	mA 2
		60ns	-	180	
$ICC4$	Extended Data Out page Mode Current ($RAS = V_{IL}, \overline{CAS}, Address \text{ Cycling: } t_{HPC} = t_{HPC \min}$)	50ns	-	120	mA 1,3
		60ns	-	110	
$ICC5$	CMOS interface ($RAS, UCAS, LCAS \geq V_{CC}-0.2V, DOUT = High-Z$)	-	0.5	mA	
	Standby Current(L_Version)	-	300	μA	4
$ICC6$	$\overline{CAS}$ -before-RAS Refresh Current ($t_{RC} = t_{RC \min}$)	50ns	-	160	mA
		60ns	-	140	
$ICC7$	Battery Back Up Operating Current(Standby with CBR) ($t_{RC}=31.25\mu s, t_{RAS}=300ns, Dout=High-Z$)	-	500	μA	4, 5
$ICC8$	Standby Current (CMOS) Power Supply Standby Current $RAS = V_{IH}, UCAS, LCAS = V_{IL}, DOUT = Enable$	-	5	mA	1
$ICC9$	Self Refresh Current ($RAS, UCAS, LCAS \leq 0.2V, Dout=High-Z$)	-	400	μA	5
I_{IL}	Input Leakage Current, Any Input ($0V \leq V_{IN} \leq V_{CC}$)	-5	5	μA	
I_{OL}	Output Leakage Current ($DOUT$ is Disabled, $0V \leq V_{OUT} \leq V_{CC}$)	-5	5	μA	

Note: 1. ICC depends on output load condition when the device is selected. $ICC(max)$ is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Measured with one sequential address change per EDO cycle, t_{HPC} .

4. $V_{IH} \geq V_{CC}-0.2V, 0V \leq V_{IL} \leq 0.2V$

5. L-version

Capacitance ($V_{CC} = 3.3V \pm 10\%$, $T_A = 25^\circ C$)

Symbol	Parameter	Typ	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	-	5	pF	1
C_{I2}	Input Capacitance (Clocks)	-	7	pF	1
$C_{I/O}$	Output Capacitance (Data-in,Data-Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

 2. $\overline{RAS}$, $\overline{UCAS}$ and $\overline{LCAS} = V_{IH}$ to disable DOUT.

AC Characteristics ($V_{CC} = 3.3V \pm 10\%$, $T_A = 0 \sim 70^\circ C$, Notes 1,2,19,20)

Test Conditions

Input rise and fall times : 2ns

 Input level : $V_{IL}/V_{IH} = 0.0/3.0V$

 Input timing reference levels : $V_{IL}/V_{IH} = 0.8/2.0V$

 Output timing reference levels : $V_{OL}/V_{OH} = 0.8/2.0V$

 Output load : 1 TTL gate+ C_L (100pF)

(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71V(S)65163A/AL-5		GM71V(S)65163A/AL-6		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	84	-	104	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	30	-	40	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	8	-	10	-	ns	24
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10000	60	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	8	10000	10	10000	ns	
t_{ASR}	Row Address Set-up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	8	-	10	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	ns	21
t_{CAH}	Column Address Hold Time	8	-	10	-	ns	21
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	12	37	14	45	ns	3
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	10	25	12	30	ns	4
t_{RSH}	$\overline{RAS}$ Hold Time	13	-	17	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	35	-	40	-	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	ns	22
t_{ODD}	$\overline{OE}$ to $\overline{DIN}$ Delay Time	13	-	15	-	ns	5
t_{DZO}	$\overline{OE}$ Delay Time from $\overline{DIN}$	0	-	0	-	ns	6
t_{DZC}	$\overline{CAS}$ Delay Time from $\overline{DIN}$	0	-	0	-	ns	6
t_T	TransitionTime (Rise and Fall)	2	50	2	50	ns	7
t_{REF}	Refresh Period	-	64	-	64	ms	4096 cycles
	Refresh Period (L-Version)	-	128	-	128	ms	4096 cycles

Read Cycles

Symbol	Parameter	GM71V(S)65163A/AL-S		GM71V(S)65163A/AL-6		Unit	Notes
		Min	Max	Min	Max		
t _{RAC}	Access Time from $\overline{\text{RAS}}$	-	50	-	60	ns	8,9
t _{CAC}	Access Time from $\overline{\text{CAS}}$	-	13	-	15	ns	9,10,17
t _{AA}	Access Time from Column Address	-	25	-	30	ns	9,11,17
t _{OAC}	Access Time from $\overline{\text{OE}}$	-	13	-	15	ns	9
t _{RCS}	Read Command Set-up Time	0	-	0	-	ns	21
t _{RCH}	Read Command Hold Time to $\overline{\text{CAS}}$	0	-	0	-	ns	12,22
t _{RRH}	Read Command Hold Time to $\overline{\text{RAS}}$	0	-	0	-	ns	12
t _{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	25	-	30	-	ns	
t _{CAL}	Column Address to $\overline{\text{CAS}}$ Lead Time	15	-	18	-	ns	
t _{OFF}	Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	-	13	-	15	ns	13,26
t _{OEZ}	Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	-	13	-	15	ns	13
t _{CDD}	$\overline{\text{CAS}}$ to D _{IN} Delay Time	13	-	15	-	ns	5
t _{RDD}	$\overline{\text{RAS}}$ to D _{IN} Delay Time	13	-	15	-	ns	
t _{WDD}	$\overline{\text{WE}}$ to D _{IN} Delay Time	13	-	15	-	ns	
t _{OFR}	Output Buffer Turn-off Delay Time from $\overline{\text{RAS}}$	-	13	-	15	ns	13,26
t _{WEZ}	Output Buffer Turn-off Delay Time from $\overline{\text{WE}}$	-	13	-	15	ns	13
t _{OH}	Output Data Hold Time	3	-	3	-	ns	26
t _{OHR}	Output Data Hold Time from $\overline{\text{RAS}}$	3	-	3	-	ns	26
t _{RCHR}	Read Command Hold Time from $\overline{\text{RAS}}$	50	-	60	-	ns	
t _{OH0}	Output data hold time from $\overline{\text{OE}}$	3	-	3	-	ns	
t _{CLZ}	$\overline{\text{CAS}}$ to Output in Low - Z	0	-	0	-	ns	

Write Cycles

Symbol	Parameter	GM71V(S)65163A/AL-5		GM71V(S)65163A/AL-6		Unit	Notes
		Min	Max	Min	Max		
twCS	Write Command Set-up Time	0	-	0	-	ns	14,21
twCH	Write Command Hold Time	8	-	10	-	ns	21
tWP	Write Command Pulse Width	8	-	10	-	ns	
trWL	Write Command to $\overline{\text{RAS}}$ Lead Time	13	-	17	-	ns	
tcWL	Write Command to $\overline{\text{CAS}}$ Lead Time	8	-	10	-	ns	23
tDS	Data-in Set-up Time	0	-	0	-	ns	15,23
tDH	Data-in Hold Time	8	-	10	-	ns	15,23

Read-Modify-Write Cycles

Symbol	Parameter	GM71V(S)65163A/AL-5		GM71V(S)65163A/AL-6		Unit	Notes
		Min	Max	Min	Max		
trWC	Read-Modify-Write Cycle Time	116	-	140	-	ns	
trWD	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	67	-	79	-	ns	14
tcWD	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	30	-	34	-	ns	14
tAWD	Column Address to $\overline{\text{WE}}$ Delay Time	42	-	49	-	ns	14
toEH	$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$	13	-	15	-	ns	

Refresh Cycles

Symbol	Parameter	GM71V(S)65163A/AL-5		GM71V(S)65163A/AL-6		Unit	Notes
		Min	Max	Min	Max		
tCSR	$\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ -before-RAS Refresh Cycle)	5	-	5	-	ns	21
tCHR	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ -before-RAS Refresh Cycle)	8	-	10	-	ns	22
tWRP	$\overline{\text{WE}}$ setup time ($\overline{\text{CAS}}$ -before-RAS Refresh Cycle)	0	-	0	-	ns	
tWRH	$\overline{\text{WE}}$ hold time ($\overline{\text{CAS}}$ -before-RAS Refresh Cycle)	8	-	10	-	ns	
trPC	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	5	-	5	-	ns	21

Extended Data Out Mode Cycles

Symbol	Parameter	GM71V(S)65163A/AL-5		GM71V(S)65163A/AL-6		Unit	Notes
		Min	Max	Min	Max		
tHPC	EDO Page Mode Cycle Time	20	-	25	-	ns	25
tWPE	Write pulse width during $\overline{\text{CAS}}$ precharge	8	-	10	-	ns	
tRASP	EDO Mode $\overline{\text{RAS}}$ Pulse Width	-	100000	-	100000	ns	16
tACP	Access Time from $\overline{\text{CAS}}$ Precharge	-	28	-	35	ns	9.17.22
tRHCP	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	28	-	35	-	ns	
tCOL	$\overline{\text{CAS}}$ Hold Time Referred $\overline{\text{OE}}$	8	-	10	-	ns	
tCOP	$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ set-up Time	5	-	5	-	ns	
tRCHP	Read Command Hold Time from $\overline{\text{CAS}}$ Precharge	28	-	35	-	ns	
tDOH	Output Data Hold Time from $\overline{\text{CAS}}$ Low	3	-	3	-	ns	9.27
tOEP	$\overline{\text{OE}}$ Precharge Time	8	-	10	-	ns	

EDO Page Mode Read-Modify-Write cycle

Symbol	Parameter	GM71V(S)65163A/AL-5		GM71V(S)65163A/AL-6		Unit	Notes
		Min	Max	Min	Max		
tHPRWC	EDO Read-Modify-Write Cycle Time	57	-	68	-	ns	
tCPW	EDO Page Mode Read-Modify-Write Cycle $\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	45	-	54	-	ns	14.22

Self Refresh Cycles (L_Version)

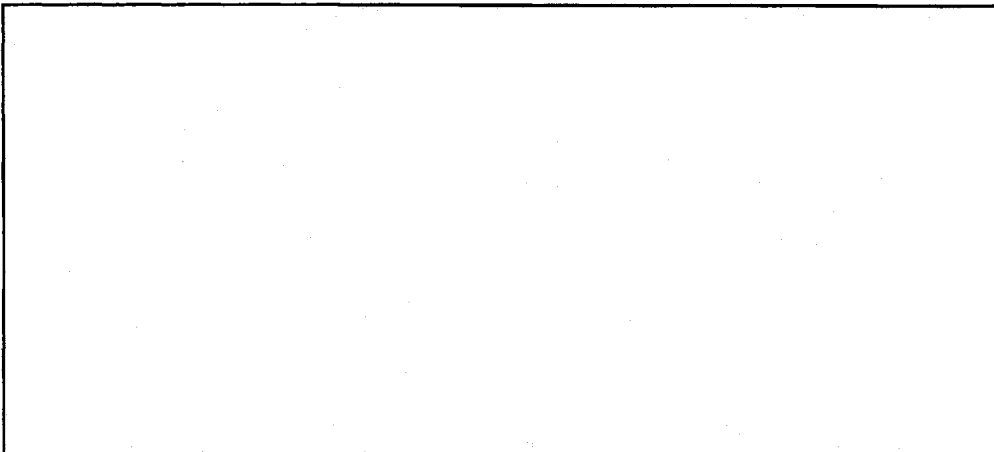
Symbol	Parameter	GM71V(S)65163A/AL-5		GM71V(S)65163A/AL-6		Unit	Notes
		Min	Max	Min	Max		
tRASS	$\overline{\text{RAS}}$ Pulse Width(Self-Refresh)	100	-	100	-	μs	31
tRPS	$\overline{\text{RAS}}$ Precharge Time(Self-Refresh)	90	-	110	-	μs	31
tCHS	$\overline{\text{CAS}}$ Hold Time(Self-Refresh)	-50	-	-50	-	μs	23

Notes:

1. AC measurements assume $t_r = 2\text{ ns}$.
2. AC initial pause of $200\mu\text{s}$ is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)
3. Operation with the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RCD}}(\text{max})$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
4. Operation with the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RAD}}(\text{max})$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
5. Either t_{ODD} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$.
8. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}}(\text{max}) \geq t_{\text{RAD}} + t_{\text{AA}}(\text{max})$.
11. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}}(\text{max}) \leq t_{\text{RAD}} + t_{\text{AA}}(\text{max})$.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. $t_{\text{OFF}}(\text{max})$, $t_{\text{OEZ}}(\text{max})$, $t_{\text{OFR}}(\text{max})$ and $t_{\text{WEZ}}(\text{max})$ define the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle: if $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell: if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. t_{DS} and t_{DH} are referred to $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in extended data out mode cycles.
17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{ACP} .
18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
19. When output buffers are enabled once, sustain the low impedance state until valid t_{dAA} is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{\text{CC}}/V_{\text{SS}}$ line noise, which causes to degrade $V_{\text{IH min}}/V_{\text{IL max}}$ level.
20. When both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ go low at the same time, all 16-bit data are written into the device. $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ cannot be staggered within the same write/read cycles.
21. t_{ASC} , t_{CAH} , t_{RCS} , t_{WCS} , t_{WCH} , t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
22. t_{CRP} , t_{CHR} , t_{RCH} , t_{ACP} and t_{CPW} are determined by the later rising edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.

23. t_{CWL} , t_{DH} , t_{DS} and t_{CHS} should be satisfied by the both $\overline{UCAS}$ and $\overline{LCAS}$.
24. t_{CP} is determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
25. $t_{HPC}(\min)$ can be achieved during a series of EDO mode early write cycles or EDO mode read cycles. If both write and read operation are mixed in a EDO mode, $\overline{RAS}$ cycle { EDO mode mix cycle (1),(2) } minimum value of $\overline{CAS}$ cycle $t_{HPC}(t_{CAS} + t_{CP} + 2t_r)$ becomes greater than the specified $t_{HPC}(\min)$ value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
26. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH} , and between t_{OFF} and t_{OFF} .
27. t_{DOH} defines the time at which the output level go cross. $V_{OL}=0.8V$, $V_{OH}=2.0V$ of output timing reference level.
28. Before and after self refresh mode, execute CBR refresh to all refresh addresses in or within 64_{ms} period on the condition a and b below.
 - a. Enter self refresh mode within $15.6_{\mu s}$ after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
 - b. Start burst refresh or distributed refresh at equal interval to all refresh addressed within $15.6_{\mu s}$ after exiting from self refresh mode.
29. In case of entering from $\overline{RAS}$ -only-refresh, it is necessary to execute CBR refresh before and after self refresh mode according as note 28.
30. For L version, it is available to apply each 128_{ms} and $31.2_{\mu s}$ instead of 64_{ms} and $15.6_{\mu s}$ at note 28.
31. At $t_{RASS} > 100_{\mu s}$, self refresh mode is activated, and not activated at $t_{RASS} < 10_{\mu s}$. It is undefined within the range of $10_{\mu s} < t_{RASS} < 100_{\mu s}$. for $t_{RASS} > 10_{\mu s}$, it is necessary to satisfy t_{RPS} .
32. XXX: H or L (H : $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$, L: $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$)
 ##### Invalid Dout
 When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

SOJ 50 PIN Package Dimension



TSOP II 50 PIN Package Dimension

