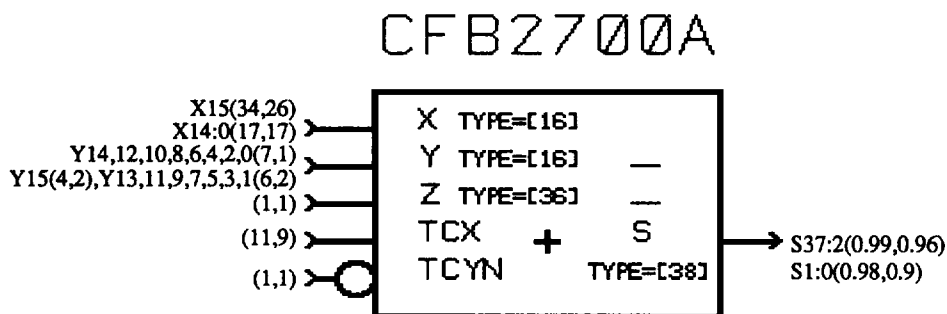**GENERAL DESCRIPTION:** 16 X 16 MIXED-MODE MAC WITH 36-BIT ADDEND

CFB2700A is a 16 x 16 mixed-mode multiplier. It has a 36-bit addend, which is unsigned and left-shifted by 0 positions. Sign interpretation of the multiplier and multiplicand is controlled by TCX and TCYN: the multiplicand is unsigned if TCX is LOW, and two's complement if it is HIGH. TCYN controls the multiplier in the OPPOSITE manner. The architecture of the multiplier can be broken down into the following modules: Booth Recoder, Wallace Tree, and Final Adder.

PIN CONNECTION DIAGRAM:

CFB2700A

```
X15(34,26)
X14:0(17,17)        X  TYPE=[16]
Y14,12,10,8,6,4,2,0(7,1)
Y15(4,2),Y13,11,9,7,5,3,1(6,2)    Y  TYPE=[16]    —
(1,1)               Z  TYPE=[36]    —
(11,9)              TCX        S         S37:2(0.99,0.96)
(1,1)               TCYN    +  TYPE=[38]            S1:0(0.98,0.9)
```

FEATURES:

- 16-bit mixed-mode multiplicand
- 16-bit mixed-mode multiplier
- 36-bit addend
- 38-bit mixed-mode result

EQUIVALENT USED GATES: 2524 GATES
(for rough area estimates)

THIS MEGAFUNCTION CONSISTS OF :
    2524 soft-coded gates.

POWER: NOT AVAILABLE.

FAULT COVERAGE(%): NOT AVAILABLE.

Copyright LSI Logic Corporation 1989, 1990

PIN DESCRIPTION:
INPUT
=====
X15:0   MULTIPLICAND MSB TO LSB.
TCX   MULTIPLICAND MODE CONTROL.
Y15:0   MULTIPLIER MSB TO LSB.
TCYN   MULTIPLIER MODE CONTROL.
Z35:0   ADDEND MSB TO LSB.
OUTPUT
======
S37:0   MAC RESULT TO LSB.

AC CHARACTERISTICS: (DELAY PREDICTED BY LPACE)

```
+---------------+-------------+---------------------------+
|  FROM         | TO          | 10K TYPICAL DELAY (ns)    |
+---------------+-------------+---------------------------+
| ANY X         | ANY S       |           34.0            |
| ANY Y         | ANY S       |           35.9            |
+---------------+-------------+---------------------------+
```
ASSUMING OUTPUT LOADING OF 2