CAT35C704

4K-Bit Secure Access Serial E²PROM

FEATURES

- Single 5V Supply
- Password READ/WRITE Protection: 1 to 8 Bytes
- Memory Pointer WRITE Protection
- Sequential READ Operation
- 256 x16 or 512 x 8 Selectable Serial Memory
- High Speed Synchronous Protocol
- Commercial and Industrial Temperature Ranges
- Operating Frequency: DC–3MHz
- Low Power Consumption:
  –Active: 3 mA
  –Standby: 250 µA
- 100,000 Program/Erase Cycles
- 100 Year Data Retention

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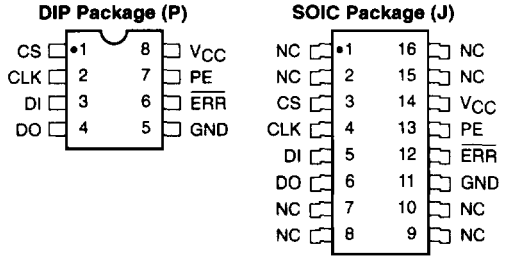
DESCRIPTION

The CAT35C704 is a 4K-bit Serial E²PROM that safeguards stored data from unauthorized access by use of a user selectable (1 to 8 byte) access code and a movable memory pointer. Two operating modes provide unprotected and password-protected operation allowing the user to configure the device as anything from a ROM to a fully protected no-access memory. The CAT35C704 uses a unique serial-byte synchronous communication protocol and has a Sequential Read feature where data can be sequentially clocked out of the memory array. The device is available in 8-pin DIP or 16-pin SOIC packages.

PIN CONFIGURATION

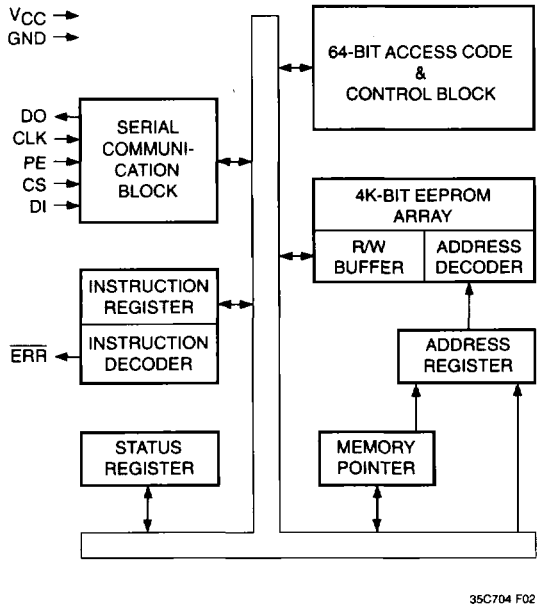


PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
DO(1)	Serial Data Output
CLK	Clock Input
DI(1)	Serial Data Input
PE	Parity Enable
$\overline{ERR}$	Error Indication Pin
VCC	+5V Power Supply
GND	Ground

Note:
(1) DI, DO may be tied together to form a common I/O.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −55°C to +125°C

Storage Temperature ..... −65°C to +150°C

Voltage on Any Pin with Respect to Ground[1] ..... −2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... −2.0V to +7.0V

Package Power Dissipation Capability (T_a = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current[2] 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}[3]	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}[3]	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}[3]	ESD Susceptability	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}[3][4]	Latch-up	100		mA	JEDEC Standard 17

D.C. CHARACTERISTICS

V_{CC} = +5V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	V_{CC} = 5.5V, CS = V_{CC} DO is Unloaded.
I_{SB}	Power Supply Current (Standby)			250	µA	V_{CC} = 5.5V, CS = 0V DI = 0V, CLK = 0V
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400µA
I_{LI}[5]	Input Leakage Current			2	µA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 5.5V, CS = 0V

Note:
(1) The minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from −1V to V_{CC} +1V.
(5) PE pin test conditions: $V_{IH} < V_{IN} < V_{IL}$

A.C. CHARACTERISTICS

V_{CC} = +5V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	150			ns	
t_{CSH}	CS Hold Time	0			ns	C_L = 100pF
t_{DIS}	DI Setup Time	50			ns	V_{IN} = V_{IH} or V_{IL}
t_{DIH}	DI Hold Time	0			ns	V_{OUT} = V_{OH} or V_{OL}
t_{PD}	CLK to DO Delay			150	ns	
t_{HZ}(1) (2)	CLK to DO High-Z Delay			50	ns	
t_{EW}	Program/Erase Pulse Width			12	ms	
t_{CSL}	CS Low Pulse Width	200			ns	
t_{CKH}	CLK High Pulse Width	165			ns	
t_{CKL}	CLK Low Pulse Width	100			ns	
t_{SV}	$\overline{ERR}$ Output Delay			150	ns	C_L = 100pF
t_{VCCS}(1)	V_{CC} to CS Setup Time	5			µs	C_L = 100pF
t_{CSZ}(1)	CS to DO High-Z Delay			50	ns	
t_{CSD}	CS to DO Busy Delay			150	ns	
f_{CLK}	Clock Frequency	DC		3	MHz	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{HZ} is measured from the falling edge of the clock to the time when the output is no longer driven.

PASSWORD PROTECTION

The CAT35C704 is a 4K-bit E^2PROM that features a password protection scheme to prevent unauthorized access to the information stored in the device. It contains an access code register which stores one to eight bytes of access code along with the length of that access code. Additionally, a memory pointer register stores the address that partitions the memory into protected and unprotected areas. As shipped from the factory, the device is unprogrammed and unprotected. The length of the access code is equal to zero and the memory pointer register points to location zero. Every byte of the device is fully accessible without an access code. Setting a password and moving the memory pointer register to cover all or part of the memory secures the device. Once secured, the memory is divided into a read/write area and a read-only area with the entry of a valid access code. If no access code is entered, the memory is divided into a read-only area and a non-access area. Figure 2 illlustrates this partitioning of the memory array.

WRITE PROTECTION

Another feature of the CAT35C704 is WRITE-protection without the use of an access code. If the memory pointer register is set to cover all or part of the memory, without setting the access code register, the device may be divided into an area which allows full access, and an area which allows READ-only access. To write into the READ-only area, the user can override the memory pointer register for every WRITE instruction or he can simply move the address in the memory pointer register to uncover this area, and then write into the memory. This mechanism prevents inadvertent overwriting of important data in the memory without the use of an access code. Figure 3 illustrates this partitioning of the memory array.

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Figure 1. A.C. Timing

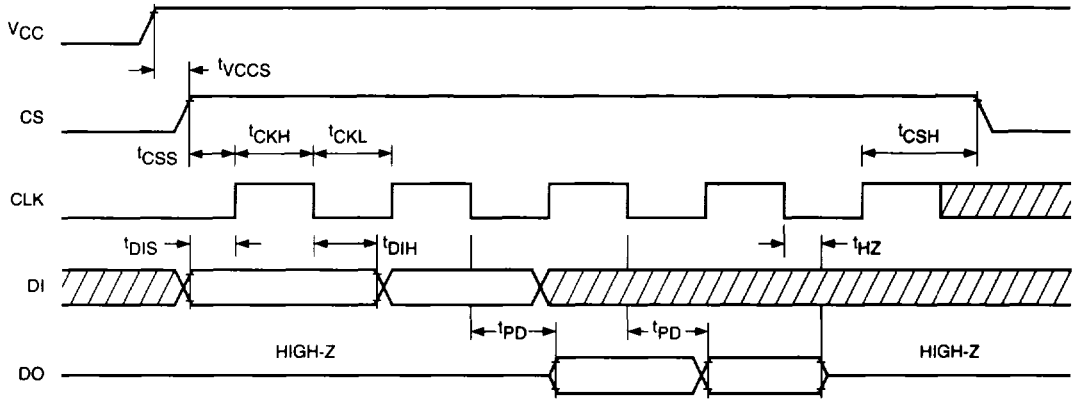
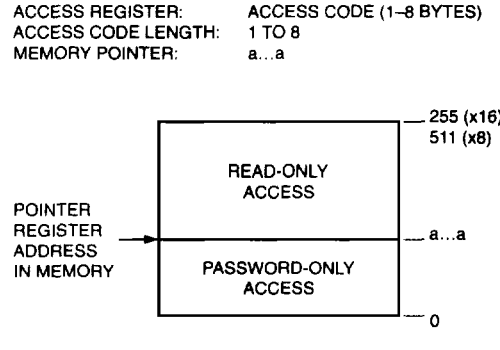


Figure 2. Secure Mode



READ SEQUENTIAL

To allow for convenient reading of blocks of contiguous data, the device has a READ SEQUENTIAL instruction which accepts a starting address of the block and continuously outputs data of subsequent addresses until the end of memory, or until Chip Select goes LOW.

The CAT35C704 communicates with external devices via a synchronous serial communication protocol (SECS) that has a maximum transmission rate of 3 MHz. The data transmission may be a continuous stream of data or it can be packed by pulsing Chip Select LOW in between each packet of information. (Except for the SEQUENTIAL READ instruction where Chip Select must be held high).

PIN DESCRIPTIONS

CS

Chip Select is a TTL compatible input which, when set HIGH, allows normal operation of the device. Any time Chip Select is set LOW, it resets the device, terminating all I/O communication, and puts the output in a high impedance state. CS is used to reset the device if an error condition exists or to put the device in a power-down mode to minimize power consumption. It may also be used to frame data transmission in applications where the clock and data input have to be ignored from time to time. Although CS resets the device, it does not change the program/erase or the access-enable status, nor does it terminate a programming cycle once it has started. The program/erase and access-enable operations, once enabled, will remain enabled until specific disabling instructions are sent or until power is removed.

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Figure 3. Unprotected Mode(1)

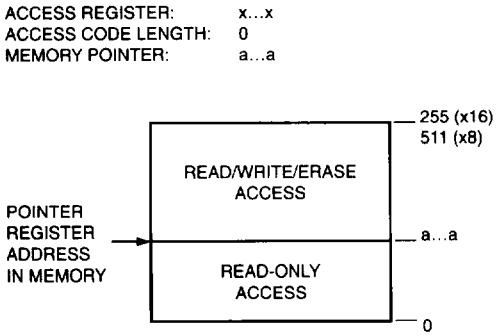

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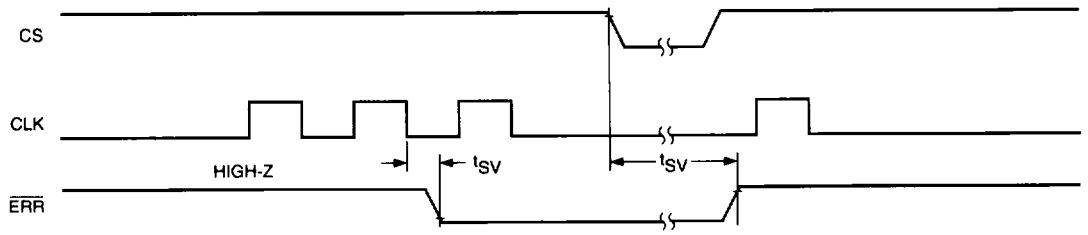
Figure 4. $\overline{ERR}$ Pin Timing



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Note:
(1) x = DON'T CARE; a = ADDRESS BIT.

CLK

The System Clock is a TTL compatible input pin that allows operation of the device over a frequency range of DC to 3 MHz.

DI

The Data Input pin is TTL compatible and accepts data and instructions in a serial format. Each instruction must begin with "1" as a start bit. The device will accept as many bytes as an instruction requires, including both data and address bytes. With the SECS protocol, extra bits will be disregarded if they are "0"s and misinterpreted as the next instruction if they are "1"s. An instruction error will cause the device to abort operation and all I/O communication will be terminated until a reset is received.

DO

The Data Output pin is a tri-state TTL compatible output. It is normally in a high impedance state unless a READ or an ENABLE BUSY instruction is executed. Following the completion of a 16-bit or 8-bit data stream, the output will return to the high impedance state. During a program/erase cycle, if the ENABLE BUSY instruction has been previously executed, the output will stay LOW while the device is BUSY, and it will be set HIGH when the program/erase cycle is completed. DO will stay HIGH until the completion of the next instruction's opcode and, if the next instruction is a READ, DO will output the appropriate data at the end of the instruction. If the ENABLE BUSY instruction has not been previously executed, DO will stay in a high impedance state. DO will

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Figure 5. Program/Erase Timing

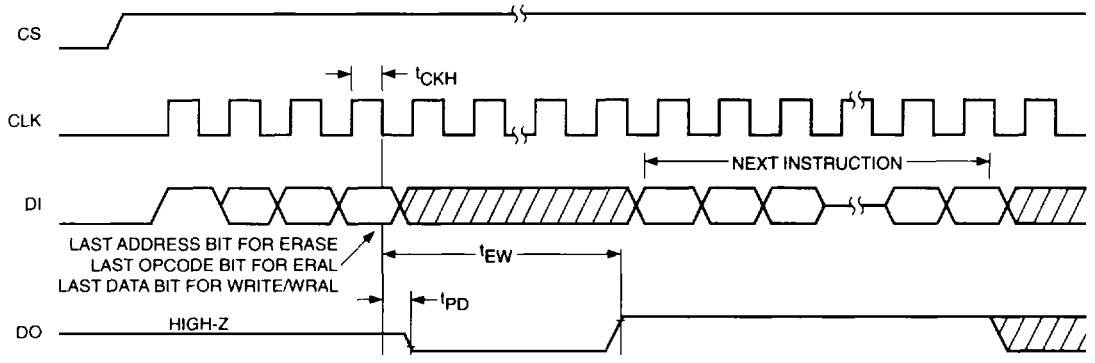
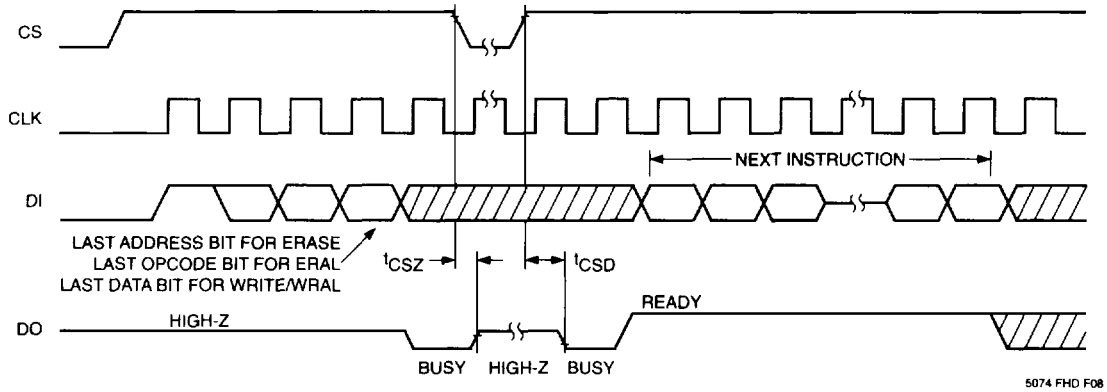


Figure 6. CS to DO Status Timing



also go to the high impedance state if an error condition is detected. If the ENABLE BUSY instruction has not been executed, to determine whether the device is in a program/erase cycle or in an error condition, a READ STATUS instruction may be entered. When the device is in a program/erase cycle it will output an 8-bit status word. If it does not, it is in an error condition.

PE

The Parity Enable pin is a TTL compatible input. If the PE pin is set HIGH, the device will be configured to communicate using even parity, and if the pin is set LOW, it will use no parity. In this case, instructions or data that include parity bits will not be interpreted correctly. Note: The PE input is internally pulled down to GND (i.e. default = no parity). As with all CMOS devices, CS, CLK and DI inputs must be connected to either HIGH or LOW, and not left floating.

$\overline{ERR}$

The Error indication pin is an open drain output. If either an instruction or parity error exists, the $\overline{ERR}$ pin will output a "0" until the device is reset. This can be done by pulsing CS LOW.

Figure 7. Read Timing

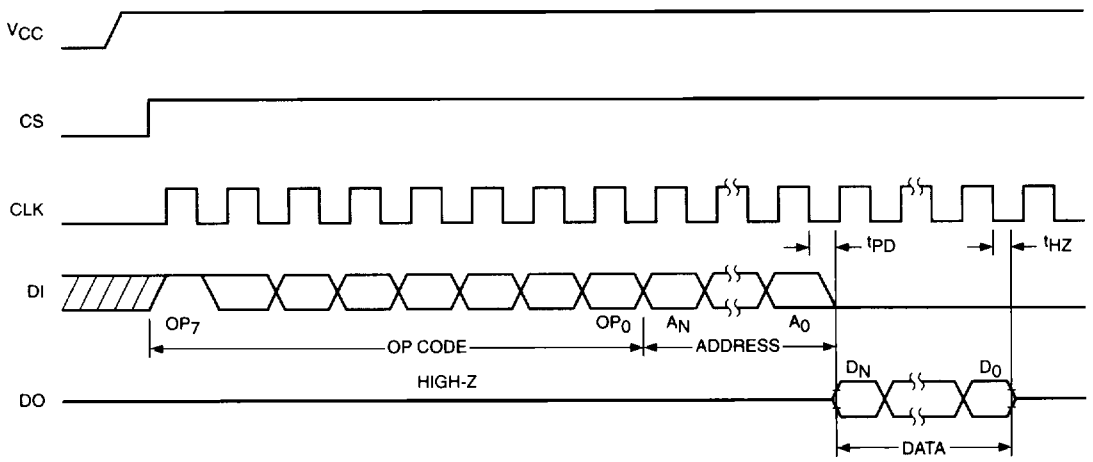


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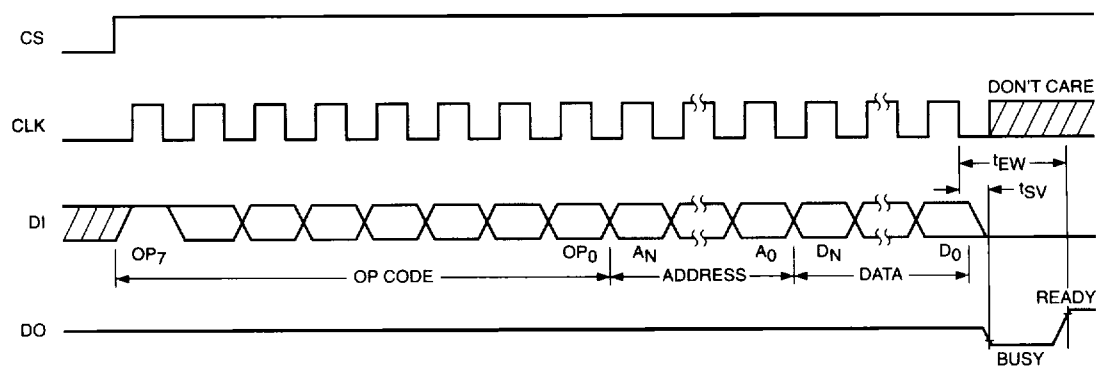
Figure 8. Write Timing



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DEVICE OPERATION

INSTRUCTIONS

The CAT35C704 instruction set includes 19 instructions.

Six instructions are related to security or write protection:

DISAC	Disable Access
ENAC	Enable Access
MACC	Modify Access Code
OVMPR	Override Memory Pointer Register
RMPR	Read Memory Pointer Register
WMPR	Write Memory Pointer Register

Six instructions are READ/WRITE/ERASE instructions:

ERAL	Clear All Locations
ERASE	Clear Memory Locations
READ	Read Memory
RSEQ	Read Sequentially
WRAL	Write All
WRITE	Write memory

Note: All write instructions will automatically perform a clear before writing data.

Seven instructions are used as control and status functions:

DISBSY	Disable Busy
ENBSY	Enable Busy
EWEN	Program/Erase Enable
EWDS	Program/Erase Disable
NOP	No Operations
ORG	Select Memory Organization
RSR	Read Status Register

UNPROTECTED MODE

As shipped from the factory, the CAT35C704 is in the unprotected mode. The access code length is set to 0, and the memory pointer is at address 00 hex. While in this mode, any portion of the E^2PROM array can be read or written to without an access code. A portion of the memory may be protected from any write or clear operation by setting the memory pointer to the appropriate address via the WMPR (Write Memory Pointer Register) instruction:

WMPR [address]

Figure 9. EWEN/EWDS Timing

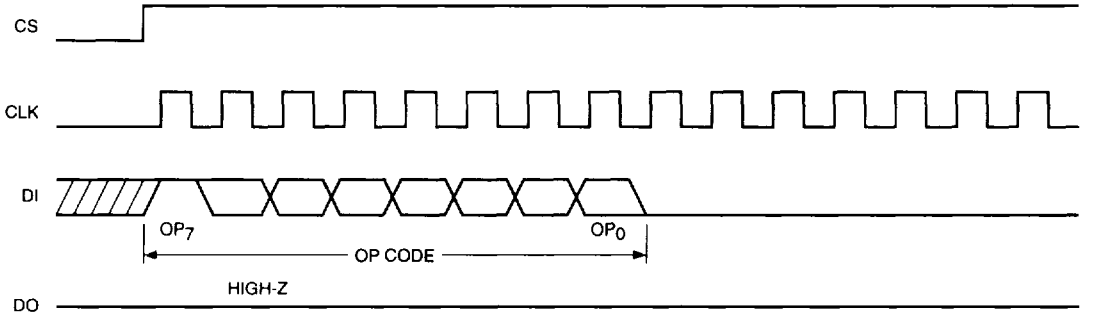

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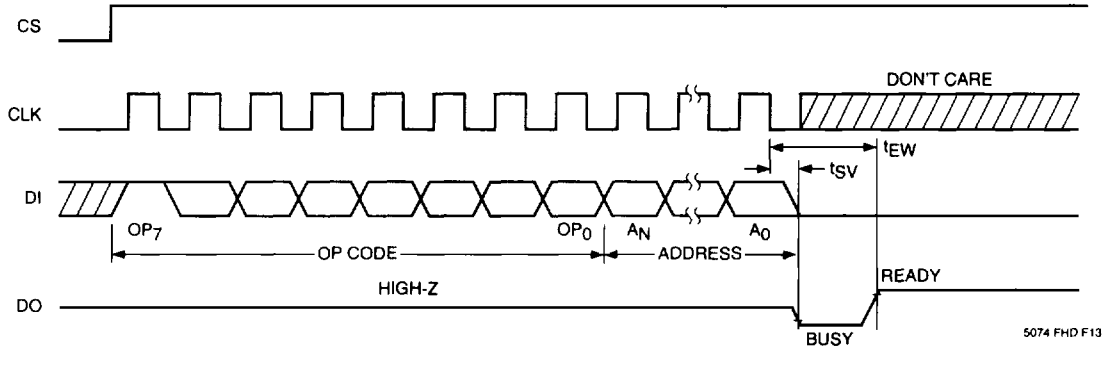
Figure 10. Erase Timing



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As shown previously in Figure 3, memory locations below the address set in the memory pointer will be program/erase protected. Thus, unintentional clearing or writing of data in this area will be prevented, while memory locations at or above the protected area still allow full access. This protection does not apply to the ERAL and WRAL commands which are not blocked by the memory pointer.

SECURE MODE

As shown previously in Figure 2, in the secure mode, memory locations at or above the address set in the memory pointer allow READ-only access. Memory locations below that address will require an access code before they can be accessed. The secure mode is activated with an MACC (Modify Access Code) instruction followed by a user access code which can be one to eight bytes in length.

EWEN
MACC [old code][new code][new code]

The EWEN instruction enables the device to perform program/erase operations. The new access code must be entered twice for verification. If the device already has an access code, the old access code must be entered before the new access code can be accepted. The length of the password is incorporated into the MACC portion of the instruction.

Once the secure mode is activated, access to memory locations is under software control. Access (read, write, and clear instructions) to the memory locations below the address in the memory pointer is allowed only if the ENAC (Enable Access) instruction followed by the correct access code has been previously executed.

ENAC [access code]
EWEN
WRITE [address][data]

The ENAC instruction, along with the access code, enables access to the protected area of the device. The EWEN instruction enables execution of the program/erase operations. This portion of the memory is otherwise inaccessible for any operation. Read-only access is allowed without the access code for memory locations at or above the address in the memory pointer.

The access code can be changed by the following instruction:

ENAC [old access code]
EWEN
MACC [old code][new code][new code]

A two-tier protection scheme is implemented to protect data against inadvertent clearing or writing. To write to the memory, an EWEN (Program/Erase Enable) must first be issued. The CAT35C704 will now allow program/erase operations to be performed only on memory locations at or above the address set in the memory pointer. The remaining portion of the memory is still protected. To override this protection, an OVMPR (Override Memory Pointer Register—see Memory Pointer Register) must be issued for every program/erase instruction which accesses the protected area:

ENAC [access code]
EWEN
OVMPR
WRITE [address][data]

As an alternative to the OVMPR instruction, the WMPR (Write Memory Pointer Register) instruction may be used to move the memory pointer address to uncover the area where writing is to be performed:

ENAC [access code]
EWEN
WMPR [address]
WRITE [address][data]

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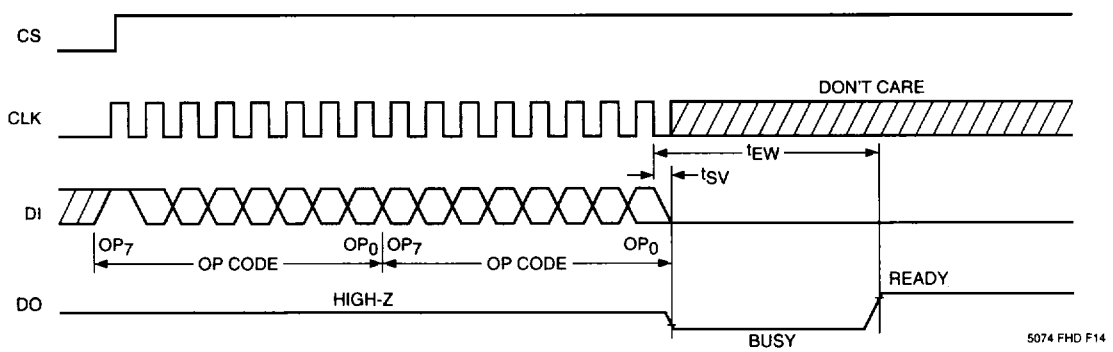
Figure 11. ERAL Timing



As shipped from the factory, the device is in the unprotected mode. The length of the access code is user selectable from a minimum of one byte to a maximum of eight bytes (> 1.84×10^{19} combinations). Loading a zero-length access code will disable protection.

MEMORY POINTER REGISTER

The memory pointer enables the user to segment the E^2PROM array into two sections. In the unprotected mode, the array can be segmented between read-only and full access, while in the secure mode, the memory may be segmented between read-only access and password-only access. Three instructions are dedicated to the memory pointer operations. The first one is WMPR (Write Memory Pointer Register). This instruction, followed by an address, will load the memory pointer register with a new address. This address will be stored in the E^2PROM and can be modified only by another WMPR instruction. The second instruction is OVMPR (Override Memory Pointer Register) which allows a single program/erase to be performed to memory locations below the address set in the memory pointer. This instruction allows the user to modify data in a segmented array without having to move the memory pointer. Once the operation is complete, the device returns to the protected mode. If the device is in the secure mode both of these instructions require the ENAC instruction and a valid access code prior to their execution. The third instruction is the RMPR (Read Memory Pointer Register) which will place the current contents of the register in the serial output buffer.

SECS PROTOCOL

The CAT35C704 implements the SECS communication protocol which uses an 8-bit transmission format. As shown in Figures 7–13, all instructions are 8 bits long with the first bit being the start bit and the following 7 bits being the op-code. Data can be one or two bytes long depending on the instruction and the memory array organization. Each address is one or two bytes long depending on the organization of the memory array. In this protocol, the transmission of the MSB is always first and the LSB last. The CS (Chip Select) pin of the CAT35C704 may be used to frame the data transmission packet or it may be set HIGH for the entire duration of operation. If an error in op-code or parity (if enabled) has been detected, the $\overline{ERR}$ output will be set LOW and the CAT35C704 will stop receiving and sending data until CS is toggled from HIGH to LOW to HIGH again. Alternatively, an error condition may be detected by interrogating the device for a status word. If an error condition has been detected, the DO (Data Output) pin will not respond. DO may be programmed to become tri-stated or to output a RDY/$\overline{BUSY}$ status flag during program/erase cycles (see ENBSY instruction).

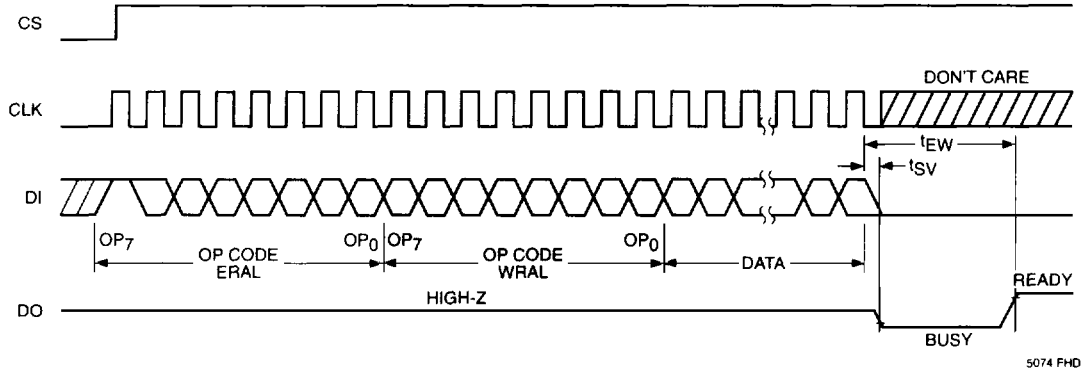
STATUS REGISTER

An eight bit status register is provided to allow the user to determine the status of the CAT35C704. The contents of the first three bits of the register are 101 which allows the user to quickly determine the condition of the device. The next three bits indicate the status of the device; they are parity error, instruction error and RDY/$\overline{BUSY}$ status. The last two bits are reserved for future use.

CLEAR ALL AND WRITE ALL

As a precaution, the ERAL instruction has to be entered twice before it is executed. This measure is required as a redundancy check on the incoming instruction for possible transmission errors. The WRAL instruction requires sending an ERAL first (this sets a flag only) and then the WRAL instruction. The CAT35C704 will accept

Figure 12. WRAL Timing



the following commands:

ERAL	**ERAL**	An ERAL will be executed
ERAL	**WRAL**	A WRAL will be executed

Both the ERAL and WRAL commands will program/erase the entire array and will not be blocked by the memory pointer.

THE PARITY BIT

The SECS protocol supports an even parity bit if the PE pin of the device is set HIGH, otherwise, there is no parity. If PE is set LOW and the incoming instruction contains a parity bit, it may be interpreted as the start bit of the next instruction. When PE is HIGH, the CAT35C704 expects a parity bit at the end of every incoming instruction packet. For example, the RSEQ instruction will look like this:

1100 1011
A15...A8
A7...A0 P

The device then outputs data continuously until it reaches the end of the memory. The last byte of data contains 9 bits. The ninth bit is the parity bit calculated over the entire transmitted data packet. The RSEQ instruction may be terminated at any time by bringing CS low; the output will then go to high impedance.

SYSTEM ERRORS

Whenever an error occurs, be it an instruction error (unknown instruction), or parity error (perhaps caused by transmission error), the device will stop its operation. To return to normal operation, the device must be reset by pulsing CS LOW and then set back to HIGH. Resetting the device will not affect the ENAC, EWEN and ENBSY status. The error may be determined by entering the READ STATUS REGISTER (RSR) instruction immediatly following the reset. The status output is an 8 bit word with the first three bits being 101. This three bit pattern indicates that the device is functioning normally. The fourth bit is "1" if a parity error occurred. The fifth bit is a "1" if an instruction error occurred. The sixth bit is a "1" if the device is in a program/erase cycle. The last two bits are reserved for future use.

The reason for the "101" pattern is to distinguish between an error conditon (DO tri-stated) and a device busy status. If an error condition exists, it will not respond to any input instruction from DI. However, if the device is in a program/erase cycle, it responds to the RSR instruction by outputting "101 00100". If RSR is executed at the end of a program/erase cycle, the output will be "101000 00".

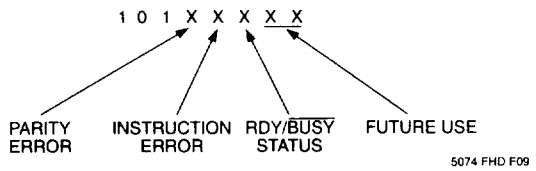


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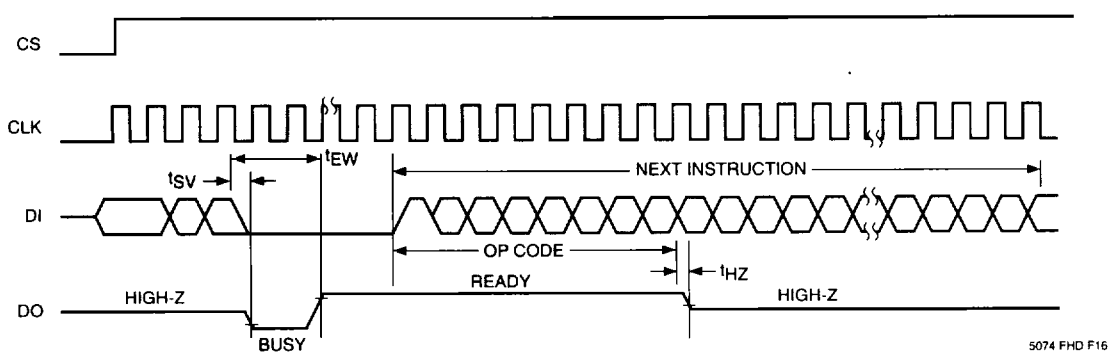
Figure 13. Next Instruction Timing(1)



Note:
(1) DO will be high impedance after the last instruction bit has been clocked in, unless the instruction is RSR or RMPR, in which case, DO will become active.

INSTRUCTION SET

DISAC Disable Access

1000	1000

This instruction will lock the memory from all program/erase operations regardless of the contents of the memory pointer. A write can be accomplished only by first entering the ENAC instruction followed by a valid access code.

ENAC Enable Access

1100	0101	[Access Code]

In the protected mode, this instruction, followed by a valid access code, unlocks the device for read/write/clear access.

WMPR Write Memory Pointer Register

1100	0100	[A15–A8] [A7–A0] *(x8 organization)*
1100	0100	[A7–A0] *(x16 organization)*

The WMPR instruction followed by 8 or 16 bits of address (depending on the organization) will move the pointer to the newly specified address.

MACC Modify Access Code

1101	[Length] [Old code] [New code] [New code]

This instruction requires the user to enter the old access code, if one was set previously, followed by the new access code and a re-entry of the new access code for verification. Within the instruction format, the variable [Length] designates the length of the access code as the following:

[Length] = [0] No access code. Set device to unprotected mode.

[Length] = [1–8] Length of access code is 1 to 8 bytes.

[Length] = [>8] Illegal number of bytes. The CAT35C704 will ignore the rest of the transmission.

RMPR Read Memory Pointer Register

1100	1010

Output the content of the memory pointer register to the serial output port.

OVMPR Override Memory Pointer Register

1000	0011

Override the memory protection for the next instruction.

READ Read Memory

1100	1001	[A15–A8] [A7–A0] *(x8 organization)*
1100	1001	[A7–A0] *(x16 organization)*

Output the contents of the addressed memory location to the serial port.

WRITE Write Memory

1100	0001	[A15–A8] [A7–A0] [D7–D0] *(x8 organization)*
1100	0001	[A7–A0] [D15–D8] [D7–D0] *(x16 organization)*

Write the 8 bit or 16 bit data to the addressed memory location. After the instruction, address, and data have been entered, the self-timed program/erase cycle will start. The addressed memory location will be erased before data is written. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENBSY instruction. During the program/erase cycle, DO will output a LOW for BUSY during this cycle and a HIGH for READY after the cycle has been completed.

ERASE Clear Memory

1100	0000	[A15–A8] [A7–A0] *(x8 organization)*
1100	0000	[A7–A0] *(x16 organization)*

Erase data in the specified memory location (set memory to "1"). After the instruction and the address have been entered, the self-timed clear cycle will start. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENSBY instruction. During the clear cycle, DO will output a LOW for BUSY during this cycle and a HIGH for ready after the cycle has been completed.

ERAL Clear All

1000	1001
1000	1001

Erase the data of all memory locations (all cells set to "1"). For protection against inadvertent chip clear, the ERAL instruction is required to be entered twice.

WRAL Write All

1000	1001	
1100	0011	[D15–D8] [D7–D0] *(x16 organization)*
1000	1001	
1100	0011	[D7–D0] *(x8 organization)*

Write one or two bytes of data to all memory locations. An ERAL will be automatically performed before the

WRAL is executed. For protection against inadvertent clearing or writing of data, the ERAL instruction is required to be entered preceding the WRAL instruction.

RSEQ Read Sequentially

1100	1011	[A15–A8] [A7–A0] *(x8 organization)*

1100	1011	[A7–A0] *(x16 organization)*

Read memory starting from specified address, sequentially to the highest address or until CS goes LOW. The instruction is terminated when CS goes LOW.

ENBSY Enable Busy

1000	0100

Enable the status indicator on DO during program/erase cycle. DO goes LOW then HIGH once the write cycle is complete. DO will go to HIGH-Z at the end of the next op code transmission.

DISBSY Disable Busy

1000	0101

Disable the status indicator on DO during program/erase cycle.

EWEN Program/Erase Enable

1000	0001

Enable program/erase to be performed on non-protected portion of memory. This instruction must be entered before any program/erase instruction will be carried out. Once entered, it will remain valid until power-down or an EWDS (Program/Erase Disable) is executed.

EWDS Program/Erase Disable

1000	0010

Disable all write and clear functions.

ORG Select Memory Organization

1000	011R	*(where R = 0 or 1)*

Set memory organization to 512 x 8 if R = 0.

Set memory organization to 256 x 16 if R = 1.

RSR Read Status Register

1100	1000

Output the contents of the 8-bit status register. The contents of the first three bits of the register are 101, which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate parity error, instruction error and RDY/$\overline{\text{BUSY}}$ status. The last two bits are reserved for future use.

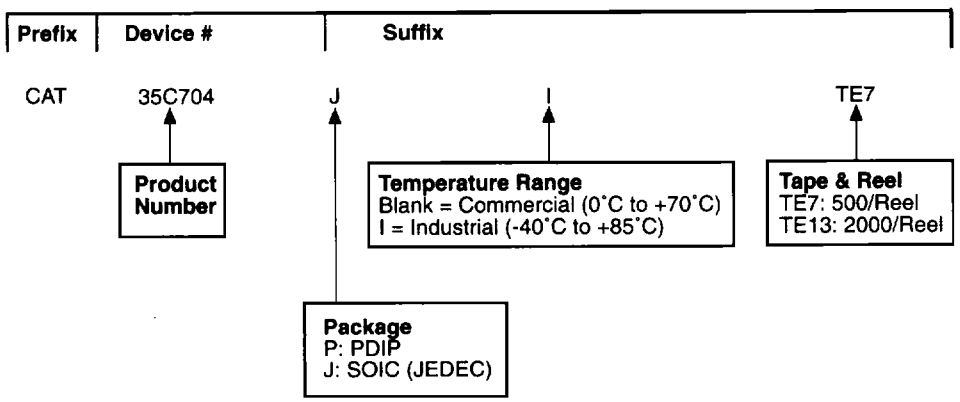
NOP No Operation

1000	0000

No Operation.

5

ORDERING INFORMATION



35C704 F17

Notes:
(1) The device used in the above example is a 35C704JI-TE7 (SOIC, Industrial Temperature, Tape & Reel)