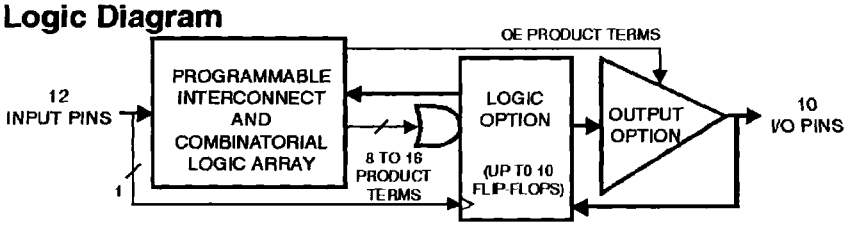
Features

- **Industry Standard Architecture**
  - **Low Cost Easy-to-Use Software Tools**
- **High Speed Electrically Erasable Programmable Logic Devices**
  - **7.5 ns Maximum Pin-to-Pin Delay**
- **Several Power Saving Options**

Device	Icc, Stand-By	Icc, Active
ATF22V10B	85 mA	90 mA
ATF22V10BQ	35 mA	40 mA
ATF22V10BL	5 mA	60 mA
ATF22V10BQL	5 mA	20 mA

- **CMOS and TTL Compatible Inputs and Outputs**
  - **Input and I/O Pull-Up Resistors**
- **Advanced Flash Technology**
  - **Reprogrammable**
  - **100% Tested**
- **High Reliability CMOS Process**
  - **20 Year Data Retention**
  - **100 Erase/Write Cycles**
  - **2,000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Full Military, Commercial, and Industrial Temperature Ranges**
- **Dual-in-Line and Surface Mount Packages in Standard Pinouts**

Logic Diagram

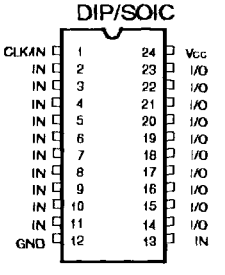


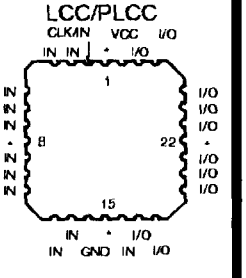
Description

The ATF22V10B is a high performance CMOS (Electrically Erasable) Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 7.5 ns and power dissipation as low as 10 mA are offered. All speed ranges are specified over the full 5 V ± 10% range for military and industrial temperature ranges, and 5 V ± 5% for commercial temperature ranges.

Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5 V Supply





High Performance Flash PLD

ATF22V10B

Description (Continued)

Several low power options allow selection of the best solution for various types of power-limited applications. Each of these options significantly reduces total system power and enhances system reliability.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc, which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75 V dc, which may overshoot to 7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Conditions

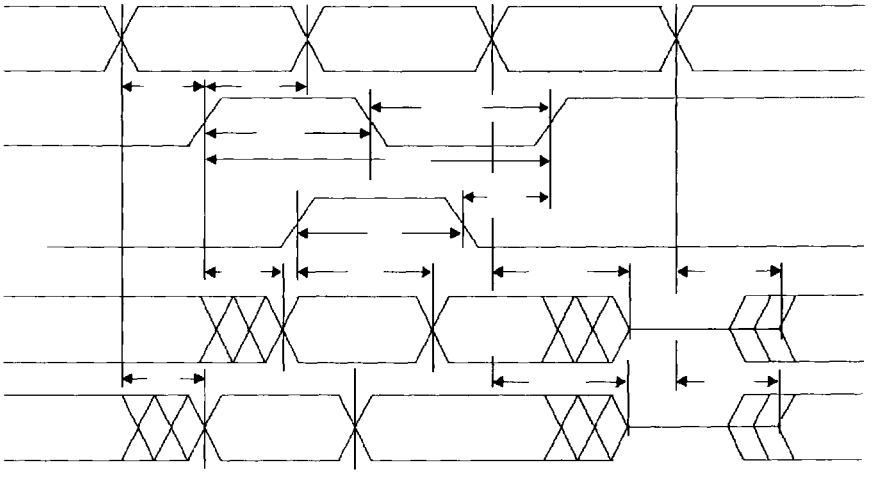
	Commercial	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}(MAX)$				-35	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = MAX, V_{IN} = MAX, Outputs Open	B-7, -10	Com.		85	120	mA
				Ind., Mil.		85	140	mA
			B-15, -25	Com.		85	120	mA
				Ind., Mil.		85	140	mA
			BQ-15	Com.		35	60	mA
			BL-15, BQL-25	Com.		5	10	mA
				Ind., Mil.		5	15	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open	BL-15, BQL-25	Com.		1		mA/MHz(2)
				Ind., Mil.		1		mA/MHz(2)
I_{CC3}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open, f = 15 MHz	B-7, -10	Com.		90	120	mA
				Ind., Mil.		90	140	mA
			B-15, -25	Com.		90	120	mA
				Ind., Mil.		90	140	mA
			BQ-15	Com.		40	55	mA
			BL-15	Com.		60	90	mA
				Ind., Mil.		60	130	mA
			BQL-25	Com.		20	50	mA
				Ind., Mil.		20	70	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-130	mA
V_{IL}	Input Low Voltage				-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		Vcc+0.75	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = MIN	I_{OL} = 16 mA	Com., Ind.			0.5	V
			I_{OL} = 12 mA	Mil.			0.5	V
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = MIN	I_{OH} = -4.0 mA		2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. Low frequency only. See Supply Current versus Input Frequency curves.

A.C. Waveforms [1]



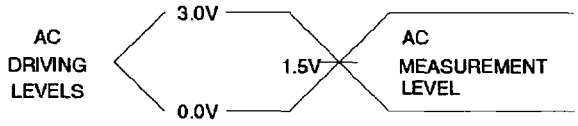
Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics [1]

Symbol	Parameter	-7		-10		-15		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output	3	7.5	3	10	3	15	3	25	ns
t_{CO}	Clock to Output	2	4.5 [2]	2	6.5	2	8	2	15	ns
t_{CF}	Clock to Feedback		3.5		4		4.5		13	ns
t_S	Input or Feedback Setup Time	3.5		4.5		10		15		ns
t_H	Hold Time	0		0		0		0		ns
F_{MAX}	External Feedback $1/(t_S + t_{CO})$	125 [3]		90		55.5		33.3		MHz
	Internal Feedback $1/(t_S + t_{CF})$	153		125		69		35.7		MHz
	No Feedback	166		166		83.3		38.5		MHz
t_P	Clock Period	6		8		12		26		ns
t_W	Clock Width	3		3		6		13		ns
t_{EA}	Input or I/O to Output Enable	3	7.5	3	10	3	15	3	25	ns
t_{ER}	Input or I/O to Output Disable	3	7.5	3	9	3	15	3	25	ns
t_{AP}	Input or I/O to Asynchronous Reset of Register	3	10	3	12	3	20	3	25	ns
t_{AW}	Asynchronous Reset Width	7		8		15		25		ns
t_{AR}	Asynchronous Reset Recovery Time	5		6		10		25		ns
t_{SP}	Setup Time, Synchronous Preset	4.5		6		10		15		ns
t_{SPR}	Synchronous Preset to Clock Recovery Time	5		8		10		15		ns

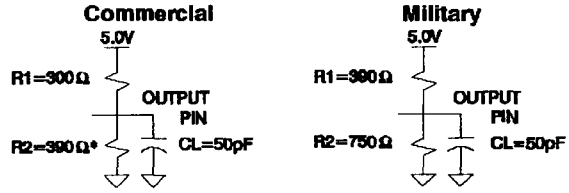
Note: 1. See ordering information for valid part numbers.
2. 5.5 nsec for DIP package devices.
3. 111 MHz for DIP package devices.

Input Test Waveforms and Measurement Levels



t_R, t_F < 3 nsec

Output Test Loads:



* All except -7 which is R2=300Ω

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

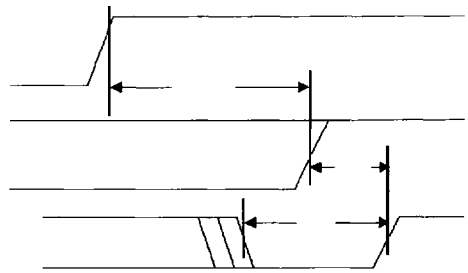
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The registers in the ATF22V10Bs are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
3. The clock must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-Up Reset Time	600	1,000	ns
V_{RST}	Power-Up Reset Voltage	3.8	4.5	V

Preload of Registered Outputs

The ATF22V10B's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF22V10B fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

Electronic Signature Word

There are 64-bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

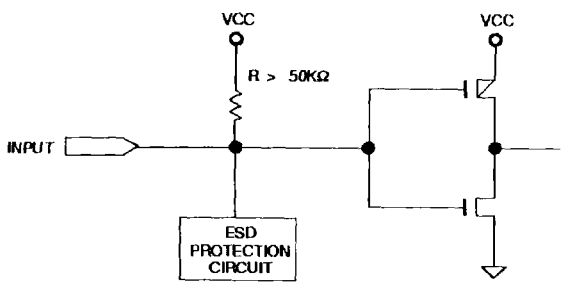
Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See *CMOS PLD Programming Hardware & Software Support* for information on software/programming.

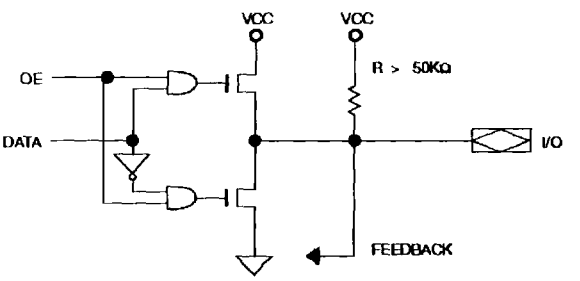
Input and I/O Pull-Ups

All ATF22V10B family members have internal input and I/O pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to Vcc. This ensures that all logic array inputs are at known states. These are relatively weak active pull-ups that can easily be overdriven by TTL-compatible drivers (see input and I/O diagrams below).

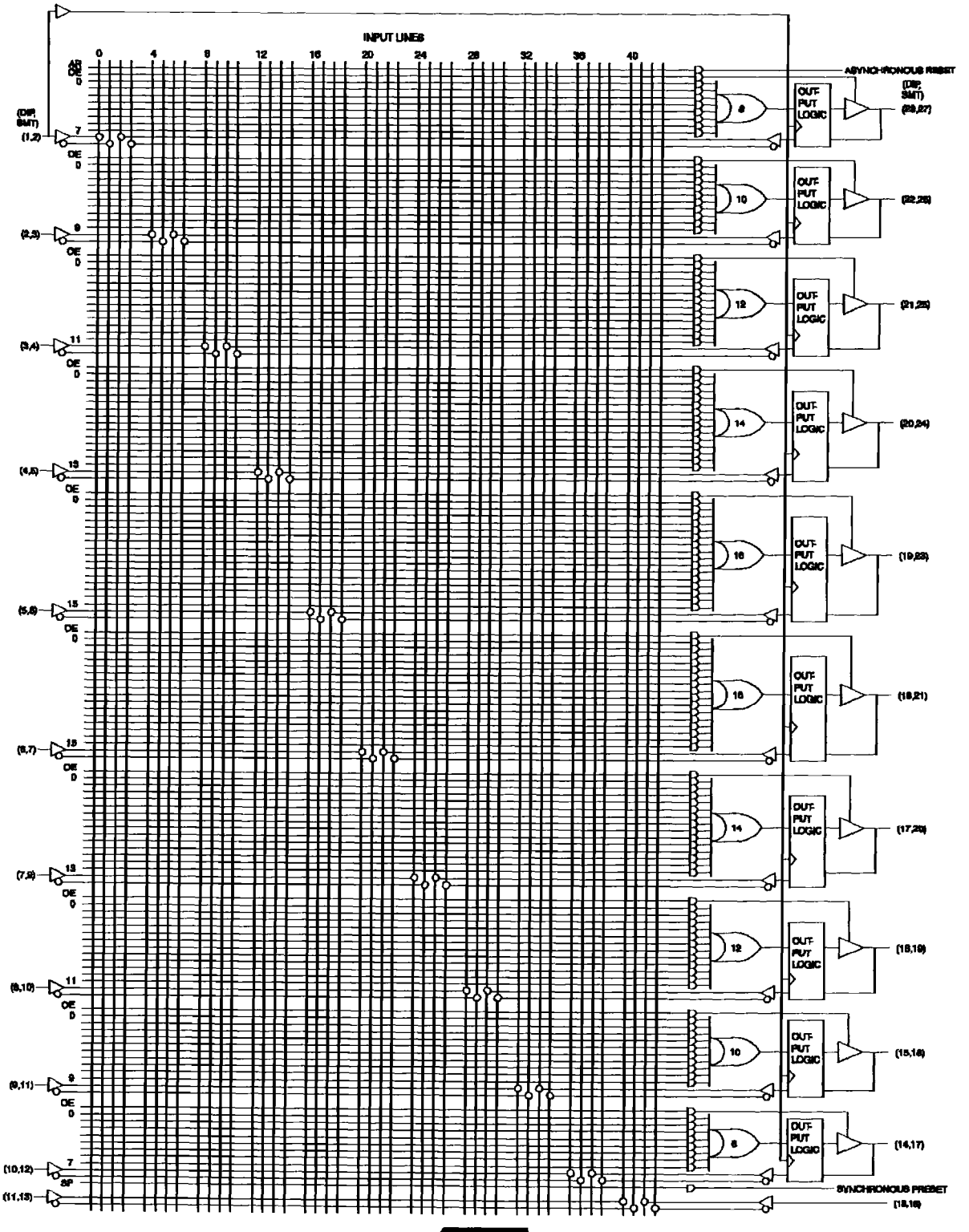
Input Diagram

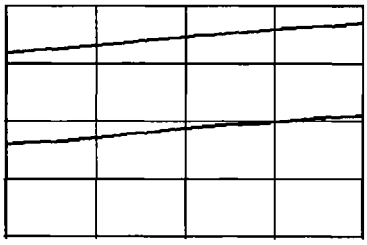


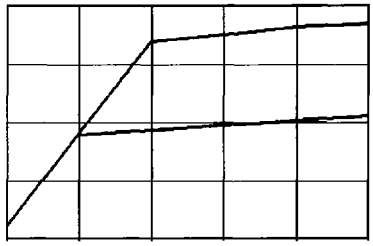
I/O Diagram

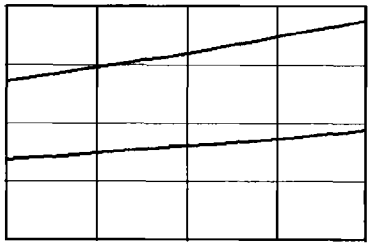


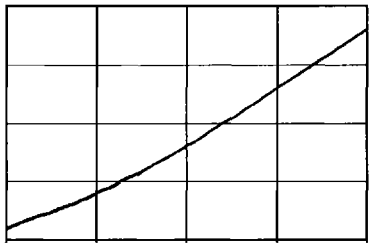
Functional Logic Diagram ATF22V10B

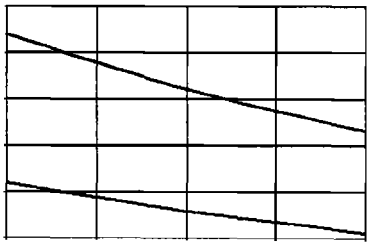


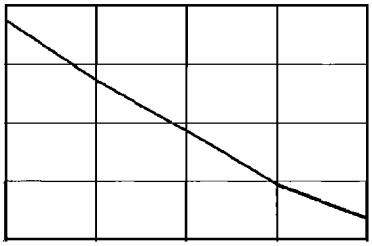


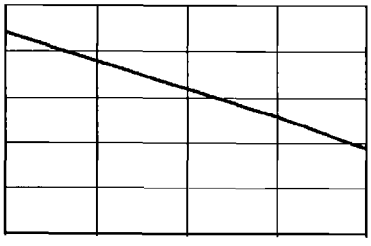


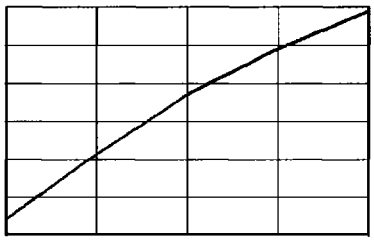




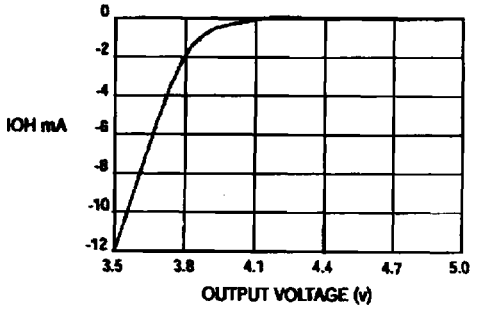




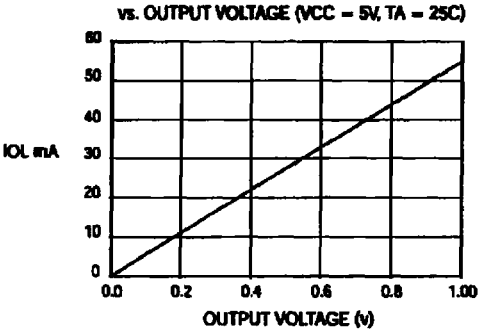




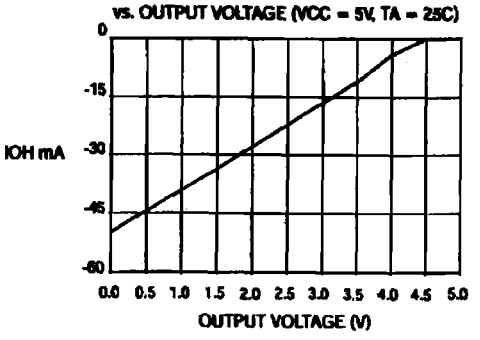
OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



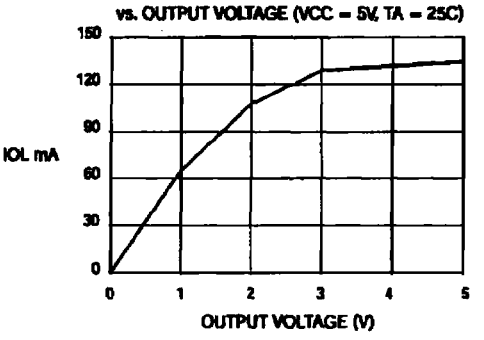
OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



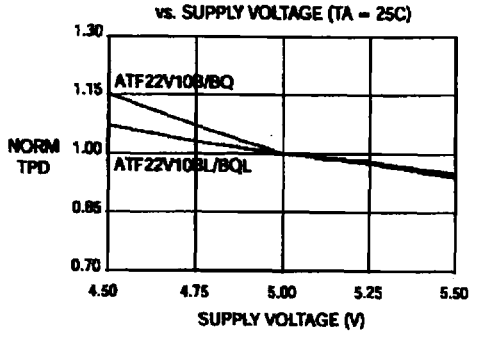
OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



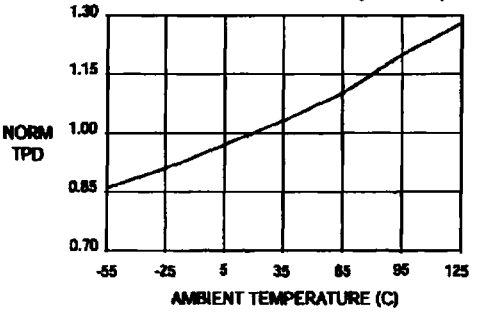
OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



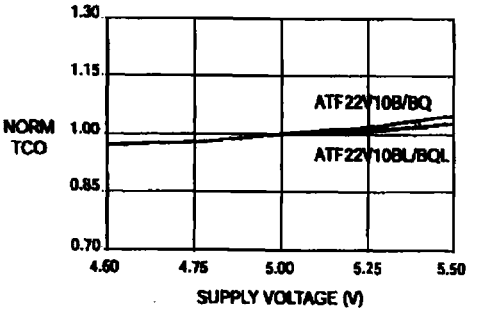
NORMALIZED TPD
vs. SUPPLY VOLTAGE (TA = 25C)



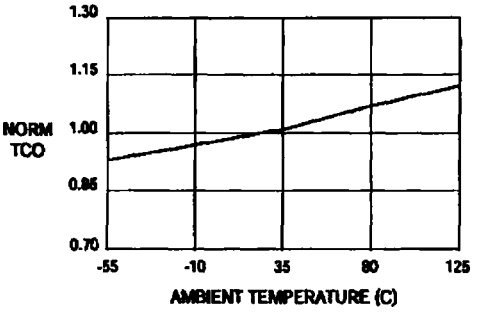
NORMALIZED TPD
vs. AMBIENT TEMPERATURE (VCC = 5V)



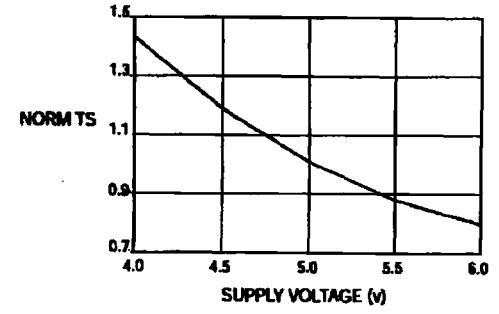
NORMALIZED TCO
vs. SUPPLY VOLTAGE (TA = 25C)



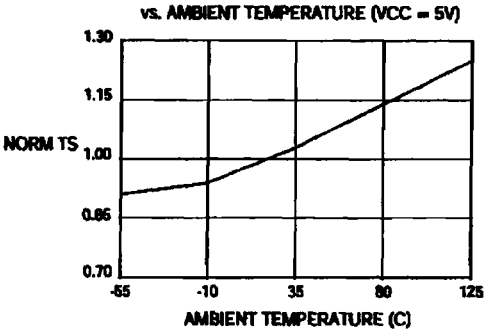
NORMALIZED TCO
vs. AMBIENT TEMPERATURE (VCC = 5V)



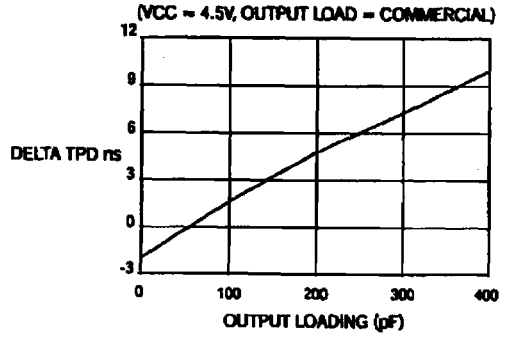
NORMALIZED TS
vs. SUPPLY VOLTAGE (TA = 25C)



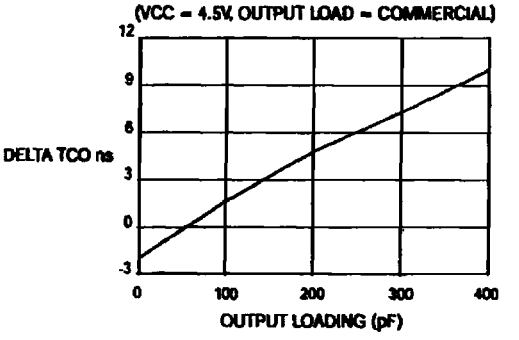
NORMALIZED TS
vs. AMBIENT TEMPERATURE (VCC = 5V)



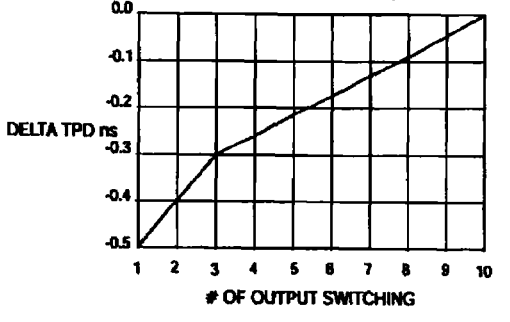
DELTA TPD vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



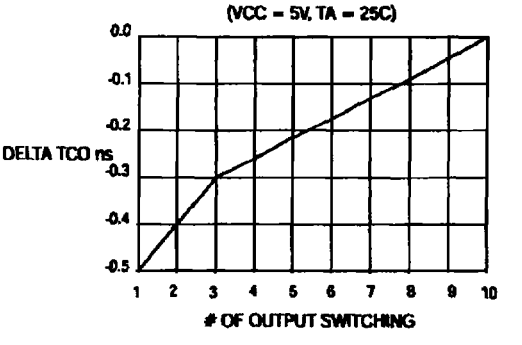
DELTA TCO vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



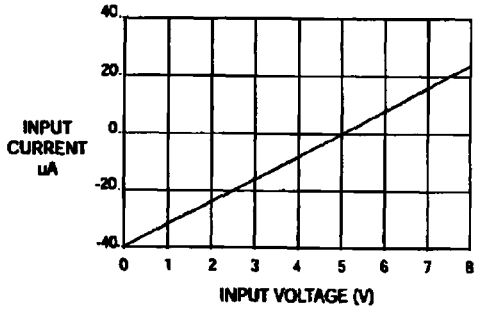
DELTA TPD vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)



DELTA TCO vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)



INPUT CURRENT vs. INPUT VOLTAGE
(VCC = 5V, TA = 25C)



INPUT CLAMP CURRENT
vs. INPUT VOLTAGE (VCC = 5V, TA = 25C)