

## Digital Attenuator 31.5 dB, 6-Bit, TTL Driver, DC-4.0 GHz

M/A-COM Products  
Rev. 12

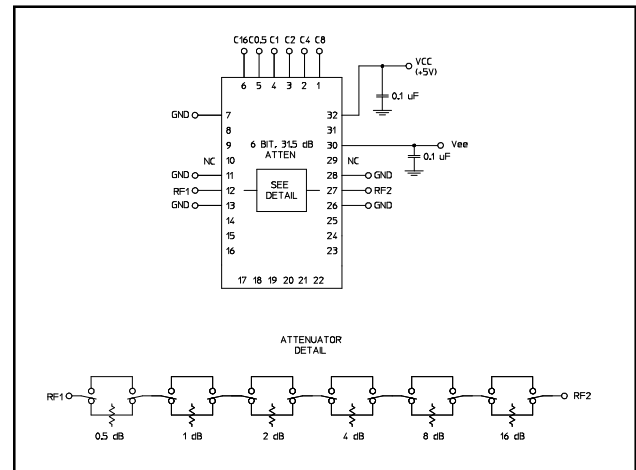
### Features

- Attenuation: 0.5 dB Steps to 31.5 dB
- Low DC Power Consumption
- Small Footprint, JEDEC Package
- Integral TTL Driver
- 50 ohm Impedance
- Test Boards are Available
- Tape and Reel Packaging Available
- CSP-1 Package

### Description

M/A-COM's AT90-0107 is a GaAs FET 6-bit digital attenuator with integral TTL driver. Step size is 0.5 dB providing a 31.5 dB total attenuation range. This device is in an PQFN plastic surface mount package. The AT90-0107 is ideally suited for use where accuracy, fast speed, very low power consumption and low costs are required.

### Schematic with Off-Chip Components



### Pin Configuration<sup>2</sup>

Pin No.	Function	Pin No.	Function
1	C8	17	NC
2	C4	18	NC
3	C2	19	NC
4	C1	20	NC
5	C0.5	21	NC
6	C16	22	NC
7	GND	23	NC
8	NC	24	NC
9	NC	25	NC
10	NC <sup>1</sup>	26	GND
11	GND	27	RF2
12	RF1	28	GND
13	GND	29	NC <sup>1</sup>
14	NC	30	-Vee
15	NC	31	NC
16	NC	32	+Vcc

1. Pins 10 & 29 must be isolated
2. The exposed pad centered on the package bottom must be connected to RF and DC ground. (For PQFN Packages)

### Ordering Information

Part Number	Package
AT90-0107	Bulk Packaging
AT90-0107TR	1000 piece reel
AT90-0107-TB	Sample Test Board

Note: Reference Application Note M513 for reel size information.

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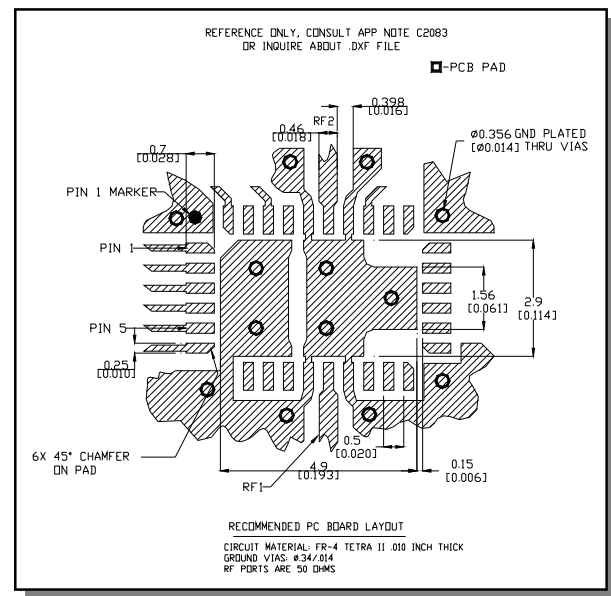
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**Electrical Specifications:  $T_A = +25^\circ\text{C}$ ,  $V_{EE} = -5\text{ V} \pm 0.25\text{ V}$ ,  $V_{CC} = +5\text{ V} \pm 0.25\text{ V}$** 

Parameter	Test Conditions	Frequency	Units	Min	Typ	Max
Insertion Loss	—	DC - 4.0 GHz	dB	—	4.5	5.1
Attenuation Accuracy	Individual Bits 0.5-1-2-4-8-16 dB Any Combination of Bits 1 to 31.5 dB	DC - 4.0 GHz DC - 4.0 GHz	dB dB	— —	— —	$\pm(.3 + 7\% \text{ of atten setting})$ $\pm(.5 + 8\% \text{ of atten setting})$
VSWR	Full Range	DC - 4.0 GHz	Ratio	—	2.0:1	2.2:1
Switching Speed	50% Cntl to 90%/10% RF 10% to 90% or 90% to 10%	— —	ns ns	— —	75 20	— —
1 dB Compression	— —	50 MHz 0.5 - 4.0 GHz	dBm dBm	— —	+21 +24	— —
Input $IP_3$	Two-tone inputs up to +5 dBm	50 MHz 0.5-4.0 GHz	dBm dBm	— —	+35 +48	— —
$V_{IL}$ $V_{IH}$	LOW-level input voltage HIGH-level input voltage	— —	V V	0.0 2.0	— —	0.8 5.0
$I_{in}$ (Input Leakage Current)	$V_{in} = V_{CC}$ or GND	—	uA	-1.0	—	1.0
$I_{CC}$ (Quiescent Supply Current)	$V_{cntrl} = V_{CC}$ or GND	—	uA	—	250	400
$\Delta I_{CC}$ (Additional Supply Current Per TTL Input Pin)	$V_{CC} = \text{Max}$ , $V_{cntrl} = V_{CC} - 2.1\text{ V}$	—	mA	—	—	1.0
$I_{EE}$	$V_{EE}$ min to max, $V_{in} = V_{IL}$ or $V_{IH}$	—	mA	-1.0	-0.2	—
Thermal Resistance $\theta_{jc}$	—	—	$^\circ\text{C/W}$	—	15	—

**Absolute Maximum Ratings** <sup>3,4</sup>

Parameter	Absolute Maximum
Max. Input Power 0.05 GHz 0.5 - 4.0 GHz	+27 dBm +34 dBm
$V_{CC}$	$-0.5\text{ V} \leq V_{CC} \leq +7.0\text{ V}$
$V_{EE}$	$-8.5\text{ V} \leq V_{EE} \leq +0.5\text{ V}$
$V_{CC} - V_{EE}$	$-0.5\text{ V} \leq V_{CC} - V_{EE} \leq 14.5\text{ V}$
$V_{in}^5$	$-0.5\text{ V} \leq V_{in} \leq V_{CC} + 0.5\text{ V}$
Operating Temperature	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Storage Temperature	$-65^\circ\text{C}$ to $+125^\circ\text{C}$

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

**Recommended PCB Configuration** <sup>6</sup>


- Application Note S2083 is available on line at [www.macom.com](http://www.macom.com)

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### Handling Procedures

Please observe the following precautions to avoid damage:

### Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

### Moisture Sensitivity

The MSL rating for this part is defined as Level 2 per IPC/JEDEC J-STD-020. Parts shall be stored and/or baked as required for MSL Level 2 parts.

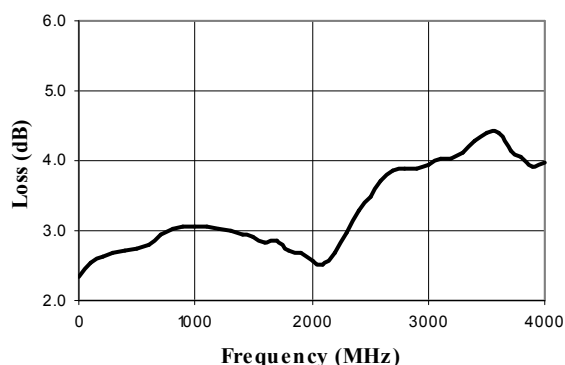
### Truth Table (Digital Attenuator)

C16	C8	C4	C2	C1	C0.5	Attenuation
0	0	0	0	0	0	Loss, Reference
0	0	0	0	0	1	0.5 dB
0	0	0	0	1	0	1.0 dB
0	0	0	1	0	0	2.0 dB
0	0	1	0	0	0	4.0 dB
0	1	0	0	0	0	8.0 dB
1	0	0	0	0	0	16.0 dB
1	1	1	1	1	1	31.5 dB

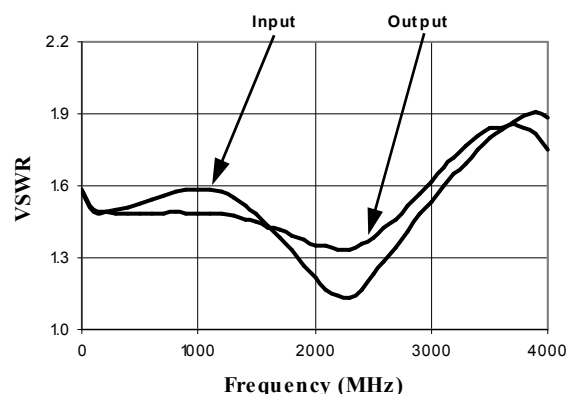
0 = TTL Low; 1 = TTL High

### Typical Performance Curves

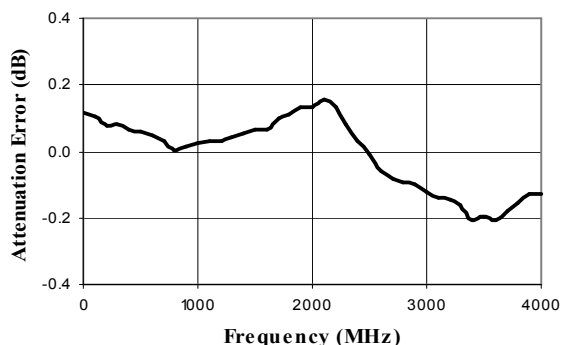
#### Insertion Loss



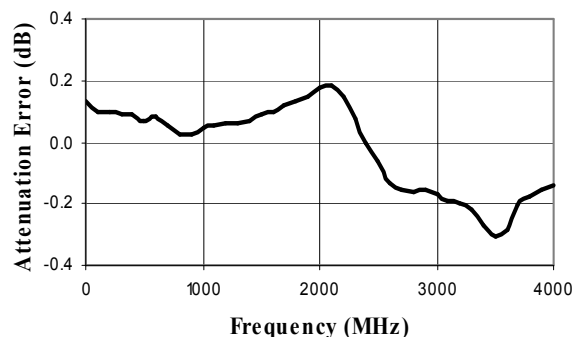
#### VSWR @ Insertion Loss



#### Attenuation Error, 0.5 dB Bit



#### Attenuation Error, 1 dB Bit

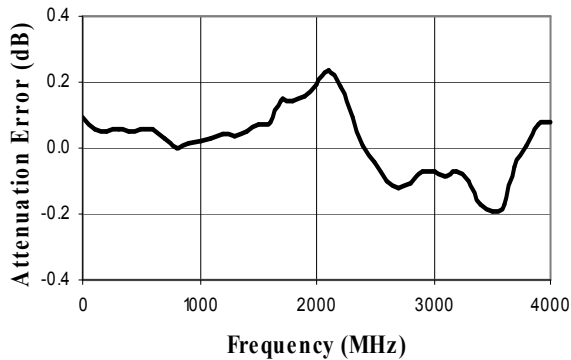


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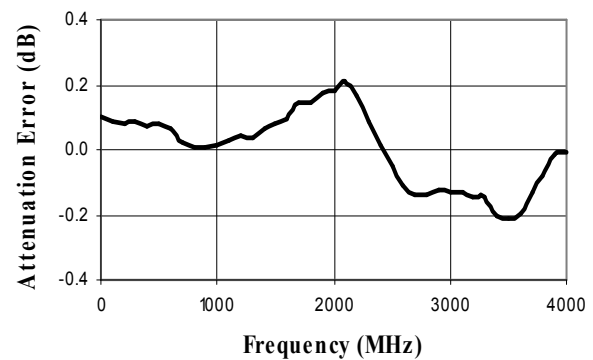
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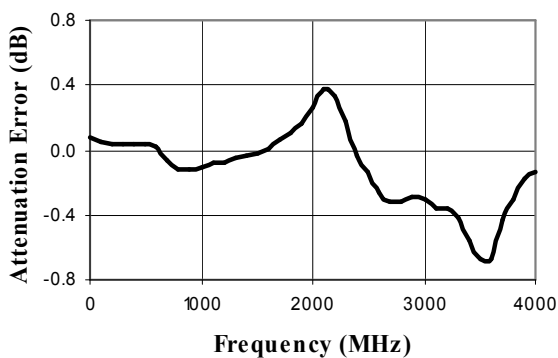
*Attenuation Error, 2 dB Bit*



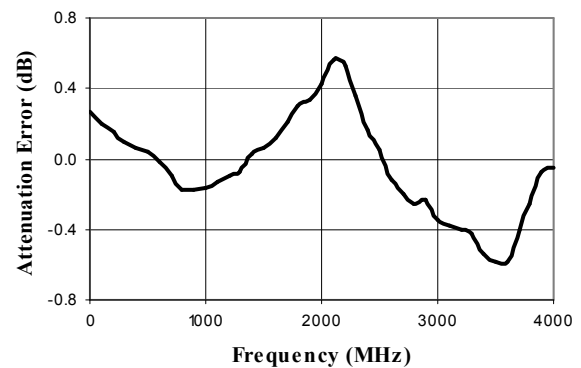
*Attenuation Error, 4 dB Bit*



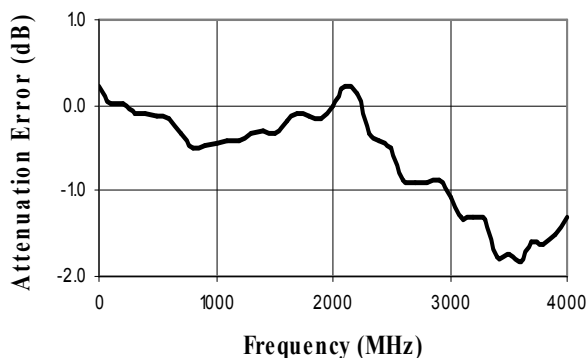
*Attenuation Error, 8 dB Bit*



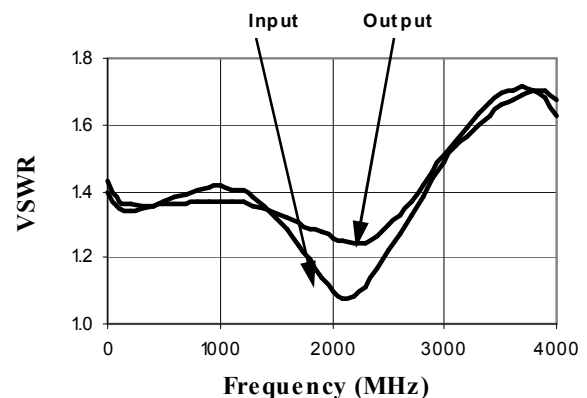
*Attenuation Error, 16 dB Bit*



*Attenuation Error, Max. Attenuation*



*VSWR, 0.5 dB Bit*

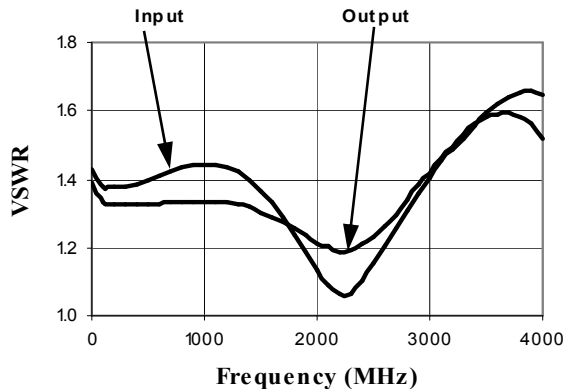


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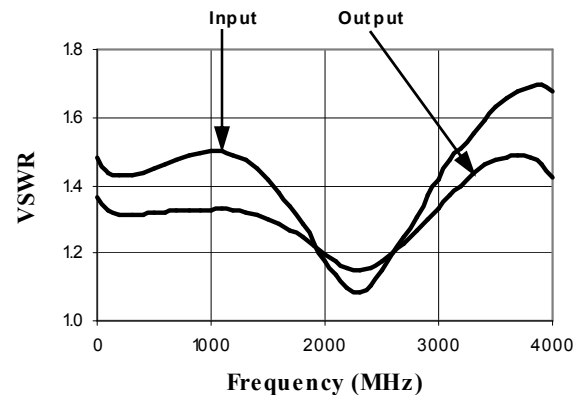
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## Typical Performance Curves

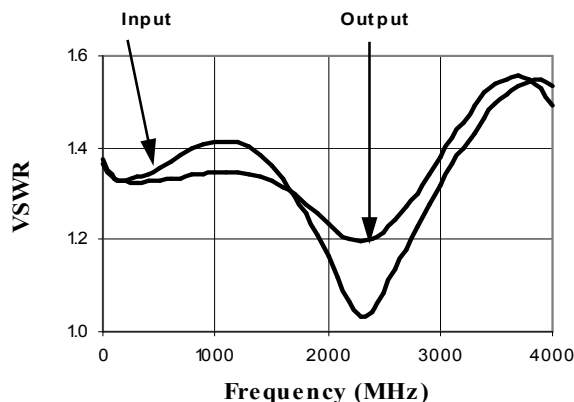
**VSWR, 1 dB Bit**



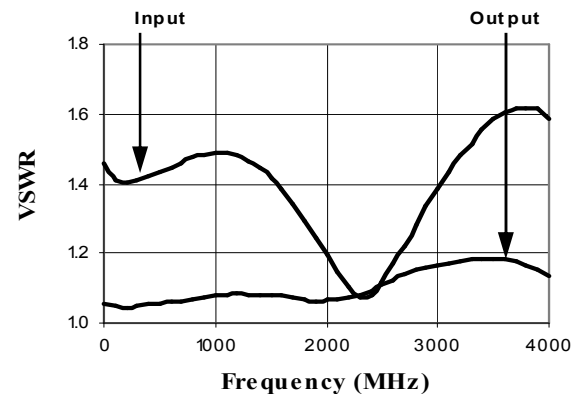
**VSWR, 2 dB Bit**



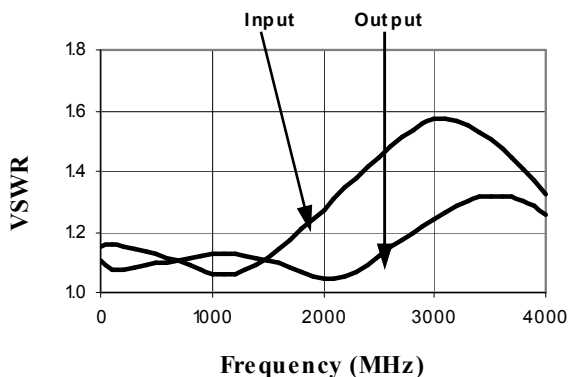
**VSWR, 4 dB Bit**



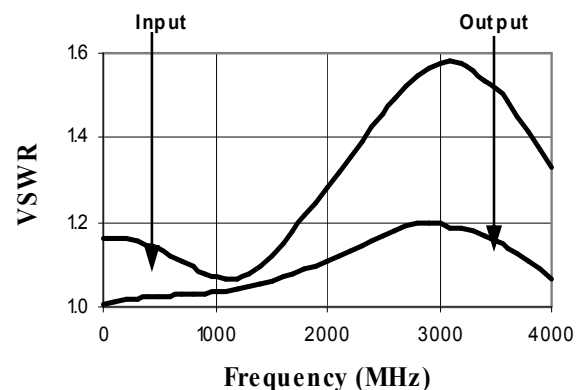
**VSWR, 8 dB Bit**



**VSWR, 16 dB Bit**



**VSWR, Max. Attenuation**

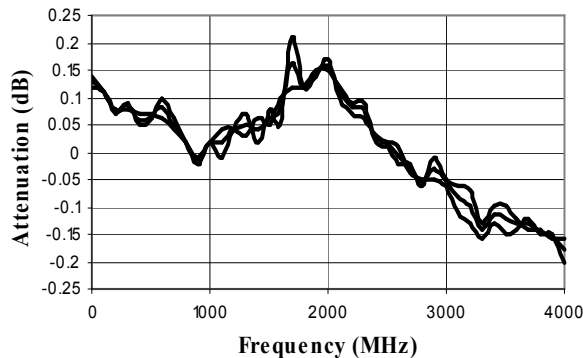


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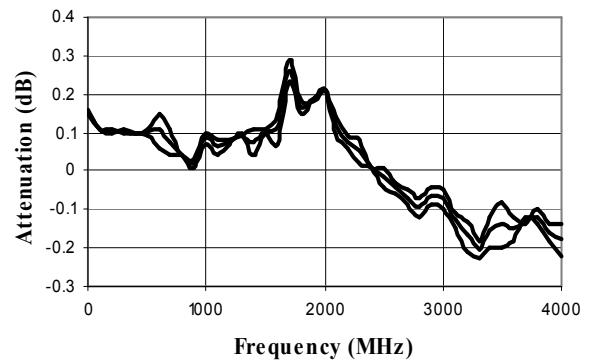
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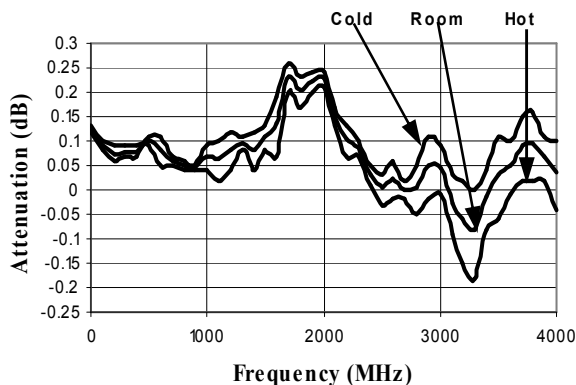
**Typical Attenuation Deviation vs. Temperature for 0.5 dB Bit**



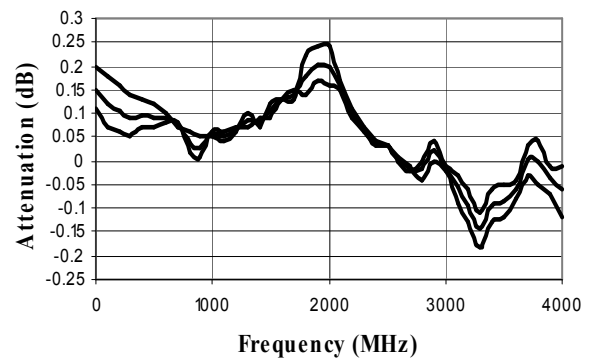
**Typical Attenuation Deviation vs. Temperature for 1 dB Bit**



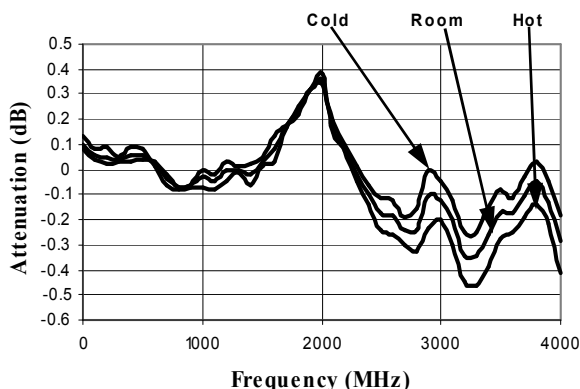
**Typical Attenuation Deviation vs. Temperature for 2 dB Bit**



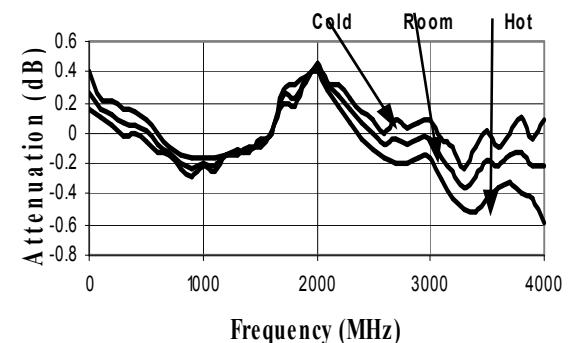
**Typical Attenuation Deviation vs. Temperature for 4 dB Bit**



**Typical Attenuation Deviation vs. Temperature for 8 dB Bit**



**Typical Attenuation Deviation vs. Temperature for 16 dB Bit**

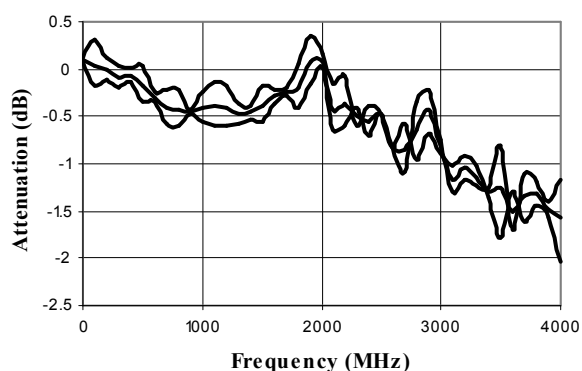


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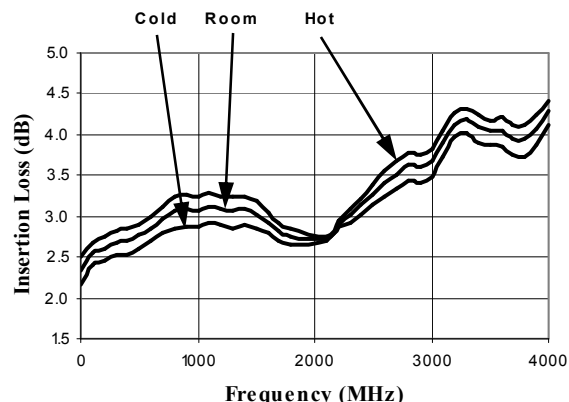
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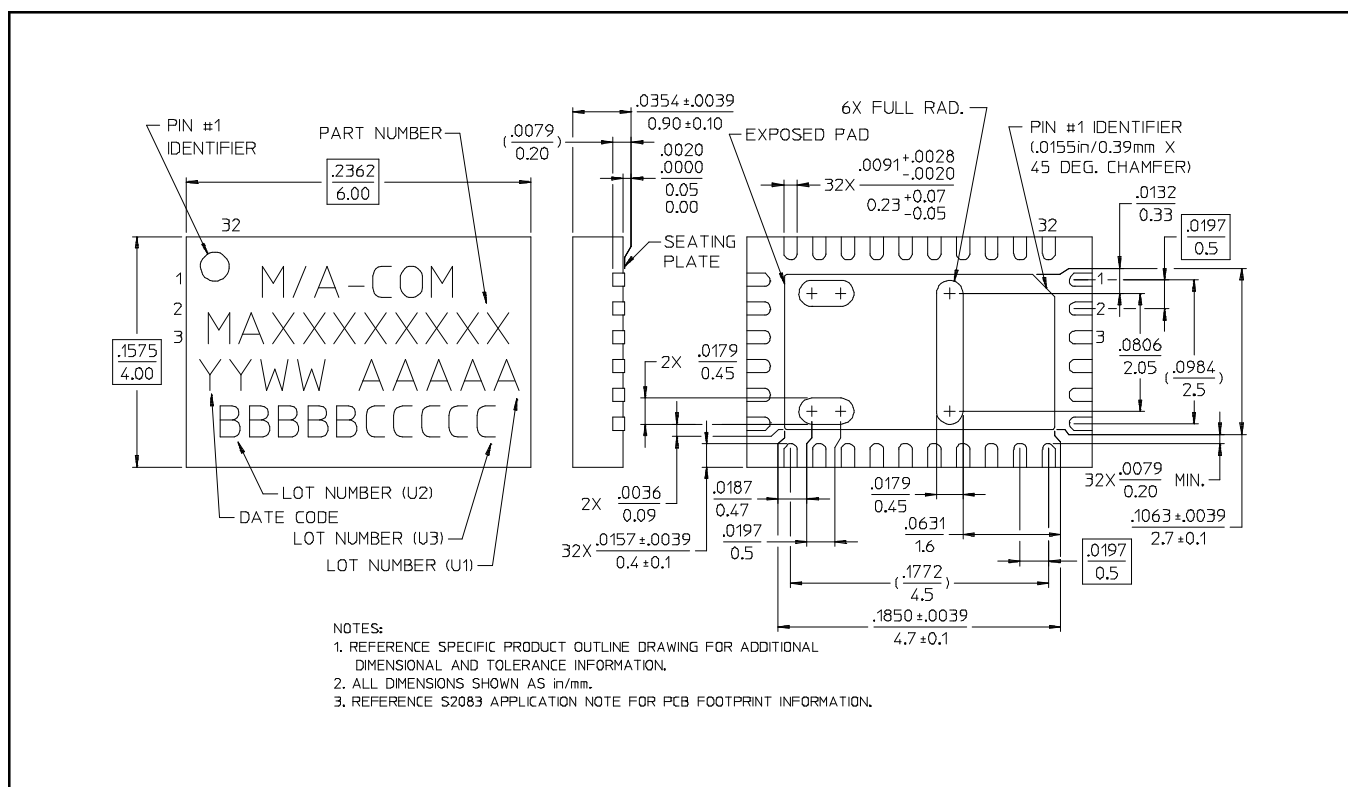
**Typical Attenuation Deviation vs. Temperature at Maximum Atten.**



**Insertion Loss vs. Temperature**



### CSP-1, 4 x 6 mm, 32-lead PQFN<sup>†</sup>



<sup>†</sup> Reference Application Note M538 for lead-free solder reflow recommendations.

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