Features

- Power Supply Control
  - Power Supply Control: Power-on Factor (2 External Signals and 2 Internal Signals)
  - Battery Voltage Detection
  - Reset Detection
  - Thermal Protection
  - SMPL (Sudden Momentary Power Loss) Function
- Power Supply Function
  - Step-down DC/DC Converter × 1 (One-shot PWM)
  - LDO × 9 (ECO-mode for LDO1 and 3)
  - Over-current Protection (All Linear Regulators)
- Li-ion Battery Charger
  - CC/CV Charge
  - Internal P-MOS, Current Sense Resistor and Schottky Diode
  - Charge Current Control by Chip Temperature
- White LED Driver and Charge Pump
  - White LED Driver for Backlight: Up to 25 mA/LED x 4
  - White LED Driver Charge Pump: Up to 100 mA
- RTC
  - Built-In Coin Charge Regulator
  - 32 kHz Crystal Oscillator (with Time Adjustment Function)
  - 32 kHz Output
- Audio CODEC
  - Voice CODEC: 16-bit Linear CODEC
  - Audio DAC: 16-bit Linear Stereo DAC
  - Tone Generator: Supports 16 DTMF Tones
  - Mono MIC Amplifier: Differential Amplifier
  - Stereo Headphone Amplifier: 22 mW (32 Ohm Load)
  - Mono Receiver Amplifier: 60 mW (32 Ohm BTL Load)
  - Mono Speaker Amplifier: 300 mW (8 Ohm BTL Load)
  - Microphone Bias Supply: Output Voltage = 2.2V
- PLL
  - Jack Detect Input 200 kOhm Pull-up
- CPU Interface
  - SPI (Max 10 MHz)
- Others
  - GPIO 4ch2ch: Common Use with ADC Input
  - 8-bit ADC (Battery Monitor, Charge Current Monitor, 2 Channels of External Input)
- Package
  - 96-pin CSP Package (Body size: 9 x 9 x 1mm, Pin pitch 0.8mm)
- Process
  - CMOS Process

Power Management And Analog Companions (PMAAC)

AT73C206 Power Management IC and Audio Codec

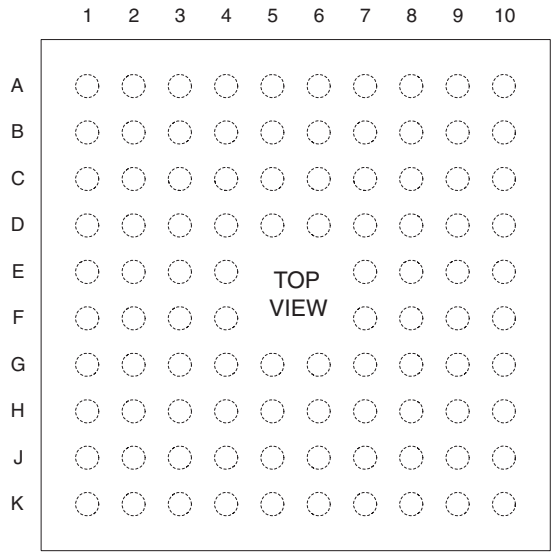
6329A–PMAAC–12-Aug-07

1. Description

The AT73C206 is the integrated analog device for VoIP and Cellular phones. It integrates a power management IC, which includes LDO, DC/DC converter, Li-ion battery charger, White LED driver, Charge Pump, RTC and GPIO, as well as Audio CODEC in one chip.

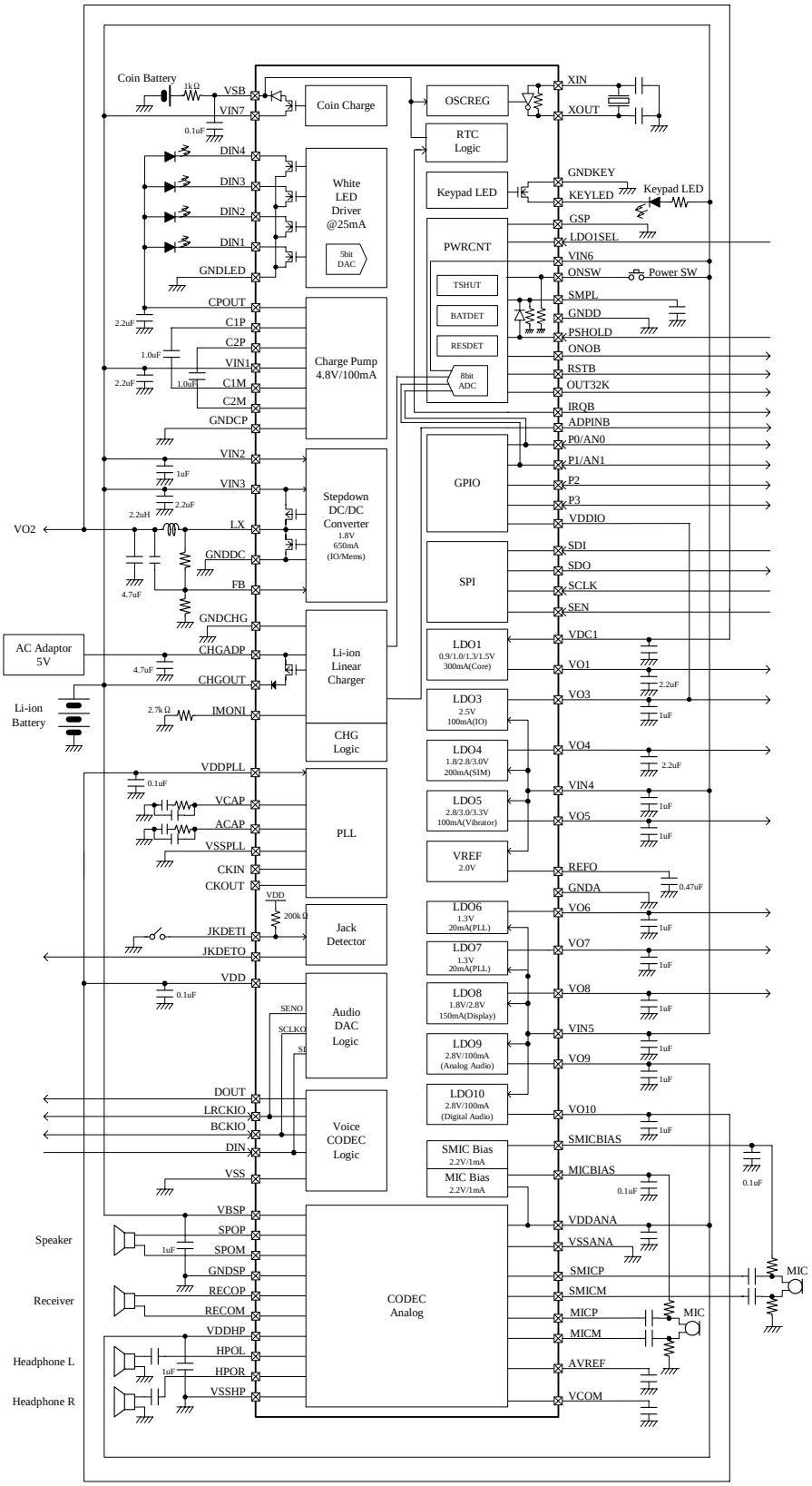
2. Pin Configuration

Figure 2-1. Pin Configuration



	1	2	3	4	5	6	7	8	9	10
A	XIN	XOUT	KEYLED	ONSW	PSHOLD	IRQB	P2	VDDIO	VO1	VO3
B	VIN7	VSB	GNDKEY	VIN6	ONOB	ADPINB	P3	SEN	VDC1	VO4
C	DIN3	DIN4	GNDLED	SMPL	RSTB	P0	SDI	SCLK	VIN4	VO5
D	DIN1	DIN2	CPOUT	GNDD	OUT32K	P1	SDO	GNDA	REFO	VO6
E	C1P	C2P	VIN1	LDO1SEL	TOP VIEW		SMIC BIAS	VIN5	VO7	VO8
F	C1M	C2M	GNDCP	GSP			SMICP	SMICM	MICBIAS	VO9
G	VIN3	VIN2	FB	JKDETI	LRCKIO	VSS	MICP	MICM	VDDANA	VO10
H	LX	GNDDC	GNDCHG	CKOUT	DOUT	DIN	SPOM	RECOP	VDDHP	VSSANA
J	CHGOUT	IMONI	VCAP	CKIN	JKDETO	BCKIO	SPOP	RECOM	VSSHP	AVREF
K	CHGADP	VSSPLL	ACAP	VDDPLL	VDD	VBSP	GNDSP	HPOL	HPOR	VCOM

3. Typical Application Circuit



4. Pin Description

Table 4-1. Pin Description

No.	Block	Pin	Name	I/O	If Level	Description	Notes
1	RTC	B2	VSB	O		Power input of coin charge regulator output and RTC	
2		B1	VIN7	VCC	VBAT	Power supply for RTCREG	
3	White LED Driver	C2	DIN4	O		Backlight White LED driver output 4	
4		C1	DIN3	O		Backlight White LED driver output 3	
5		C3	GNDLED	GND	GND	GND for Backlight White LED driver	
6		D2	DIN2	O		Backlight White LED driver output 2	
7		D1	DIN1	O		Backlight White LED driver output 1	
8	CHG Pump	D3	CPOUT	O		Charge Pump output for White LED driver	
9		E2	C2P	O		Voltage-boost capacitor connection pin for Charge Pump	
10		E1	C1P	O		Voltage-boost capacitor connection pin for Charge Pump	
11		E3	VIN1	VCC	VBAT	Power supply for Charge Pump	
12		F1	C1M	O		Voltage-boost capacitor connection pin for Charge Pump	
13		F2	C2M	O		Voltage-boost capacitor connection pin for Charge Pump	
14		F3	GNDCP	GND	GND	GND for Charge Pump	
15	DC/DC	G3	FB	I		Output voltage feedback input of DC/DC converter	
16		G2	VIN2	VCC	VBAT	Power supply for DC/DC converter control block	
17		G1	VIN3	VCC	VBAT	Power supply for DC/DC converter driver	
18		H1	LX	O	VBAT	DC/DC converter switch output	
19		H2	GNDDC	GND	GND	GND for DC/DC converter	
20	Charger	H3	GNDCHG	GND	GND	GND for charger block Filter connection pin for	
21		J2	IMONI	O		Battery charge current monitor	
22		J1	CHGOUT	O	VBAT	Li-ion battery charger output	
23		K1	CHGADP	VCC	ACADP	Charger block power (AC adaptor connected)	
24	PLL	K2	VSSPLL	GND	GND	PLL for GND	
25		J3	VCAP	O		Filter connection pin for Voice PLL	
26		K3	ACAP	O		Filter connection pin for Audio PLL	
27		K4	VDDPLL	VCC	VO10	PLL power	
28		J4	CKIN	I		Clock input	
29		H4	CKOUT	O		Clock output	
30	Jackdet	G4	JKDETI	I		JACKDET input	
31		J5	JKDETO	O		JACKDET output	

No	Block	Pin	Name	I/O	If Level	Description	Notes
32	Audio /Voice	K5	VDD	VCC	VO10	Power supply for CODEC digital block	
33		H5	DOUT	O	VDD	Voice CODEC output	
34		G5	LRCKIO	I/O	VDD	Audio / Voice interface L/R select input / output	
35		J6	BCKIO	I/O	VDD	Audio / Voice interface serial clock input / output	
36		H6	DIN	I	VDD	Audio and Voice interface serial data input	
37		G6	VSS	GND	GND	GND for CODEC digital block	
38		K6	VBSP	VCC	VBAT	Power supply for speaker AMP	
39		J7	SPOP	O		Speaker AMP output +	
40		H7	SPOM	O		Speaker AMP output -	
41		K7	GNDSP	GND	GND	GND for speaker AMP output	
42		H8	RECOP	O		Receiver AMP output +	
43		J8	RECOM	O		Receiver AMP output -	
44		H9	VDDHP	VCC	VO9	Power supply for headphone AMP output	
45		K8	HPOL	O		Headphone output L	
46		K9	HPOR	O		Headphone output R	
47		J9	VSSHP	GND	GND	GND for headphone AMP	
48		K10	VCOM	O		Reference voltage	Don't load this pin
49		J10	AVREF	O		Reference voltage	Don't load this pin
50		G7	MICP	I		MIC input +	
51		G8	MICM	I		MIC input -	
52		H10	VSSANA	GND	GND	GND for analog CODEC	
53		G9	VDDANA	VCC	VO9	Power for analog CODEC	
54		F7	SMICP	I		SMIC input +	
55		F8	SMICM	I		SMIC input -	
56		F9	MICBIAS	O		MIC Bias output	
57		E7	SMICBIAS	O		SMIC Bias output	
58	LDO	G10	VO10	O		LDO10 output	
59		F10	VO9	O		LDO9 output	
60		E8	VIN5	VCC	VBAT	Power supply for LDO6, 7, 8, 9, 10	
61		E10	VO8	O		LDO8 output	
62		E9	VO7	O		LDO7 output	
63		D10	VO6	O		LDO6 output	
64		D8	GNDA	GND	GND	GND for analog circuit	
65		D9	REFO	O		Capacitor connection pin for reference voltage source	Don't load this pin

No	Block	Pin	Name	I/o	If Level	Description	Notes
66	LDO	C10	VO5	O		LDO5 output	
67		C9	VIN4	VCC	VBAT	Power supply for LDO3, 4, 5 and VREF	
68		B10	VO4	O		LDO4 output	
69		A10	VO3	O		LDO3 output	
70		A9	VO1	O		LDO1 output	
71		B9	VDC1	VCC	VO2	Power supply for LDO1(DC/DC Output)	
72	SPI	B8	SEN	I	VDDIO	SPI enable input signal	
73		C8	SCLK	I	VDDIO	SPI clock input	
74		D7	SDO	O	VDDIO	SPI data output	
75		C7	SDI	O	VDDIO	SPI data input	
76		A8	VDDIO	VCC	VO3	Power supply for I/O	
77	GPIO	B7	P3	I/O	VDDIO	General purpose I/O port 3	
78		A7	P2	I/O	VDDIO	General purpose I/O port 2	
79		D6	P1/AN1	I/O	VDDIO	General purpose I/O port 1/ADC input 1	
80		C6	P0/AN0	I/O	VDDIO	General purpose I/O port 0/ADC input 0	
81	Power Control	B6	ADPINB	O	VDDIO	AC adaptor insertion detection output	
82		A6	IRQB	O	VDDIO	Interrupt request output	
83		D5	OUT32K	O	VDDIO	32 kHz oscillation output	
84		C5	RSTB	O	VDDIO	Reset output (Low-active)	
85		B5	ONOB	O	VDDIO	Inverted output signal of ONSW.	
86		A5	PSHOLD	I	VDDIO	Signal input pin to maintain power-on.	
87		D4	GNDD	GND	GND	GND for digital circuit	
88		C4	SMPL	I	VBAT	SMPL enable signal input	Pull-down
89		A4	ONSW	I	VBAT	Power-on switch enable signal input	Pull-down
90		B4	VIN6	VCC	VBAT	Power supply for VBAT detector and other circuits	
91		E4	LDO1SEL	I	VBAT	LDO1 initial value select input pin(1.5V or 1.3V)	
92		F4	GSP	I	VBAT	Initial state select input pin	
93	Keypad LED	A3	KEYLED	O		Keypad LED output (Nch open-drain)	
94		B3	GNDKEY	GND	GND	GND for Keypad LED driver	
95	RTC	A2	XOUT	O		32.768kHz crystal oscillator output	
96		A1	XIN	I		32.768kHz crystal oscillator Input	

5. Functional Blocks

5.1 Power Control & Reset

5.1.1 Power Control & Reset Block Diagram

Figure 5-1. Power Control & Reset Block Diagram

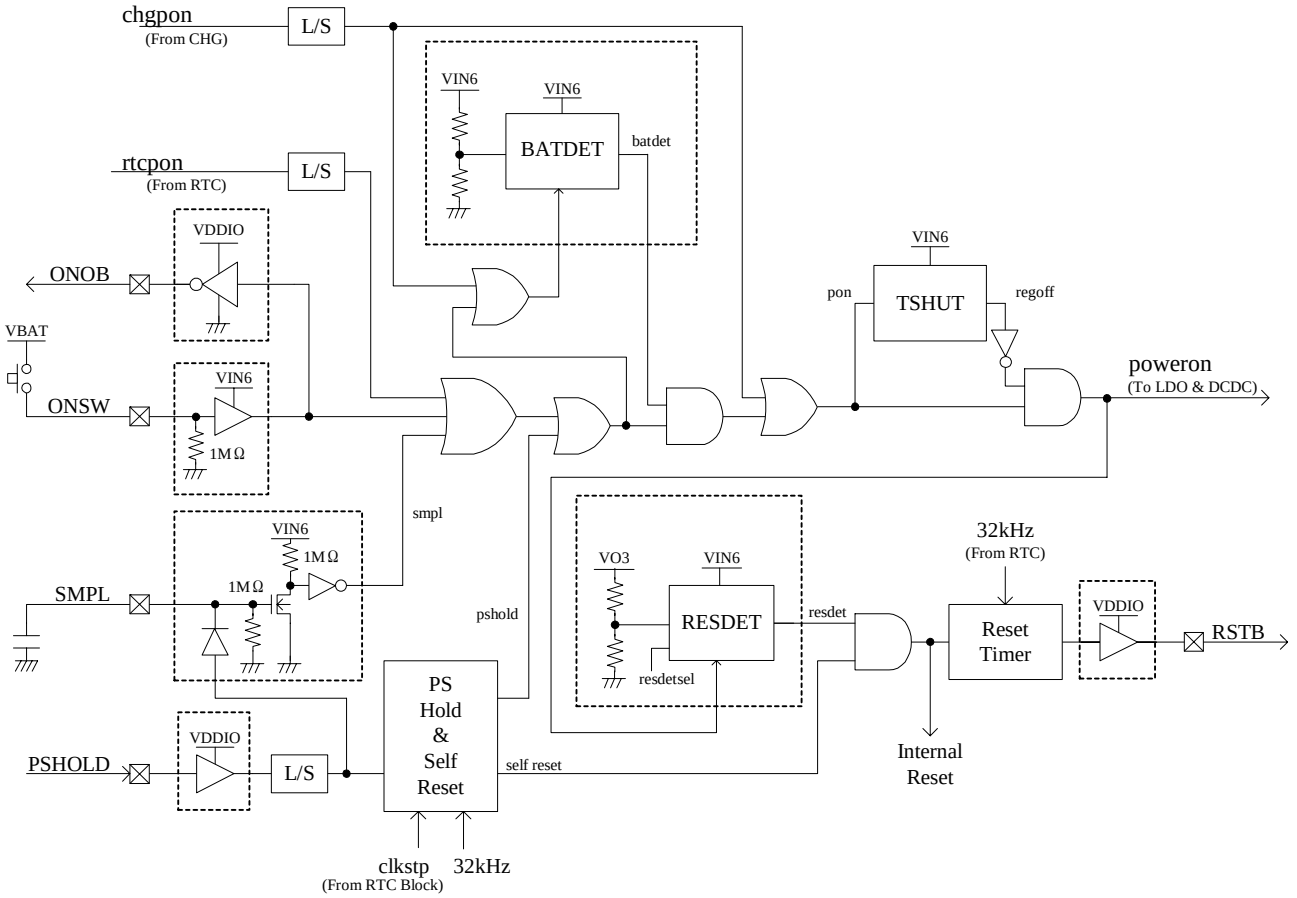


Table 5-1. Pin/Signal Description

Pin/signal Name	Function	Level
ONSW	Power-on signal input pin	VBAT
ONOB	Inverted output signal of ONSW	VDDIO
SMPL	Power-on hold time setting capacitor connection at SMPL	VDDO
PSHOLD	- Signal input pin to maintain power-on - Self-reset input pin	VDDIO
RSTB	CPU reset signal output pin	VDDIO
chgpon	Power-on signal from charger block (Rapid Charge signal)	

Table 5-1. Pin/Signal Description

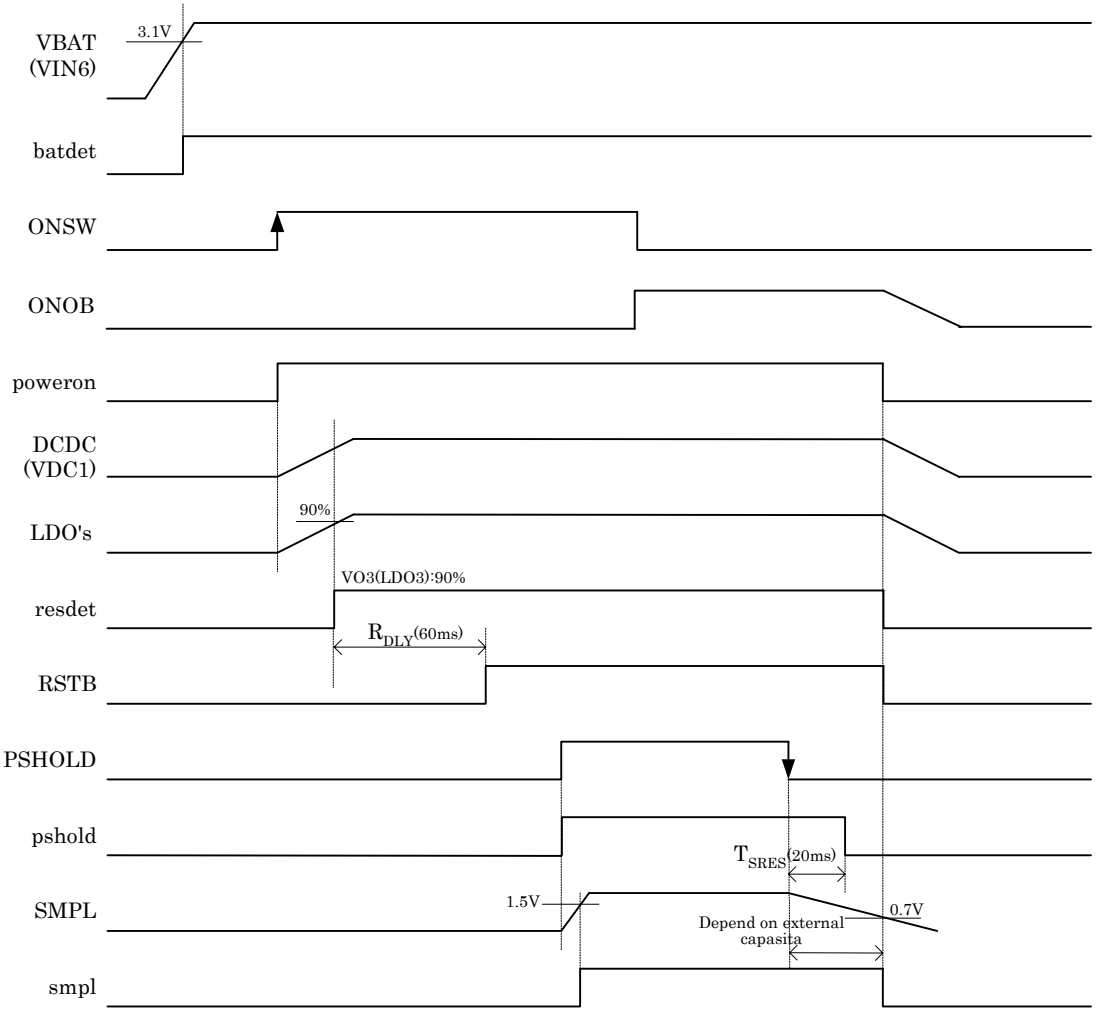
Pin/signal Name	Function	Level
rtcpon	RTC alarm interrupt signal	
clkstp	32 kHz oscillator stop signal	
poweron	DC/DC & LDO enable signal output	

Note: Pin & Bit name (capital letter), Signal name (lowercase), Register name (r + capital letter)

5.1.2 Power ON/OFF Operation

The AT73C206 is asserted by ONSW (External pin), rtcpon(RTC alarm interrupt), SMPL (Sudden Momentary Power Loss) or chgpon (Power-on signal from charger block).

Figure 5-2. Power ON/OFF Sequence

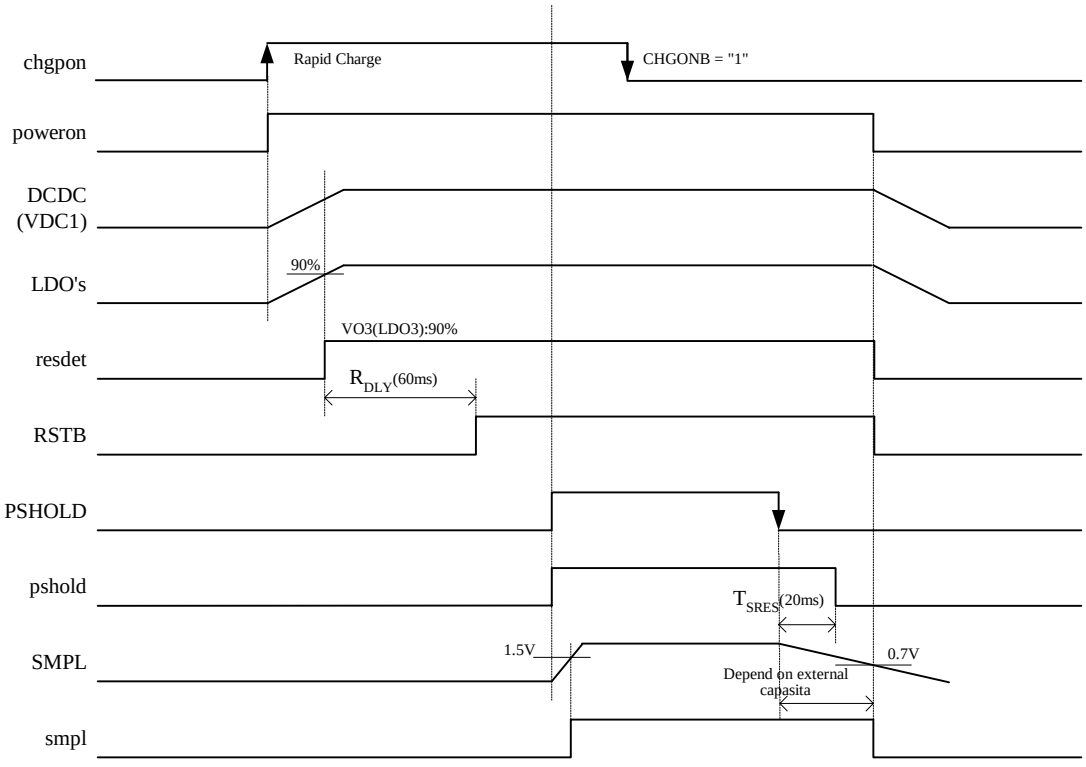


1. Power ON by ONSW pin
   When the "H" signal is input into ONSW pin at battery voltage over 3.1V, poweron signal goes "H" and DC/DC, LDO (GSP= “L”:LDO1, 3, 6, 7, GSP= “H”: LDO1,3,5,6,8) are turned on. ONOB goes “L”.
   When the output voltage of LDO3 reaches 90% of its regulation voltage, the internal

reset timer starts and outputs “L” through the RSTB pin. CPU powers up and RSTB pin becomes "H" after reset delay time 60ms (Typ). After CPU finishes its system initialization, CPU will turn PSHOLD to "H".The system can keep power on by holding this PSHOLD at "H". For this operation, it needs to push PSHOLD signal “H” before ONSW pin falls “L”. If ONSW falls “L” before pushing PSHOLD “H”, AT73C206 will power off.

2. Power ON by rtcpon signal
   When an interrupt generates in RTC block, rtcpon goes “H” and AT73C206 powers on performing same power-on sequence as ONSW.
3. Power ON by SMPL pin
   When PSHOLD goes "H", SMPL becomes "H" through the internal diode. SMPL keeps "H" by external capacitor even when the battery is momentarily disconnected.
   If it keeps "H" until battery is reconnected, AT73C206 powers on performing same power-on sequence as ONSW.
4. Power ON by chgpon signal
   When AC adapter is inserted, AT73C206 enters to Rapid Charge Mode and chgpon goes "H" and poweron signal goes “H” irrespective of BATDET output. PSHOLD functions as same as when power-on by ONSW.
   AT73C206 cannot perform power-off during Rapid Charge.

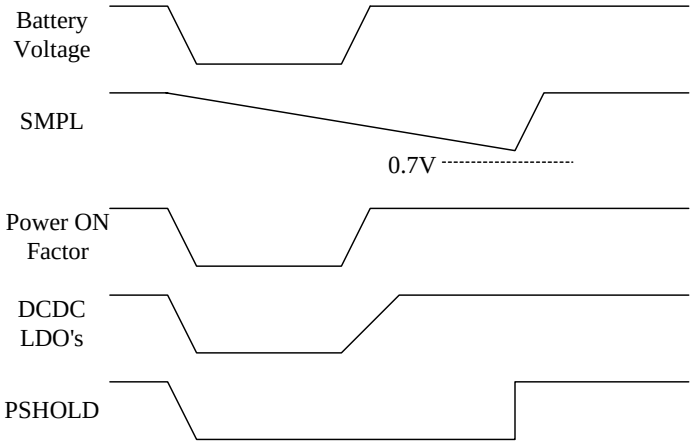
Figure 5-3. Power ON/OFF Sequence by chgpon



5.1.3 SMPL Operation

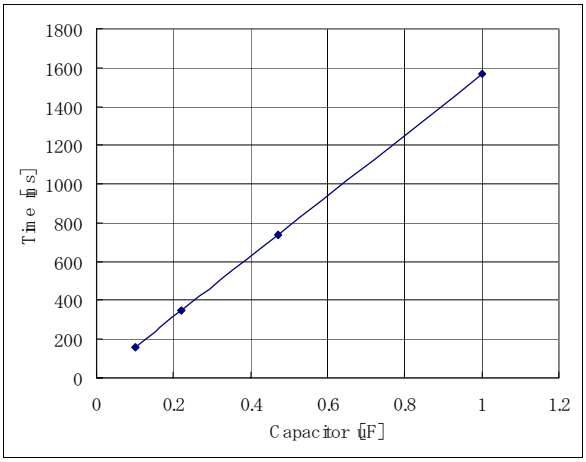
When the battery loses contact momentarily due to impact or vibration on the handset by some event such as dropping the device, SMPL remains “H” with capacitor and re-powers as the battery is reconnected. The SMPL “H” maintain time depends on the capacitor size. To achieve this function, pull PSHOLD “H” before SMPL falls down to 0.7V.

Figure 5-4. SMPL Operation Timing



5.1.3.1 Relation of SMPL-high-maintain-time vs. Capacitor when momentary power loss

Figure 5-5. SMPL-high-maintain-time when momentary power loss (VIN6 = 3.6V)



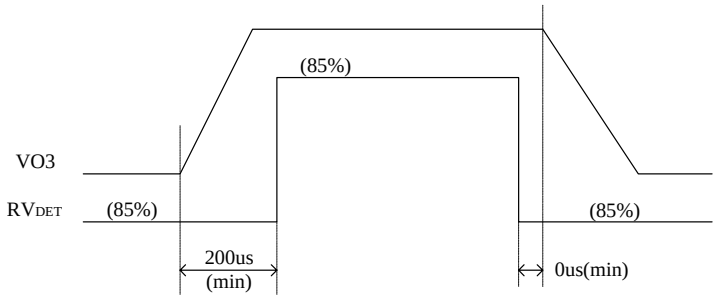
C[uF]	Time[ms]
0.10	157
0.22	345
0.47	738
1.00	1570

5.1.4 Voltage Detector

The AT73C206 has two voltage detectors in power control block, BATDET and RESDET. BATDET detects low battery voltage and RESDET detects the LDO3 output voltage and generates

the reset signal through RSTB pin. RESDET needs to change by LDO3 output voltage set. When raise LDO3 output setting voltage, set LDO3 output voltage by LDO3SEL bit first and then change RESDET voltage by RESDETSEL bit with 200us of delay time. Adversely, when lower LDO3 output setting voltage, RESDETSEL bit should be set prior to LDO3SEL bit.

Figure 5-6. VO3 and RESDET Control Timing



5.1.5 BATDET Electrical Characteristic

Operating Conditions (unless otherwise specified) $T_a = 25° C$.

Table 5-2. BATDET Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
BV_{REL}	BATDET Cancellation Voltage	Battery Voltage Rising	-3 %	3.1	+3 %	V
BV_{DET}	BATDET Detection Voltage	Battery Voltage Falling		2.9		V

5.1.6 RESDET Electrical Characteristic

Operating Conditions (unless otherwise specified) VIN = 3.6V, $T_a = 25° C$.

Table 5-3. RESDET Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
RV_{REL}	RESDET Cancellation Voltage	VO3 Voltage Rising	-3	90	+3	%
RV_{DET}	RESDET Detection Voltage	VO3 Voltage Falling		85		%

5.1.7 RSTB Electrical Characteristic

Operating Conditions (unless otherwise specified) VIN = 3.6V, $T_a = 25° C$.

Table 5-4. RSTB Electrical Characteristics

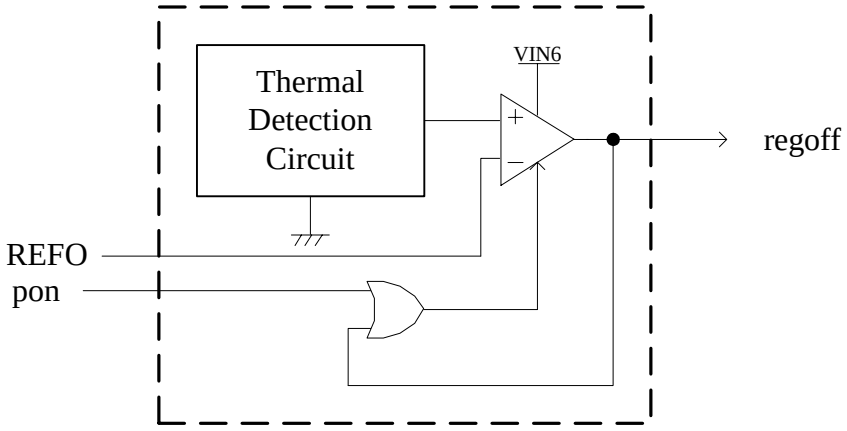
Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{DLY}	Reset Delay Timer	Delay Time from VO390% to RSTB = “H”		60		ms

5.1.8 Thermal Shutdown Circuit

The thermal shutdown circuit consists of Thermal Detection Circuit and Comparator.

5.1.8.1 Thermal Shutdown Block Diagram

Figure 5-7. Thermal Shutdown Block Diagram



5.1.8.2 Thermal Shutdown Explanation of Operation

Thermal shutdown circuit detects overheat state by comparing the output voltages of Thermal Detection Circuit and REFO. If the overheat state is detected, AT73C206 will turn off to protect itself from overheating. It is impossible to power on AT73C206 at overheat state.

5.1.8.3 Target Thermal Shutdown Electrical Characteristics

Operating Conditions (unless otherwise specified) VIN = 3.6V

Table 5-5. Thermal Shutdown Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DET}	Detected Temperature			140		
T_{RET}	Return Temperature			110		
I_{SS1}	Supply Current	Ta = 25° C		5	15	uA
I_{SS2}	Standby Current	Ta = 25° C			1	uA

5.1.9 Self-reset by PSHOLD

When PSHOLD pin is held at “L” more than 20 ms, AT73C206 powers off as described in Section 5.1.2 “Power ON/OFF Operation” on page 8.

However, if PSHOLD pin is pushed up “H” within 20 ms, the AT73C206 will conduct self-reset by RSTB= “L” for 60 ms.

When self-reset, the DC/DC and LDOs are all reset to initial state since all the register is initialized.

After self-reset, AT73C206 maintains power-on by PSHOLD="H" as same as when normal power-on.

Figure 5-8. Self-reset

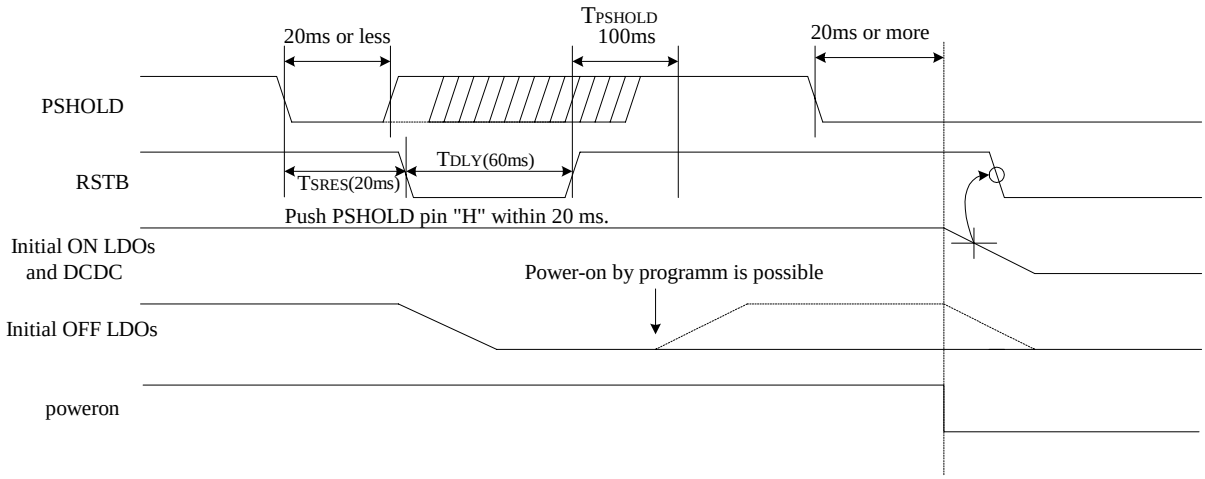


Table 5-6. Self-reset Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SRES}	Self-reset time			20		ms
T_{PSHOLD}	PSHOLD time			100		ms

5.1.10 Oscillator Stop

If the 32 kHz clock oscillator stops, clkstp signal goes "H" and self-reset function becomes invalid. In this case, PSHOLD= “L” will power off the AT73C206.

Also, when the 32 kHz clock oscillator stops, AT73C206 generates an interrupt. (See “Power-on reset and Oscillator stop detection function” on page 42.)

5.2 Regulators

The AT73C206 has 9 Low Drop Output regulators. The output voltage of LDO1, 3, 4, 5 and 8 are programmable. LDO1 must be power supplied by DC/DC output (1.8V) and the other LDOs are power supplied by battery.

The initial output voltage of LDO1 is selectable by LDO1SEL pin or GSP pin. After power-on, the LDO1 output voltage is programmable via SPI.

After power-on, the output voltages for LDO3, 4, 5 and 8 are programmable via SPI.

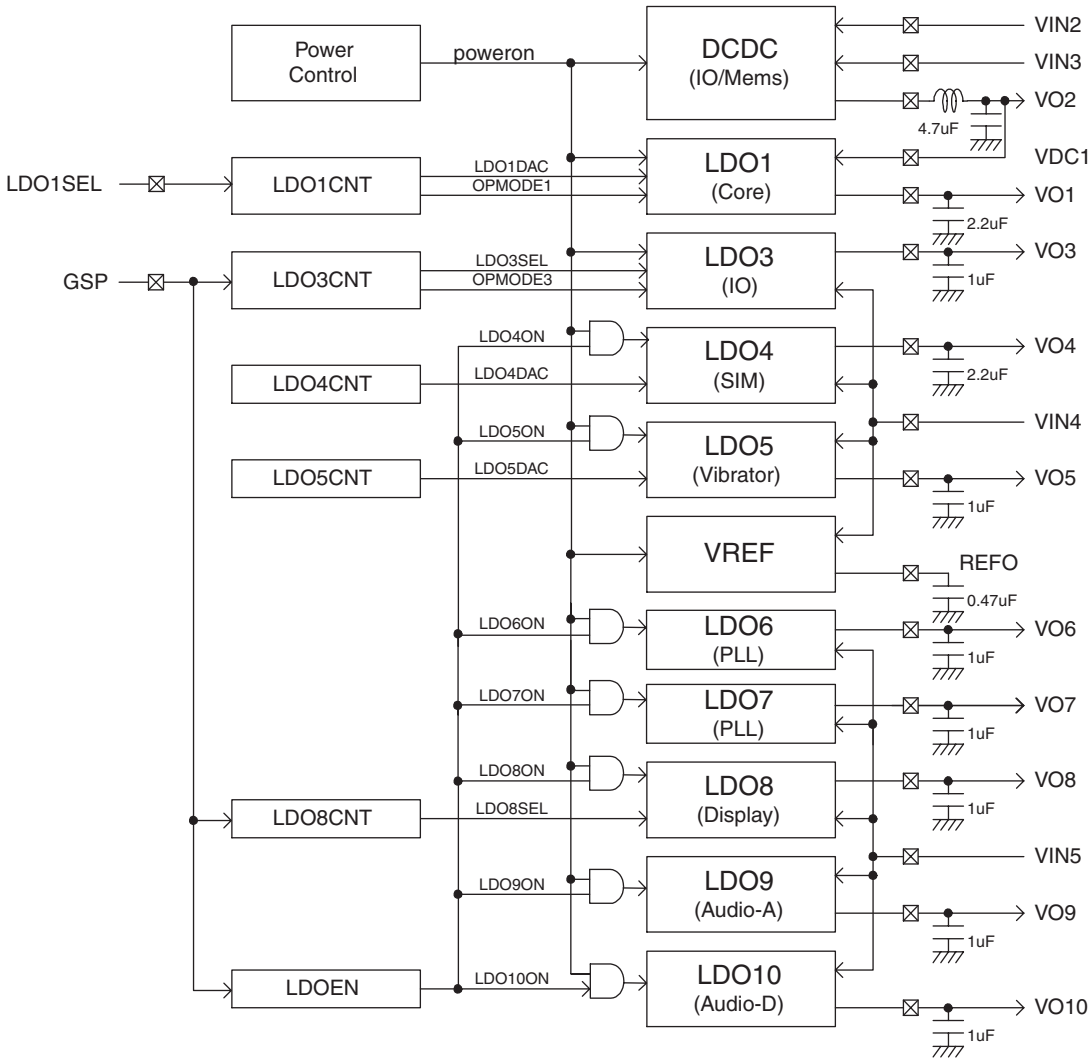
Power on/off of LDO4 to 10 regulators and switchover between ECO-mode and Normal-mode of LDO1 and 3 are controllable via SPI.

For optimized phase compensation, the bypass capacitor must be ceramic type.

VREF regulator provides reference voltage to LDO1, 3, 5, 6, 7, 10, RESDET and TSHUT.

5.2.1 LDO Regulator Block Diagram

Figure 5-9. LDO Regulator Block Diagram



5.2.2 Linear Regulators Table

Table 5-7. Linear Regulators Table

	GSP	LDO1 (Core)	LDO3 (IO)	LDO4 (SIM)	LDO5 (Vibrator)	LDO6 (PLL)	LDO7 (PLL)	LDO8 (Display)	LDO9 (Audio Analog)	LDO10 (Audio Digital)
Initial Value	L	1.3V/1.5V (LDO1SEL)	2.5V	1.8V	3.0V	1.3V	1.3V	1.8V	2.8V	2.8V
	H	1.3V/1.5V (LDO1SEL)	2.8V	1.8V	2.8 V			2.8V		
Output current max		300mA	100mA	200mA	100mA	20mA	20mA	150mA	100mA	100mA
Programmable Output Voltage		0.9V 1.0V 1.3V 1.5V	2.5V 2.8V 3.0V	1.8V 2.8V 3.0V 3.1V	2.7V 2.8V 3.0V 3.3V	Fixed	Fixed	1.8V 2.8V	Fixed	Fixed
Initial State	L	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF
	H	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF
ECO-mode		Yes	Yes	No	No	No	No	No	No	No
ON/OFF Control				SPI (LDO4ON)	SPI (LDO5ON)	SPI (LDO6ON)	SPI (LDO7ON)	SPI (LDO8ON)	SPI (LDO9ON)	SPI (LDO10ON)
Bypass Capacitor (C_{OUT})		2.2uF	1.0uF	2.2uF	1.0uF	1.0uF	1.0uF	1.0uF	1.0uF	1.0uF

Table 5-8. Recommended Capacitor

Capacitor	Manufacturer	Model No
2.2 uF	TAIYO YUDEN®	JMK107BJ225KA
1.0 uF	TAIYO YUDEN®	JMK105BJ105KVB

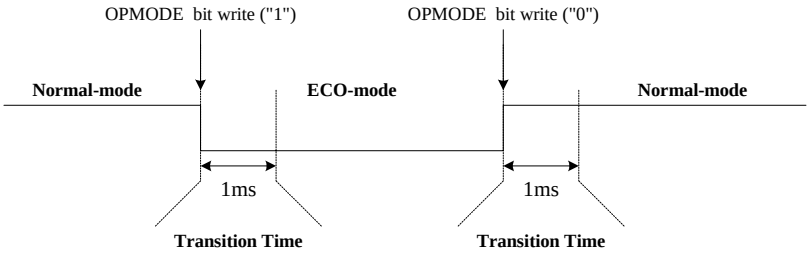
5.2.3 ECO-mode of LDO1 and 3

During ECO-mode, LDO1 and 3 are operating on the low bias current for reducing the power consumption. When CPU are in Sleep State or Low Power State, ECO-mode makes it possible to keep outputting voltage to peripheral ICs at low power consumption current. The maximum output current in ECO-mode is half as much as in Normal-mode.

LDO1 and 3 can be ECO-mode by setting the corresponding bits to the operation mode control register OPMODE1and OPMODE3.

5.2.3.1 Timing Chart of Switchover between ECO-mode and Normal-mode

Figure 5-10. Transition from Normal to ECO, ECO to Normal



Note: When operation mode is changed, AT73C206 has 1ms of transition time. Mode transition is not recommendable during this mode transition time (1ms). The maximum output current during transition is same as ECO-mode.

5.2.4 LDO1 Electrical Characteristic

5.2.4.1 NORMAL Mode

Operating Normal Conditions (unless otherwise specified): VDDIN1 = $DCDC_{OUT}$ = 1.8V, C_{OUT} = 2.2uF, T_a = 25° C.

Table 5-9. LDO1 Normal Mode Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT1	Output Voltage	1.8V(-3%) ≤VDDIN1 ≤1.8V(+3%) 50uA < IOUT1 < Ioutmax	-3%	1.3/1.5	+3%	V
IOUT1	Output Current	-----			300	mA
ISHT1	Short Current	VO1=0V		200		mA
$\frac{\Delta VOUT1}{\Delta VIN}$	Line Regulation	1.8V(-3%) ≤VDDIN1 ≤1.8V(+3%) IOUT1 = Ioutmax/2			10	mV
$\frac{\Delta VOUT1}{\Delta IOUT1}$	Load Regulation	50uA < IOUT1 < Ioutmax			30	mV
$\frac{\Delta VOUT1}{\Delta T_a}$	Output Voltage Temperature Coefficient	-40° C ≤T_a ≤85° C		±100		ppm
RR1	Ripple Rejection	f=1kHz, IOUT1= Ioutmax/2		60		dB
EN1	Output Noise (RMS)	BW=100Hz-100kHz, IOUT1= Ioutmax/2		70		uVrms
ISS1	Supply Current	(IOUT1=0mA)		80		uA
IOFF1	Standby Current	IOUT1=0mA			1	uA
V_{Tr1}	Rising Time	IOUT1= 0mA VO1 > VOUT1 x 90%		200		us
V_{Tf1}	Falling Time	IOUT1=0mA VO1 < 0.5V			500	us
POUT1	Programmable Output Voltage	IOUT1= Ioutmax/2		0.9V 1.0V 1.3V 1.5V		V

5.2.4.2 ECO mode

Table 5-10. LDO1 ECO Mode Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT1	Output Voltage	1.8V(-3%) ≤VDDIN1 ≤1.8V(+3%) IOUT1= Ioutmax/2	-3%	1.3/1.5	+3%	V
IOUT1	Output Current	-----			150	mA
ISHT1	Short Current	VO1=0V		200		mA
ISS1	Supply Current	IOUT1= 0mA		3		uA
POUT1	Programmable Output Voltage	IOUT1= Ioutmax/2	-4%	0.9V 1.0V	+4%	V
			-3%	1.3V 1.5V	+3%	

5.2.5 LDO3 Electrical Characteristic

5.2.5.1 NORMAL mode

Operating Normal Conditions (unless otherwise specified): VIN = 3.6V, C_{OUT} = 1uF, T_a = 25° C

Table 5-11. LDO3 Normal Mode Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT3	Output Voltage	3.1V ≤VIN ≤4.2V 50uA < IOUT3 < Ioutmax	-3%	2.5	+3%	V
IOUT3	Output Current	-----			100	mA
ISHT3	Short Current	VO3=0V		60		mA
ΔVOUT3 ΔVIN	Line Regulation	3.1V ≤VIN ≤4.2V IOUT3=Ioutmax/2			10	mV
ΔVOUT3 ΔIOUT3	Load Regulation	50uA < IOUT3 < Ioutmax			20	mV
ΔVOUT3 ΔT_a	Output Voltage Temperature Coefficient	-40° C ≤T_a ≤85° C		±100		ppm
RR3	Ripple Rejection	f=1kHz, IOUT3= Ioutmax/2		60		dB
EN3	Output Noise (RMS)	BW=100Hz-100kHz, IOUT3= Ioutmax/2		100		uVrms
ISS3	Supply Current	(IOUT3=0mA)		50		uA
IOFF3	Standby Current	IOUT3=0mA			1	uA
V_{Tr3}	Rising Time	IOUT3= 0mA VO3 > VOUT3 x 90%		200		us
V_{Tf3}	Falling Time	IOUT3=0mA VO3 < 0.5V			500	us
POUT3	Programmable Output Voltage	IOUT3= Ioutmax/2	-3%	2.5V 2.8V 3.0V	+3%	V

5.2.5.2 ECO mode

Table 5-12. LDO3 ECO Mode Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT3	Output Voltage	3.1V ≤VIN ≤4.2V IOUT3= Ioutmax/2	-3%	2.5	+3%	V
IOUT3	Output Current	-----			50	mA
ISHT3	Short Current	VO3=0V		60		mA
ISS3	Supply Current	IOUT3= 0mA		3		uA
POUT3	Programmable Output Voltage	IOUT3= Ioutmax/2	-3%	2.5V 2.8V 3.0V	+3%	V

5.2.6 LDO4 Electrical Characteristic

Operating Conditions (unless otherwise specified) VIN = 3.6V, C_{OUT} = 2.2uF, T_a = 25° C.

Table 5-13. LDO4 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT4	Output Voltage	3.1V ≤VIN ≤4.2V 50uA < IOUT4 < Ioutmax	-3%	1.8	+3%	V
IOUT4	Output Current	-----			200	mA
ISHT4	Short Current	VO4=0V		100		mA
ΔVOUT4 ΔVIN	Line Regulation	3.1V ≤VIN ≤4.2V IOUT4=Ioutmax/2			10	mV
ΔVOUT4 ΔIOUT4	Load Regulation	50uA < IOUT4 < Ioutmax			30	mV
ΔVOUT4 ΔT_a	Output Voltage Temperature Coefficient	-40° C ≤T_a ≤85° C		±100		ppm
RR4	Ripple Rejection	f=1kHz, IOUT4 = Ioutmax/2		60		dB
EN4	Output Noise (RMS)	BW=100Hz-100kHz, IOUT4= Ioutmax/2		50		uVrms
ISS4	Supply Current	(IOUT4=0mA)		80		uA
IOFF4	Standby Current	IOUT4=0mA			1	uA
V_{Tr4}	Rising Time	IOUT4= 0mA VO4 > VOUT4 x 90%		200		us
V_{Tf4}	Falling Time	IOUT4=0mA VO4 < 0.5V			500	us
POUT4	Programmable Output Voltage	IOUT4 = Ioutmax/2		1.8V 2.8V 3.0V 3.1V		V

5.2.7 LDO5 Electrical Characteristic

Operating Conditions (unless otherwise specified): VIN = 3.6V, C_{OUT} = 1 uF, T_a = 25° C.

Table 5-14. LDO5 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT5	Output Voltage	3.1V ≤VIN ≤4.2V 50uA < IOUT5 < Ioutmax	-3%	3.0	+3%	V
IOUT5	Output Current	-----			100	mA
ISHT5	Short Current	VO5=0V		60		mA
ΔVOUT5 ΔVIN	Line Regulation	3.1V ≤VIN ≤4.2V IOUT5=Ioutmax/2			10	mV
ΔVOUT5 ΔIOUT5	Load Regulation	50uA < IOUT5 < Ioutmax			20	mV
ΔVOUT5 ΔT_a	Output voltage Temperature Coefficient	-40° C ≤T_a ≤85° C		±100		ppm/
ISS5	Supply Current	IOUT5 = 0mA		50		uA
IOFF5	Standby Current	IOUT5 = 0mA			1	uA
V_{Tr5}	Rising Time	IOUT5= 0mA VO5 > VOUT5 x 90%		200		us
V_{Tf5}	Falling Time	IOUT5=0mA VO5 < 0.5V			500	us
POUT5	Programmable Output Voltage	IOUT5 = Ioutmax/2		2.8V 3.0V 3.3V		V

5.2.8 LDO6 Electrical Characteristic

Operating Conditions (unless otherwise specified): VIN = 3.6V, C_{OUT} = 1uF, T_a = 25° C.

Table 5-15. LDO6 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT6	Output Voltage	3.1V ≤VIN ≤4.2V 50uA < IOUT6 < Ioutmax	-3%	1.3	+3%	V
IOUT6	Output Current	-----			20	mA
ΔVOUT6 ΔVIN	Line Regulation	3.1V ≤VIN ≤4.2V IOUT6 = Ioutmax/2			10	mV
ΔVOUT6 ΔIOUT6	Load Regulation	50uA < IOUT6 < Ioutmax			10	mV
ΔVOUT6 ΔT_a	Output Voltage Temperature Coefficient	-40° C ≤T_a ≤85° C		±100		ppm/
RR6	Ripple Rejection	f=1kHz, IOUT6= Ioutmax/2		60		dB
ISS6	Supply Current	(IOUT6=0mA)		50		uA
IOFF6	Standby Current	IOUT6=0mA			1	uA
V_{Tr6}	Rising Time	IOUT6=0mA VO6 > VOUT6 x 90%		200		us
V_{Tf6}	Falling Time	IOUT6=0mA VO6 < 0.5V			500	us

5.2.9 LDO7 Electrical Characteristic

Operating Conditions (unless otherwise specified) VIN = 3.6V, C_{OUT} = 1uF, T_a = 25° C.

Table 5-16. LDO7 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT7	Output Voltage	3.1V ≤VIN ≤4.2V 50uA < IOUT7 < Ioutmax	-3%	1.3	+3%	V
IOUT7	Output Current	-----			20	mA
ΔVOUT7 ΔVIN	Line Regulation	3.1V ≤VIN ≤4.2V IOUT7 = Ioutmax/2			10	mV
ΔVOUT7 ΔIOUT7	Load Regulation	50uA < IOUT7 < Ioutmax			10	mV
ΔVOUT7 ΔT_a	Output Voltage Temperature Coefficient	-40° C ≤T_a ≤85° C		±100		ppm/
RR7	Ripple Rejection	f=1kHz, IOUT7= Ioutmax/2		60		dB
ISS7	Supply Current	(IOUT7=0mA)		50		uA
IOFF7	Standby Current	IOUT7=0mA			1	uA
V_{Tr7}	Rising Time	IOUT7=0mA VO7 > VOUT7 x 90%		200		us
V_{Tf7}	Falling Time	IOUT7 = 0mA VO7 < 0.5V			500	us

5.2.10 LDO8 Electrical Characteristic

Operating Conditions (unless otherwise specified) VIN = 3.6V, C_{OUT} = 1uF, T_a = 25° C.

Table 5-17. LDO8 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT8	Output Voltage	3.1V ≤VIN ≤4.2V 50uA < IOUT8 < Ioutmax	-3%	1.8	+3%	V
IOUT8	Output Current	-----			150	mA
ISHT8	Short Current	VO8=0V		100		mA
ΔVOUT8 ΔVIN	Line Regulation	3.1V ≤VIN ≤4.2V IOUT8=Ioutmax/2			10	mV
ΔVOUT8 ΔIOUT8	Load Regulation	50uA < IOUT8 < Ioutmax			30	mV
ΔVOUT8 ΔT_a	Output Voltage Temperature Coefficient	-40° C ≤T_a ≤85° C		±100		ppm/
RR8	Ripple Rejection	f=1kHz, IOUT8= 30mA		70		dB
EN8	Output Noise (RMS)	BW=100Hz-100kHz, IOUT8=30 mA		50		uVrms
ISS8	Supply Current	IOUT8 = 0mA		100		uA
IOFF8	Standby Current	IOUT8 = 0mA			1	uA
V_{Tr8}	Rising Time	IOUT8= 0mA VO8 > VOUT8 x 90%		200		us
V_{Tf8}	Falling Time	IOUT8=0mA VO8 < 0.5V			500	us
POUT8	Programmable Output Voltage	IOUT8 = Ioutmax/2		1.8 2.8		V

5.2.11 LDO9 Electrical Characteristic

Operating Conditions (unless otherwise specified) VIN = 3.6V, C_{OUT} = 1uF, T_a = 25° C.

Table 5-18. LDO9 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT9	Output Voltage	3.1V ≤VIN ≤4.2V 50uA < IOUT9 < Ioutmax	-3%	2.8	+3%	V
IOUT9	Output Current	-----			100	mA
ISHT9	Short Current	VO9=0V		60		mA
ΔVOUT9 ΔVIN	Line Regulation	3.1V ≤VIN ≤4.2V IOUT9=Ioutmax/2			10	mV
ΔVOUT9 ΔIOUT9	Load Regulation	50uA < IOUT9 < Ioutmax			20	mV
ΔVOUT9 ΔT_a	Output Voltage Temperature Coefficient	-40° C ≤T_a ≤85° C		±100		ppm/
RR9	Ripple Rejection	f=1kHz, IOUT9=Ioutmax/2		70		dB
EN9	Output Noise (RMS)	BW=100Hz-100kHz, IOUT9=Ioutmax/2		50		uVrms
ISS9	Supply Current	IOUT9 = 0mA		100		uA
IOFF9	Standby Current	IOUT9 = 0mA			1	uA
V_{Tr9}	Rising Time	IOUT9= 0mA VO9 > VOUT9 x 90%		200		us
V_{Tf9}	Falling Time	IOUT9=0mA VO9 < 0.5V			500	us

5.2.12 LDO10 Electrical Characteristic

Operating Conditions (unless otherwise specified) VIN = 3.6V, C_{OUT} = 1uF, T_a = 25° C.

Table 5-19. LDO10 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT10	Output Voltage	3.1V ≤VIN ≤4.2V 50uA < IOUT10 < Ioutmax	-3%	2.8	+3%	V
IOUT10	Output Current	-----			100	mA
ISHT10	Short Current	VO10=0V		60		mA
ΔVOUT10 ΔVIN	Line Regulation	3.1V ≤VIN ≤4.2V IOUT10=Ioutmax/2			10	mV
ΔVOUT10 ΔIOUT10	Load Regulation	50uA < IOUT10 < Ioutmax			20	mV
ΔVOUT10 ΔT_a	Output Voltage Temperature Coefficient	-40° C ≤T_a ≤85° C		±100		ppm/
RR10	Ripple Rejection	f=1kHz, IOUT10=Ioutmax/2		60		dB
EN10	Output Noise (RMS)	BW=100Hz-100kHz, IOUT10=Ioutmax/2		110		uVrms
ISS10	Supply Current	IOUT10 = 0mA		50		uA
IOFF10	Standby Current	IOUT10 = 0mA			1	uA
V_{Tr10}	Rising Time	IOUT10= 0mA VO10 > VOUT10 x 90%		200		us
V_{Tf10}	Falling Time	IOUT10=0mA VO10 < 0.5V			500	us

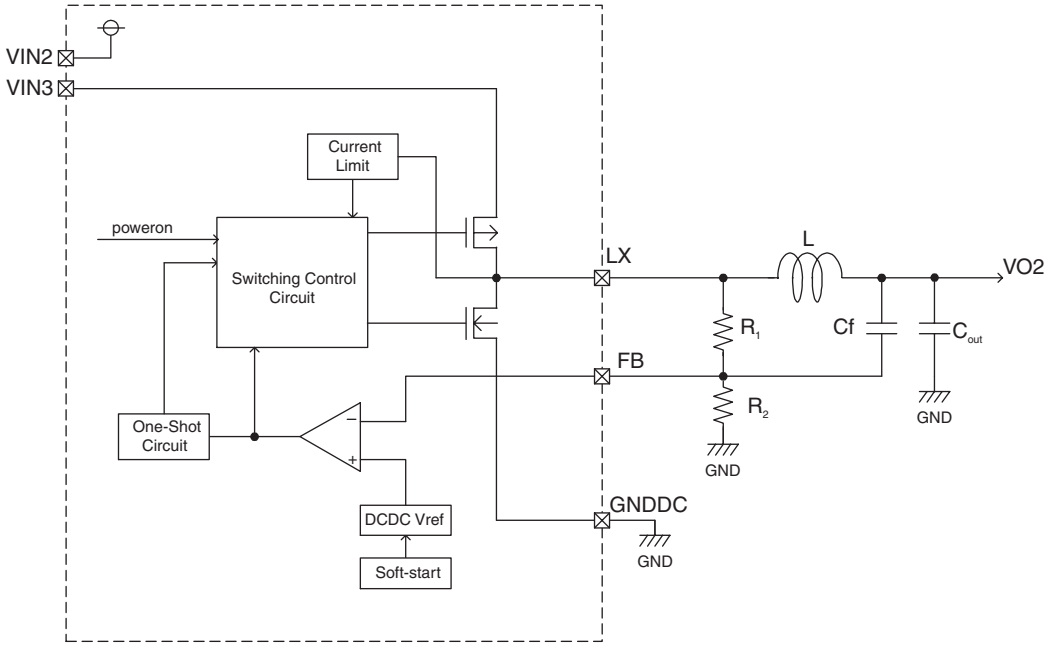
5.3 Step-down DC/DC Converter

AT73C206 has a one-shot PWM DC/DC converter. It employs external inductor and capacitor for smoothing output voltage and also external R_1, R_2 and Cf for both voltage setting and phase compensation.

The Control Circuit is power supplied by VIN2 and the Switch Transistor is power supplied by VIN3. AT73C206 features soft-start to reduce inrush current at power-on and current limit circuit for over-current protection.

5.3.1 Step-down DC/DC Converter Block Diagram

Figure 5-11. Step-down DC/DC Converter Block Diagram



5.3.2 Step-down DC/DC Converter Operation

During standby mode, LX pin is high impedance. When DC/DC becomes active, the internal soft-start circuit is enabled and output voltage starts boosting. AT73C206 compares internal reference voltage (typ.0.6V) and FB voltage. If FB voltage is below the reference voltage, it turns on high-side switch by enabling one-shot circuit.

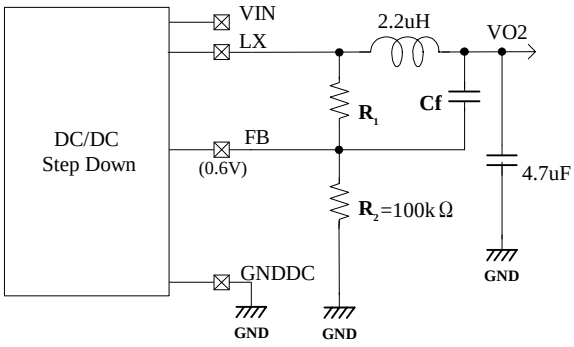
The high-side switch remains on for minimum-on-time or until FB voltage rises over the reference voltage or inductor current exceeds limit current. Once the high-side switch is disabled, it remains off until FB voltage falls below the reference voltage or inductor current falls below the limit current. During high-side switch is off, low-side switch remains on until inductor current approaches 0. The DC/DC converter regulates the output voltage by repeating the above operation.

Therefore, oscillator frequency varies by input voltage, output voltage, output current and external circuit (R1, L, Cf).

In addition, the feedback loop from LX pin through R1 and from VO2 through Cf eliminate phase lag by output capacitor providing the stable loop and fast transient response.

However, the output voltage is reduced by output current on DCR of inductor. (Theoretically, output voltage falls [IOUT(A) x DCR(Ohm)])

5.3.3 Output Voltage Setting Calculation Formula



The output voltage can be calculated by formular below.

$$VOUT2 = \frac{(R_1+R_2)\times 0.6}{R_2}$$

VOUT2 = Output Voltage
R_1= Upper part resistance

The phase margin capacitor is determined by formular below.

$$Cf \fallingdotseq \frac{L \times 10}{R_1}$$

Use the external components below for VOUT2=1.8V.

L=2.2 uH, R_1=200 kΩ, R_2=100 kΩ, VOUT2=1.8V, Cf=110 pF, Cout=4.7 uF

5.3.4 Step-down DC/DC Converter Electrical Characteristic

Operating Conditions (unless otherwise specified): VIN=3.6V, T_a = 25° C, L=2.2uH, Cout=4.7uF

Table 5-20. Step-down DC/DC Converter Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{BATT}	Input Voltage		3.1		4.2	V
VOUT2	Output Voltage Range		0.9	1.8	2.5	V
IOUTD	Output current	V_{IN}=3.1 to 4.2V			650	mA
ISSD	Consumption Current	V_{IN}=3.1 to 4.2V IOUTD=0mA, no switching		80		uA
IOFFD	Standby Current	V_{IN}=4.2V OFF state			1	uA
ILIMD	Limit detection Current		800			mA
VFB	FB Voltage		-1.5%	0.6	+1.5%	V
ΔVFB ΔVIN	FB Line Regulation	V_{IN}=3.1 to 4.2V IOUTD= Ioutmax/2		5		mV
h	Efficiency	R1=200 kΩ, R2=100 kΩ, Cf=110 pF, IOUTD=200mA		90		
t_r	Rising Time	Soft-start		120		us
ΔVFB ΔT	FB Voltage Temperature Coefficient	-30 ≤Ta ≤+85		±100		ppm/
Tonmin	Minimum-On-Time			100		ns

Note: Load Regulation, which is determined by DC resistance (DCR) on inductor, is given by:

Load Regulation(Typ) = DCR(Ω) x IOUTDA (A)

For example, if DCR is 100 mΩ;

0.1Ω x 0.65A = 65 mV (Typ.)

5.4 White LED Driver and Charge Pump

5.4.1 Charge Pump

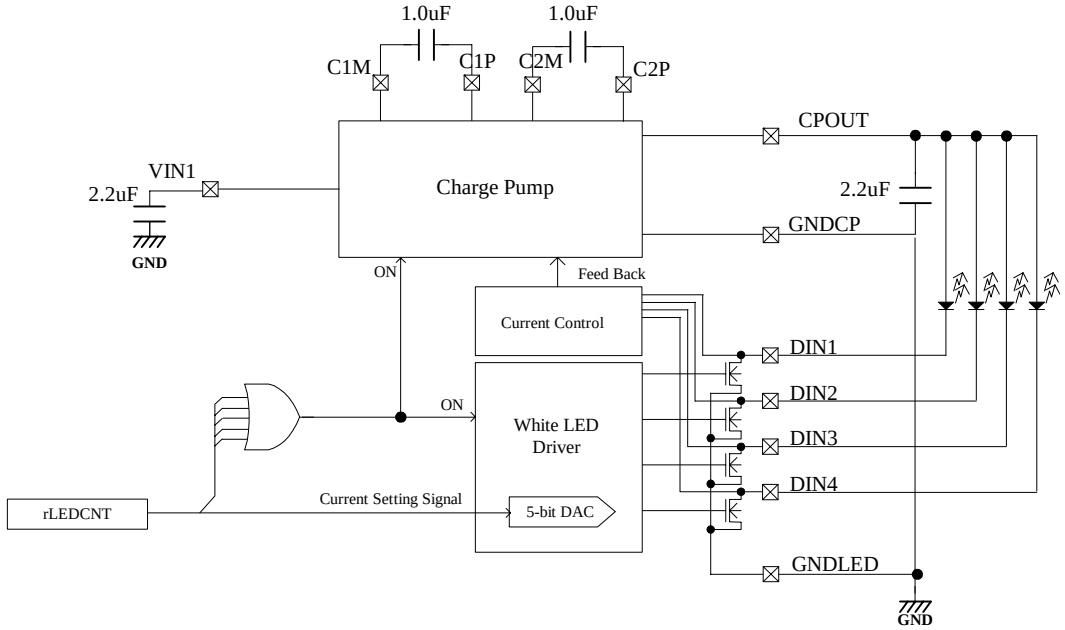
The AT73C206 integrates boost Charge Pump for White LED driver. For maximized power efficiency, the Charge Pump operates in 1x mode, 1.5x mode and 2x mode. It includes over-voltage lockout circuit to control the output voltage below the over-voltage detection voltage and Soft-start circuit to prevent excessive inrush current at power-on. The Charge Pump is on except when LEDCNT register is set to “0”.

5.4.2 White LED Driver

The AT73C206 White LED driver drives up to 4 White LEDs with regulated constant current. It integrates 5-bit DAC and performs the brightness control in 32-step by register set.

5.4.3 Block Diagram

Figure 5-12. White LED Driver and Charge Pump Block Diagram



5.4.4 Charge Pump Operation

5.4.4.1 Initial

When AT73C206 powers on, the Charge Pump initially starts in 1x mode and VOUT outputs VIN voltage. At this moment, the built-in soft-start circuit prevents excessive inrush current. See (1) in Figure 5-13 on page 31.

5.4.4.2 1x mode

The Charge Pump switches to 1.5x mode if any DIN pin meets the following condition:

DIN<0.25V

See (2) in Figure 5-13 on page 31.

5.4.4.3 1.5x mode

The Charge Pump switches to 2x mode if any DIN pin meets the following condition:

DIN<0.25V

See (3) in Figure 5-13 on page 31.

Every second, Charge Pump switches to 1x check mode only for 100us. Then it switches to:

- 1x mode if any DIN pin meets the following condition:
  DIN>0.4V

See (5) in Figure 5-13 on page 31.

- 1.5x mode if any DIN pin meets the following condition:
  DIN<0.4V

See (6) in Figure 5-13 on page 31.

5.4.4.4 2x mode

Every second, Charge Pump switches to 1.5x check mode for 100us. Then it switches to:

- 1.5x mode if any DIN pin meets the following condition:
  DIN>0.4V

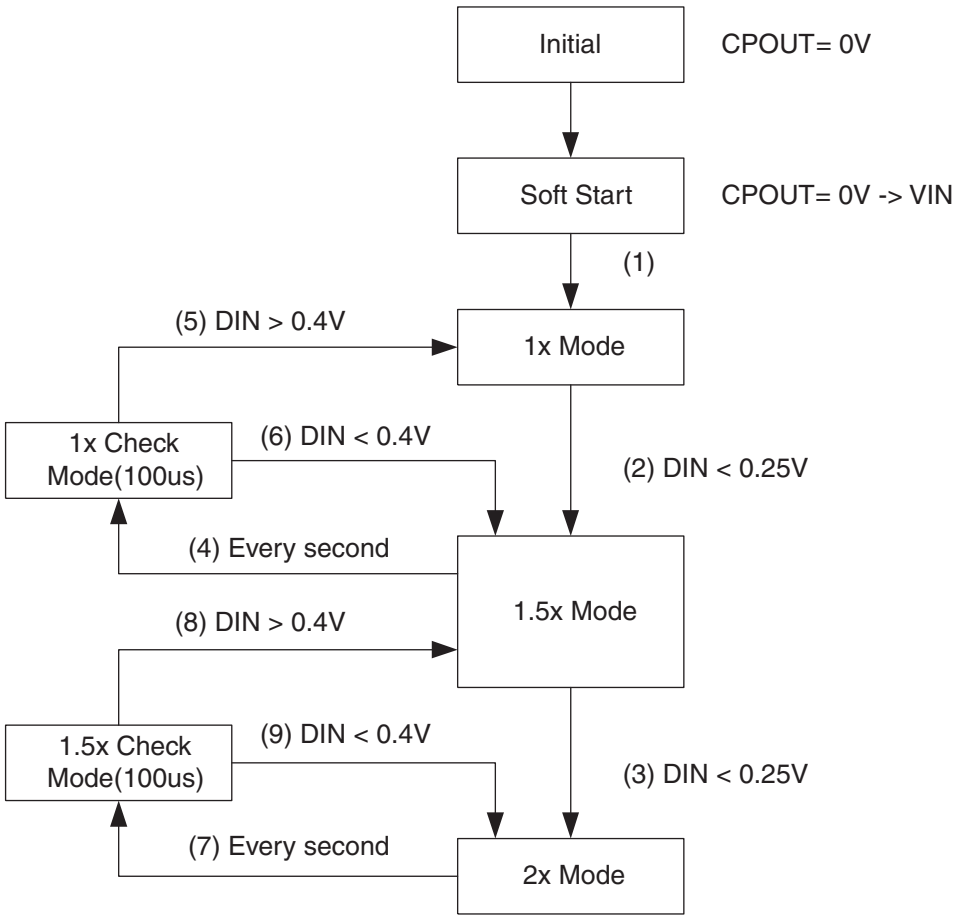
See (8) in Figure 5-13 on page 31.

- 2x mode if any DIN pin meets the following condition:
  DIN<0.4V

See (9) in Figure 5-13 on page 31.

5.4.4.5 1x/1.5x/2x mode transition

Figure 5-13. Mode Transition Diagram



5.4.5 Protection Circuit

When any DIN pin is floating or grounded during operation, Charge Pump pin switches over to 2x mode following mode transition sequence. At that time, over-voltage lockout circuit regulates output voltage below the protection voltage by on/off boost operation periodically.

Besides, when CPOUT is smaller than 1.2V, Short-Circuit Protection stops boost-operation and regulates output current. In addition, the protection operation halts when Charge Pump stops.

5.4.6 Unused DIN Pin

In case there is any unused DINx pin, connect it to GND. Then, the AT73C206 recognizes the unused pin at power-on and then excludes it from mode transition condition.

5.4.7 Target Charge Pump and White LED Driver Electrical Characteristics

Unless noted, VIN=3.6V, Ta=25° C, C1=C2=1uF, Cout=2.2uF

Table 5-21. Charge Pump and White LED Driver Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Charge Pump						
VIN	Operation voltage range	VIN1 voltage	3.1		4.5	V
V_{OVLV}	Over-voltage lockout voltage	Repeat ON/OFF		4.8		V
IOUT	Output current	VIN1>3.1V, CPOUT=4.2V			100	mA
f_{CP}	Switching frequency			1.25		MHz
t_S	Soft-start time			0.3		ms
ISS	Supply current	1x mode, No load, (DET, Reference ON)		500		uA
		1.5x mode or 2x mode		5		mA
IOFF	Standby supply current	VIN1 current		1		uA
ISHT	Short current	CPOUT=0V		50		mA
White LED Driver						
ILED	Sink current range	DIN1-4	0		25	mA
Iacc	LED current accuracy	IDIN=25mA=1Fh, DINx=0.25V	-5		5	%
Imat	LED current matching		-3		3	%
Vtth	1x to 1.5x, 1.5x to 2x transition threshold voltage	If any pin among DIN1-4 falls under,		250		mV
Vthys	1x to 1.5x, 1.5x to 2x transition hysteresis voltage			150		mV
ttr	1x to 1.5x, 1.5x to 2x transition time			100		us
Ilsd	DIN1-4 leakage current when shut-down			0.01		uA

5.5 Li-ion Battery Charger

5.5.1 Description

The Li-ion battery charger contains a Charge Regulator, Charge Control Circuit, Charge Current Monitor, AC Adapter Detector, AC Adaptor Over-voltage Detector and Chip Temperature Detector.

It has 2 charge modes, Trickle Charge and Rapid Charge, the charge current of which is controlled by registers.

When AT73C206 detects that chip temperature approaches the die temperature by chip temperature Detector, which is user selectable by register, it reduces charge current to 20% of charge current.

When AT73C206 detects over-voltage by adaptor over-voltage detector, it stops charging and outputs over-voltage interrupt request flag (ADPBIR & ADPIR). Thousandth of charge current is output from IMONI pin. The resistor on IMONI pin converts the charge current to voltage. This feature allows AT73C206 to monitor charge current through ADC.

5.5.2 Li-ion Battery Charger Block Diagram

Figure 5-14. Li-ion Battery Charger Block Diagram

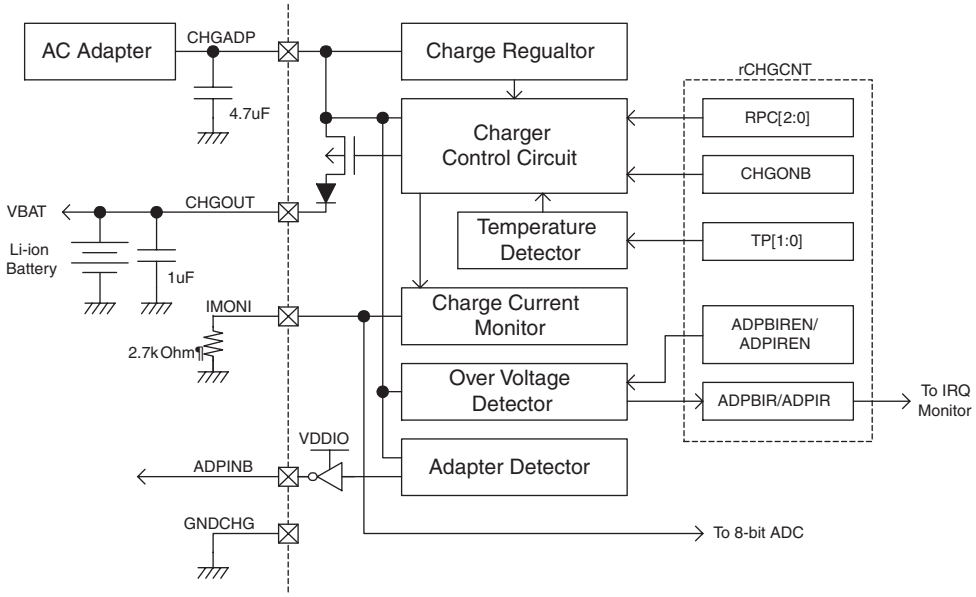


Table 5-22. Pin Description

Pin Name	Function	Level
CHGADP	Power input pin for charger block (Connected to AC adaptor)	5V
CHGOUT	Charge output pin (Connected to battery)	VBAT
IMONI	Charge current monitor output (Pull-down with external 2.7 kOhm resistor)	
ADPINB	AC adaptor insertion detection output (Output “L” when AC adaptor inserted.)	VDDIO

5.5.3 Li-ion Battery Charger Operation

When AC Adapter is connected, charge is asserted from charge off state. See (1) in Figure 5-15 on page 35.

5.5.3.1 Charge OFF Mode

At Charge OFF state, charge is disabled and charge current is 0mA. And, the power-on signal from charger block (chgpon) is “L”. AT73C206 moves to Trickle Charge mode if:

V_{CHGADP} > 4.6V and V_{CHGADP} 5.9V and CHGONB bit = “0"

See (2) in Figure 5-15 on page 35.

5.5.3.2 Trickle Charge Mode

Perform the Trickle Charge with 10% of the Rapid Charge current, which is register-programmable. The power-on signal from charger block (chgpon) is “L”. AT73C206 moves to Rapid Charge 1 Mode with Soft-start if:

V_{CHGOUT} > 2.7V

See (3) in Figure 5-15 on page 35.

5.5.3.3 Rapid Charge 1 Mode

Rapid Charge 1 current is register-programmable. The power-on signal from charger block (chgpon) becomes “H”. AT73C206 moves to Trickle Charge mode with Soft-stop if:

V_{CHGOUT} 2.6V

See (4) in Figure 5-15 on page 35.

Also, over-temperature is detected by chip temperature detector, AT73C206 moves to Rapid Charge 2 with Soft-stop.

See (5) in Figure 5-15 on page 35.

5.5.3.4 Rapid Charge 2 Mode

Perform the Rapid Charge 2 with 20% of Rapid Charge 1 current, which is register-programmable. The power-on signal from charger block (chgpon) is “H”. When chip temperature falls, the charge current returns back to Rapid Charge Mode 1 with Soft-start.

See (6) in Figure 5-15 on page 35.

5.5.3.5 Any state

AT73C206 moves to Charge OFF mode if:

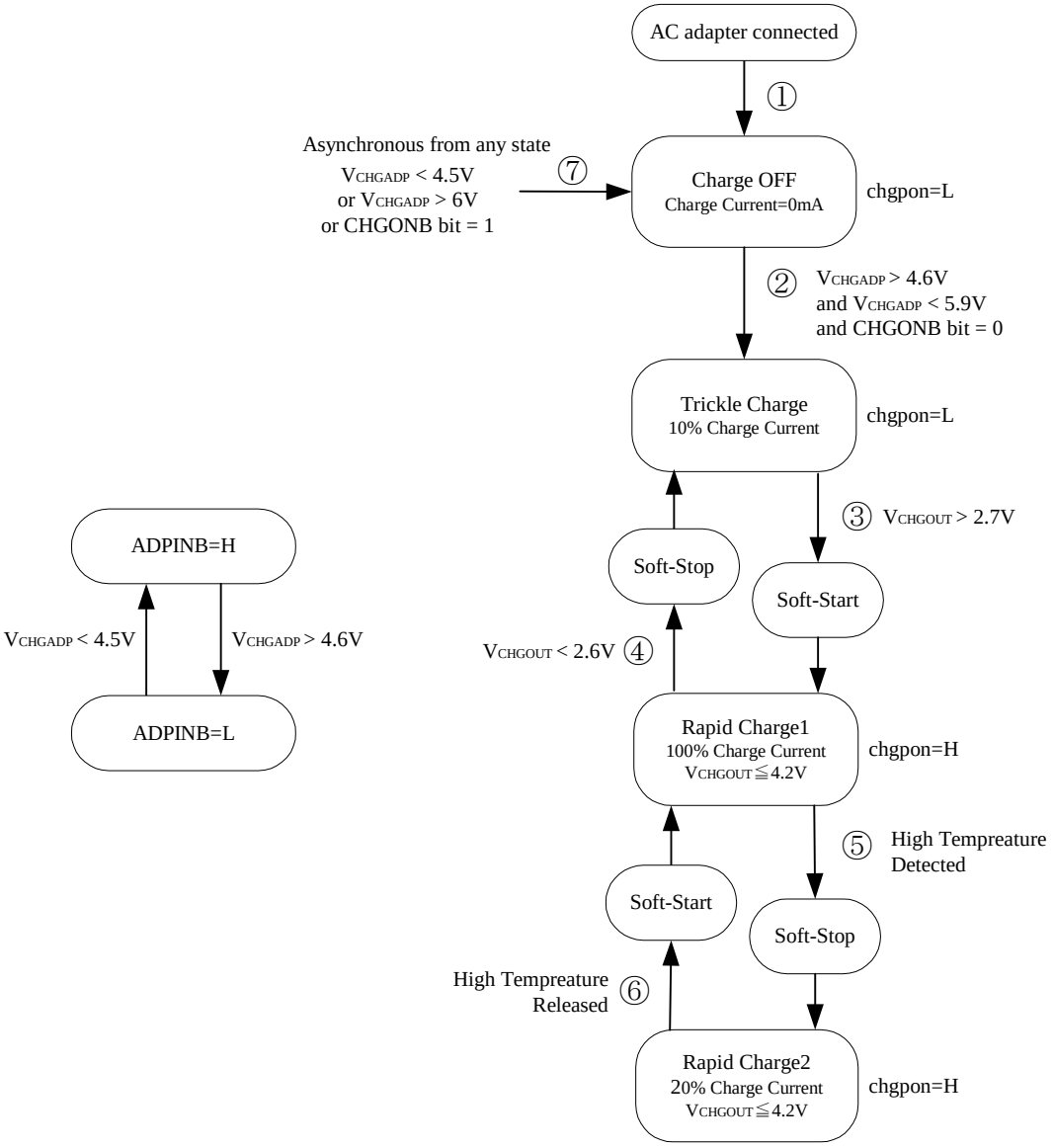
V_{CHGADP} < 4.5V or V_{CHGADP} >6V or CHGONB bit = “1”

See (7) in Figure 5-15 on page 35.

AT73C206 monitors charge current with ADC and disables charging by writing CHGONB= “1”.

5.5.4 Li-ion Battery Charger State Diagram

Figure 5-15. Li-ion Battery Charger State Diagram



5.5.5 Li-ion Battery Charger Chip Temperature Detection

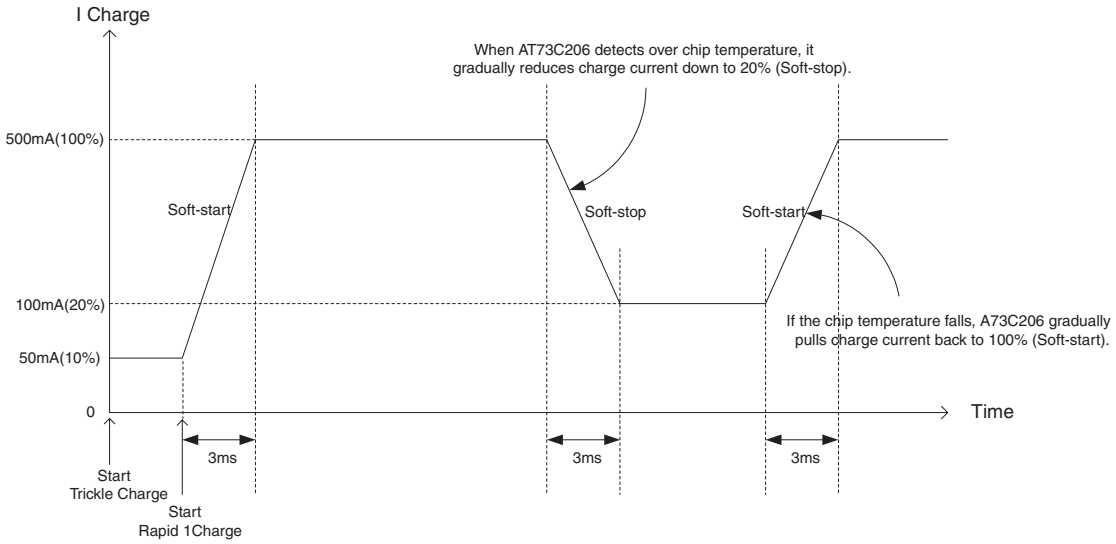
When Rapid Charge 1, if chip temperature approaches the die temperature, which is user selectable by register TP [1:0], AT73C206 reduces charge current to 20% of Rapid Charge 1 current. (Rapid Charge 2)

When chip temperature falls, the charge current returns back to its full current. By repeating this process, AT73C206 is able to keep itself in temperature regulation. This feature not only pro-

tects AT73C206 from overheating, but also allows higher charge current without risking damage to the system.

Soft-start/stop is used to minimize in-rush current on battery.

Figure 5-16. Chip Temperature Detection and Soft-start/stop



5.5.6 Li-ion Battery Charger Electrical Characteristics

Operating Conditions (unless otherwise specified): VIN= 3.6V, T_a = 25° C, CHGOUT=1uF.

Table 5-23. Li-ion Battery Charger Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CHGADP}	AC adapter Operation Voltage		4.5		6.3	V
AV_{DET}	AC adapter Detection Voltage	V_{CHGADP} rising		4.6		V
		hysteresis		0.1		
AV_{OVLO}	AC Adapter Over Voltage Lock-Out	V_{CHGADP} rising		6		V
		hysteresis		0.1		
CI_{SS}	Consumption Current	Rapid Charge = 500mA		3		mA
		Charge OFF			1	
V_{CHG}	Battery Charge Voltage	I_{CHGOUT} = 0, T_a = 0 to 85° C		4.2		V
R_{IMONI}	IMONI Resistor			2.7		kΩ
V_{IMONI}	Charge Current Monitor Output	R_{IMONI}=2.7kΩ, I_{CHGOUT} = 850mA		2.295		V

Table 5-23. Li-ion Battery Charger Electrical Characteristics

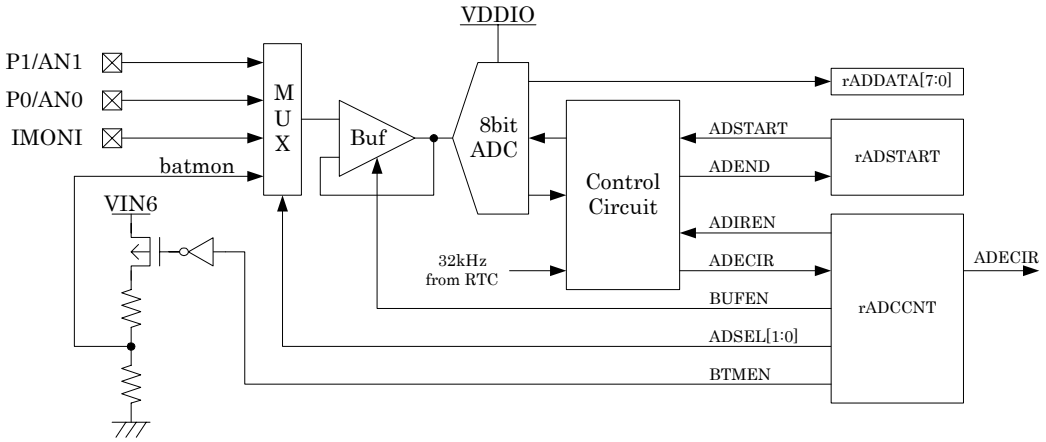
CI_{Rapid}	Rapid Charge Current		-12%	500 550 600 650 700 750 800 850	+12%	mA
$CI_{Trickle}$	Trickle Charge Current	V_{CHGOUT} =2.2V, T_a = 0 to 85° C Percentage of CI_{Rapid}	5	10	15	%
CT_{th}	Chip Temperature Detection Threshold			95 105 115 135		
CV_T	Transition Voltage to Rapid Charge 1 Mode	V_{CHGOUT}, rising		2.7		V
		hysteresis		0.1		

5.6 A/D Converter

The AT73C206 has an 8-bit A/D converter with 4 channels.

- Input is selectable by register set: External pins AN0 & AN1 (Common use with P0 and P1 pins of GPIO), battery voltage monitor (batmon) and charge current monitor (IMONI).
- Input voltage ranges from 0V to VDDIO.
- Generates the clock using RTC 32KHz
- Starts conversion by register set and inform the end of conversion to CPU through ADCECIR.
- The Resistive Voltage Divider for battery voltage monitor is on/off controllable by register.
- Buffer is on/off controllable by register.

Figure 5-17. ADC Block Diagram



5.6.1 Explanation of Operation

Writing “1” in ADSTART bit starts conversion. ADSTART bit will be automatically cleared after conversion starts. After the conversion is completed, AT73C206 sets ADEND bit and notices completion of conversion to CPU through IRQB. The ADEND bit will be cleared by reading the converted data or by writing “1” in ADSTART bit. And ADCECIR is cleared by writing “0”. For re-conversion, write “1” in ADSTART bit.

Changing ADSEL is prohibited during AD Conversion.

Figure 5-18. ADC Timing Diagram

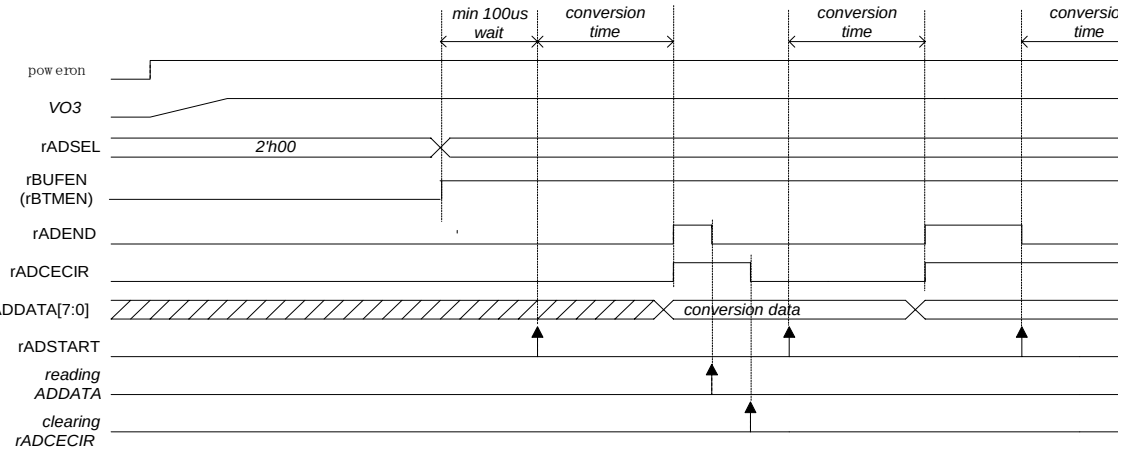
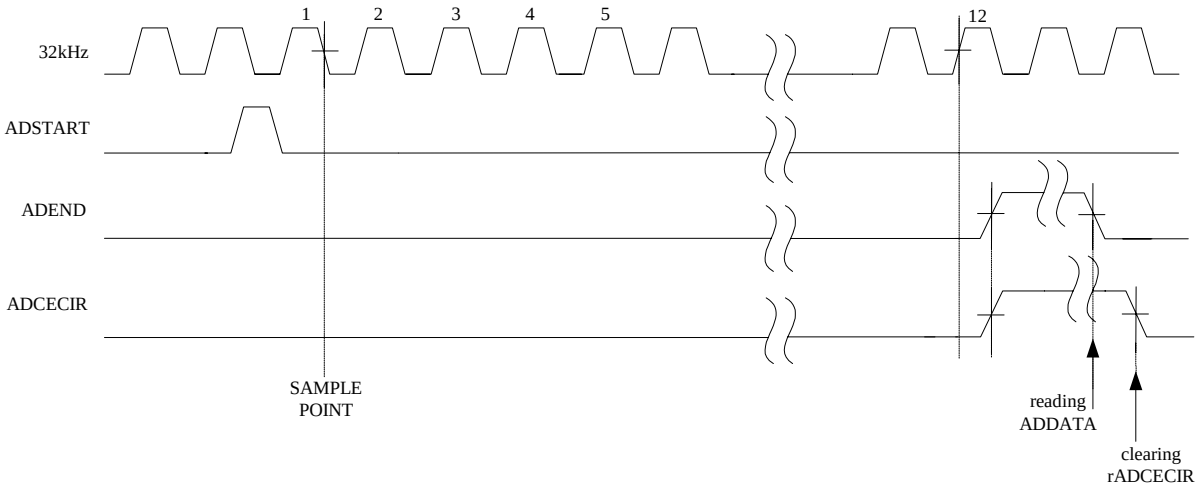


Figure 5-19. ADC Internal Operation Sequence



5.6.2 Electrical Specification

5.6.2.1 A/D Converter

Operating Conditions (unless otherwise specified) VDDIO=2.5V or 2.8V or 3.0V, T_a = 25° C.

Table 5-24. A/D Converter Electrical Characteristics

Symbol	Item	Condition	Min	Typ	Max	Units
A/D Converter						
ADBIT	Resolution				8	bits
INLE	Integral nonlinearity error	AN(0,1) = 0 to VDDIO-0.1V	-1		1	LSB
DNLE	Differential nonlinearity error	AN(0,1) = 0 to VDDIO-0.1V	-1		1	LSB
	Input voltage range		0		VDDIO	V
	Conversion time			397		us

Table 5-24. A/D Converter Electrical Characteristics

ISS	Supply Current	While Converting		1		mA
		Sleeping (Note)			1	uA
Buffer						
ISS	Supply Current	BUFEN=1		250		uA
		BUFEN=0			1	uA
Battery monitor						
Ratio	Resistive voltage divider ratio			0.5		Times
Rdiv	Resistive voltage divider			2		M

Note: After conversion, A/D converter shifts to sleep mode automatically.

5.7 Real Time Clock

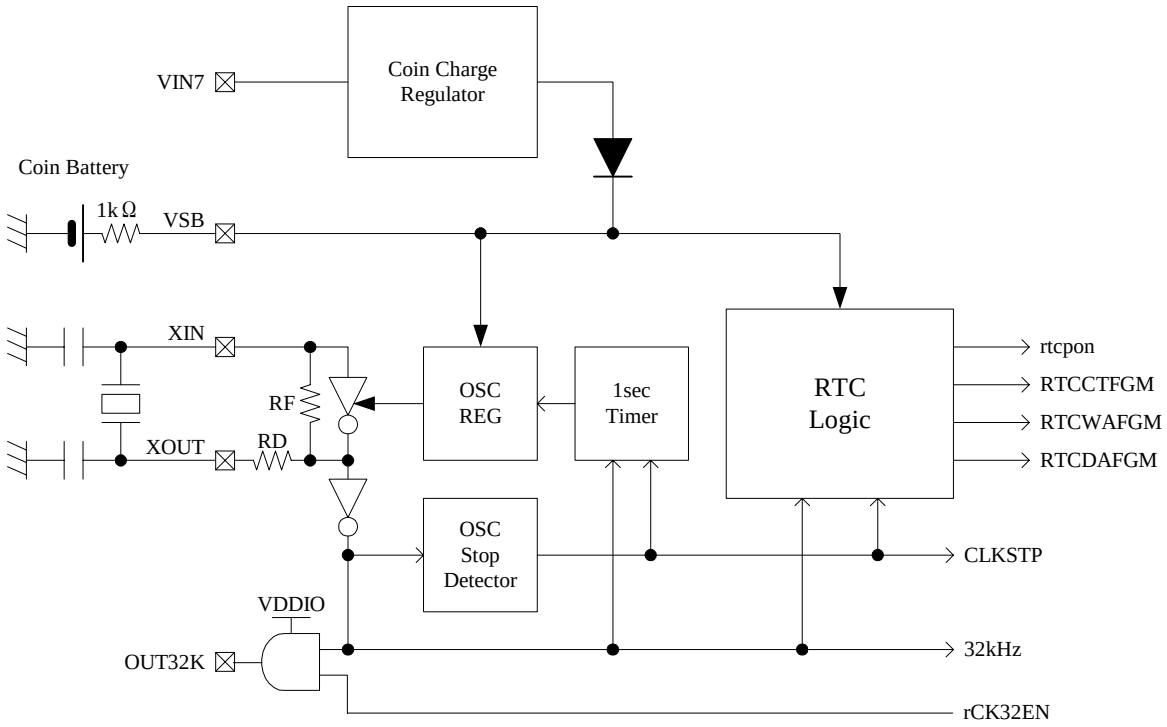
The Real Time Clock provides the coin charge regulator and 2 system of alarm function, which generate an interrupt on a set time. The accuracy of clock is dependant on the Clock Error Offset circuit. Real Time Clock operates with 32.768 kHz of external X'tal and capacitor.

5.7.1 Features

- Coin charge regulator built in with Reverse-current protection diode
- Counters for Clock and Calendar
- Alarm function
  - Combination of day of the week, hour and minute
  - Combination of hour and minute only
- Provides 32.768 kHz clock output
- Power-on flag, which recognizes that a power supplier turns on from 0V
- Automatic definition for leap year is 2099, 12-hour or 24-hour format selectable
- High-accuracy of clock error offset circuit function
- Alarm Interrupts power on AT73C206

5.7.2 Block Diagram

Figure 5-20. RTC Block Diagram



5.7.3 Power Supply and Charge of External Coin Battery

When battery voltage over monitoring voltage

The external coin battery performs charge with the regulated voltage applied from battery and, at the same time, this power is supplied to Real Time Clock.

5.7.4 Function of Real Time Clock

1. Clock Function

The clock and calendar in term of seconds, minutes, hours, day, month and below 2-digit-year are readable and writable via CPU. A low-order 2-digit-year that can be divided by 4 is defined as leap year. AT73C206 provides an automatic definition of leap year until 2099.

2. Alarm function

AT73C206 provides an alarm function, which generates interrupt signal for CPU on a programmed time. There are 2 types of alarm; Alarm_W and Alarm_D. Alarm_W can program a minute, hour and day of the week. Single and multiple day of the week are also programmable. However, Alarm_D is minute and hour programmable. These two alarms are output from IRQB pins. The CPU is allowed to check the status of each alarm by reading the corresponding register.

3. High-accuracy clock error offset circuit function

Oscillator circuit is configured by connecting an external X'tal and capacitors (CG & CD). For accuracy of the clock, AT73C206 has the internal Clock Error Offset circuit which keeps the clock precise by compensating the oscillator frequency drift with about 3 ppm (or about 1 ppm) step in range of ±189 ppm (or about ±63 ppm).

(Error ±1.5 ppm (or ±0.5 ppm) at 25° C after the compensation.)

The compensation of frequency in each system;

- Enables high-accuracy of clock by using the X'tal which covers wide fluctuation.
- Compensates a season-frequency-drift by correcting the clock error every season.
- Enables high-accuracy of clock by correcting the clock error according to the temperature fluctuation.

  (This function is available only for the system with temperature detection function.)

4. Constant cycle interrupt generation function

In addition to alarm function, constant cycle interrupt is output through IRQB pin. The cycle is selectable from 2 Hz (1 time/0.5 sec.), 1 Hz (1 time/1sec.), 1/60 Hz (minute), 1/3600 Hz (hour) and month (first day of each month). There are two types of output waveforms selectable in constant cycle; one is the waveform (2 Hz, 1 Hz) on normal pulse and the other is the one (every second, minute, hour and month), which is designed considering a CPU interrupt and a level interrupt. The status of register pin can be checked.

5. 32768 Hz clock output

Oscillator frequency clock of X'tal units can be output through an OUT32K pin. The enable/disable of clock output is controllable by the CK32EN bit.

6. Power-on reset and Oscillator stop detection function

   a. Power-on reset function (PON Flag)

   When the VSB Power-supply pin rises from 0V, AT73C206 resets the control register and, simultaneously, allows CPU informed it by issuing flag. This feature allows CPU to judge whether VSB Power-supply pin has raised from 0V or it has been power-supplied by battery.

b. Oscillator stop detection function (OSC stop detector)

AT73C206 has a register, which remembers on/off of oscillator. This feature allows CPU judge whether oscillation has stopped.

OSC stop detector generates interrupt when it detects that the clock stops. Enabling/disabling of the interrupt is selectable by STPIREN bit in CLKCNT register. Also, the output of the OSC stop detector can be read from the Status Monitor register.

5.7.5 Electrical Specification

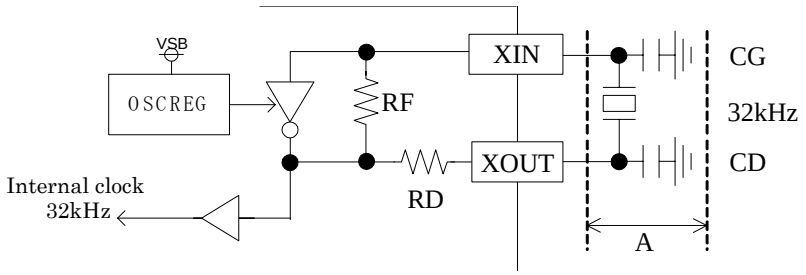
Operating Conditions (unless otherwise specified): VIN = 3.6V, T_a = 25° C.

Table 5-25. RTC Electrical Characteristics

Symbol	Parameter	Condition	Min.	TYP.	Max	Unit
COIN CHARGE REGULATOR						
CCROUT	VSB Output Voltage	VIN7=3.1 to 4.2V Iout=0uA	2.943	3.050	3.157	V
Vf	Diode Forward Voltage	Iout = 1mA		0.75		V
RTC						
VSBV	Oscillator Operating Voltage	VIN7=OPEN	1.3	3.0		V
Tosc	Oscillation Start Time				1	s
OSCtor	Oscillation Tolerance		5			times
ISS	Supply Current			1.5		uA

5.7.6 Structure of Oscillation Circuit

Figure 5-21. Structure of Oscillation Circuit



Note: Recommended external device:
X'tal: FC-135 (EPSON®), (f: 32.768 kHz), (R =70kΩmax), CL = 9 pF
CG, CD: 12 pF typ

Note: Standard of Internal device:
RF: 20MΩtyp
RD: 100kΩtyp

Note: Oscillation circuit operates in internal voltage regulator.

Note: X'tal units: For X'tal units, use FC-135 (CL=9pF) of EPSON. Check with the manufacturer about the value of crystal units in use.

Note: Notes on mounting:

Place the crystal units as close as possible to the IC.

Do not place signal/power supply lines near the oscillation circuit.

Make the insulation resistance between XIN/XOUT pins and PCB board as high as possible.

Do not wire XIN and XOUT in a long parallel line.

Condensation may stop the crystal oscillation or cause other errors.

Note: External input of clock (32.768 kHz) to XIN

Note: DC binding: Forbidden due to the inconsistency with input level.

Note: AC binding: Possible. However, oscillation stop detection is not assured, for error detection may occur due to the noise and other effects.

Note: Do not operate other IC with oscillation output (XOUT output) in order to protect the stability of oscillation characteristics.

5.8 Audio/Voice

5.8.1 Features

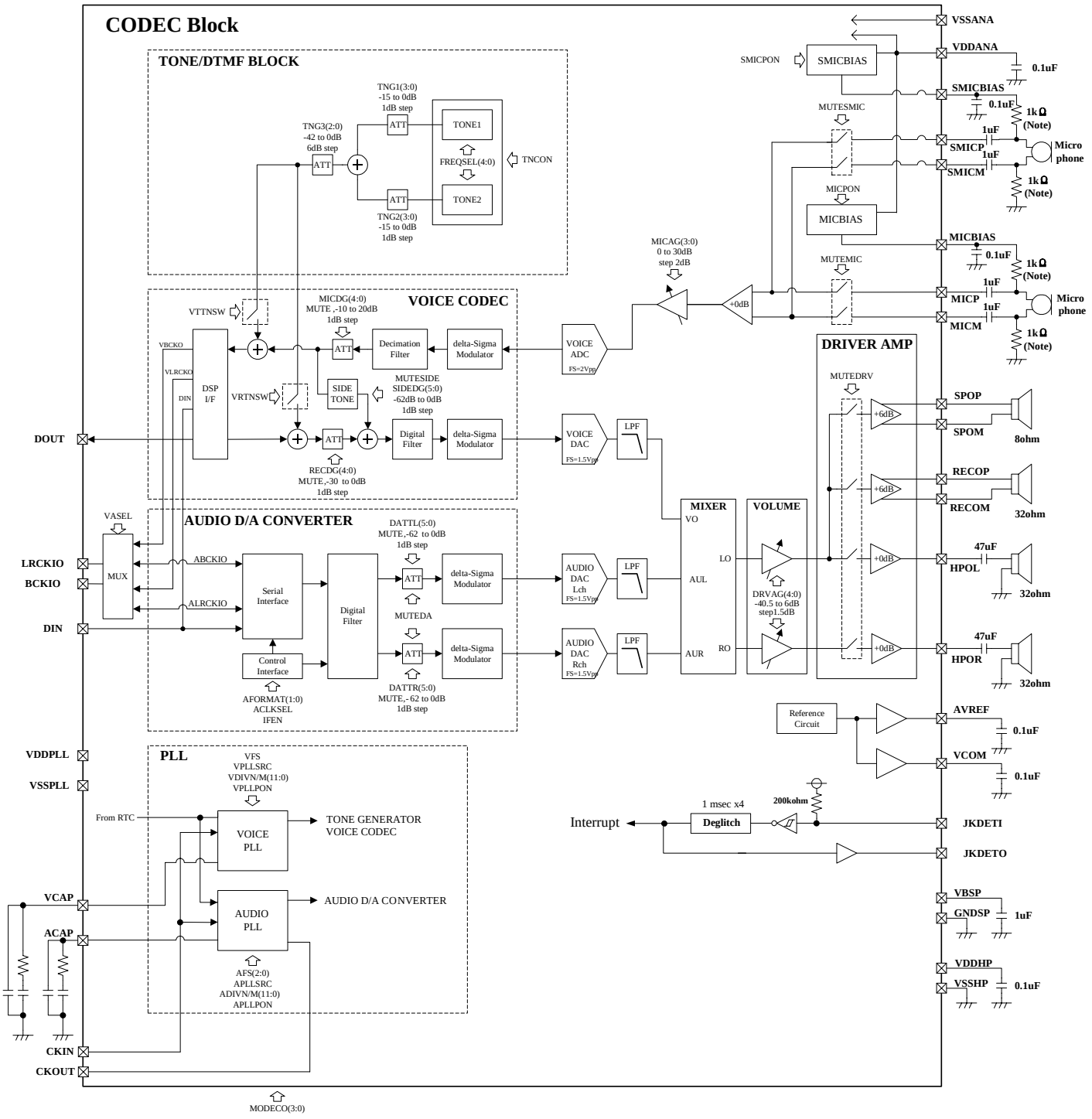
- Voice CODEC: 16-bit Linear CODEC (Sampling frequency: 8 kHz and 16 kHz)
- Audio DAC: 16-bit Linear Stereo DAC (Sampling frequency: 48 kHz to 8 kHz)
- Tone generator: Supports 16 DTMF tones
- Mono MIC amplifier: Differential amplifier
- Stereo headphone amplifier: 22 mW (32 Ohm load,THD+N=0.5%)
- Mono receiver amplifier: 60 mW (32 Ohm BTL load,THD+N=1%)
- Mono speaker amplifier: 300 mW (8 Ohm BTL load,THD+N=1%)
- Microphone bias supply: Output Voltage=2.2V
- PLL: Reference clock=32.768 kHz
- Jack detect: Input 200 kOhm pull-up

5.8.2 Block Diagram

Power supply

- Digital: 2.8V (VDD)
- Analog: 2.8V(VDDANA)
- Speaker Amplifier: 3.6V[Battery Voltage level] (VBSP)
- Receiver Amplifier: 2.8V (VDDHP)
- Headphone Amplifier: 2.8V (VDDHP)
- PLL: 2.8V (VDDPLL)

Figure 5-22. CODEC Block Diagram



Note: The value of resistance must be determined depending on the specification of the microphone which is used. When power analog CODEC (VDDANA), it is also required to supply power to digital CODEC (VDD).

5.8.3 Voice Codec

- 16-bit Linear CODEC
- Sampling frequency: 8 kHz and 16 kHz
- Interface: IIS
- Data format: Linear
- Transmit channel: 1ch
- Inputs: 2ch (MICP/MICM, SMICP/SMICM)
- Outputs: Receiver, Stereo Headphone, Speaker
- Internal Tone generator: DTMF/Single Tone
- Mode: Master
- Level Diagram: Analog Input=2.0Vpp -> DOUT Output=3.17dBm0
  DIN Input=0dBFS -> Analog Output=1.5Vpp
- TONE DATA MIX Function: Mix of TONE DATA and VOICE DATA is controlled by register set
- Attenuator: TX System: MUTE, -10dB to 20dB / 1dB step
  RX System: MUTE, -30dB to 0dB / 1dB step
- SIDE TONE: Loop-back of TX side to RX side (MUTE,-62dB to 0dB)
- Smoothing Gain control: Gain changes to the current set value by Smoothing Gain control at 1dB/fs
  - Available in TX System, RX System and SIDE TONE

5.8.4 Audio DAC

- DAC: 16-bit Linear Stereo DAC
- Sampling frequency: 48 kHz, 44.1 kHz, 32 kHz, 24 kHz, 22.05 kHz, 16 kHz, 11.025 kHz, 8 kHz
- Interface Data format: IIS, LJF, RJF
- Interface Mode: Master and Slave
- Level Diagram: DIN Input=3.17dBm0 -> Analog Output=1.5Vpp
- Outputs: Receiver, Stereo Headphone, Speaker
- Attenuator: MUTE,-62dB to 0dB / 1dB step
- Smoothing Gain control: Gain changes to the current set value by Smoothing Gain control at 1dB/fs
- Available in Lch and Rch

5.8.5 Tone Generator

- 16 DTMF tones: DTMF Low tone is 697,770, 852 or 941Hz.
  - DTMF High tone is 1209,1336, 1477 or 1633Hz.
- 2 programmable tones: From 0Hz to 3992.1875Hz
  - Frequency of programmable tone1/2 = 7.8125Hz x PTN1/2 can be generated independently
- Software start: Writing the register (TNCON bit) via SPI starts tone generating
- Hardware stop: Internal programmable hardware timer stops tone generating. The range of the time is from 80ms to 200ms (default 100ms)

- Gain Control: Gains of TONE1 and TONE2 in Tone generator are individually settable. After mixing TONE1 and TONE2, the gain of TONE3 is settable.

5.8.6 Analog Control

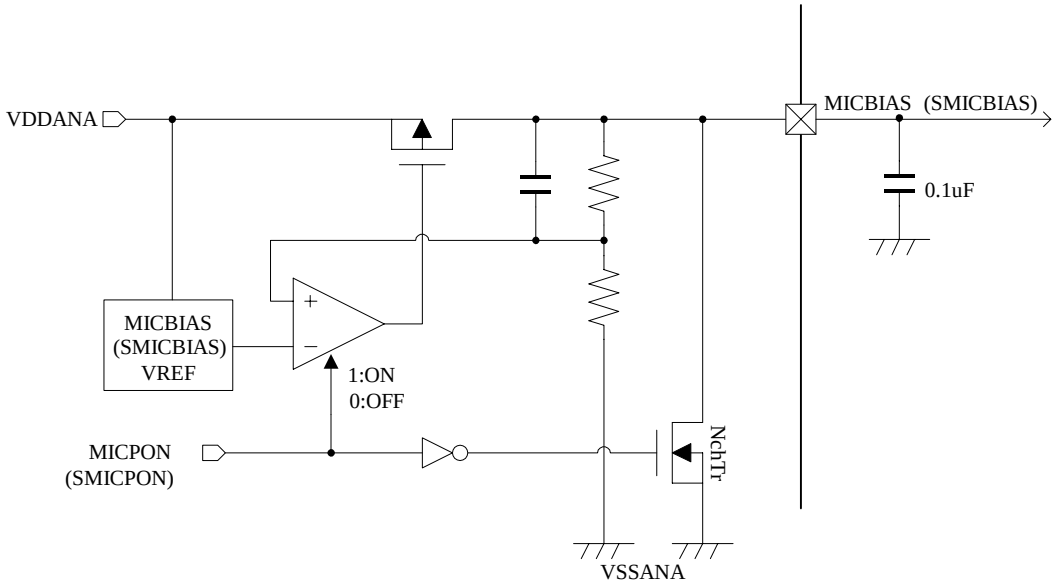
- Mode Control: Driver AMP (Receiver AMP/ Speaker AMP/ Headphone AMP)
  - Power-down / Stand-by
  - Mono/ Stereo
- Mute Control: MICAMP, SMICAMP Mute
  - DRIVER amplifier Mute
- Gain Control: MIC-Gain: 0 to 30dB/ Step 2dB

  Driver-Gain –40.5 to 6dB/ Step 1.5dB

5.8.7 MICBIAS, SMICBIAS

MICBIAS and SMICBIAS consist of Power supply, Error amplifier, Driver transistor and Resistor set for output voltage setting. ON/OFF of MICBIAS and SMICBIAS is controllable by register set. The regulator has an internal sink transistor.

Figure 5-23. MICBIAS, SMICBIAS



5.8.8 PLL

There are two types of PLL: PLL for Voice CODEC and PLL for Audio DAC. It provides the clock corresponding to the register-set sampling frequency by regulating the reference clock.Power down control of PLL for Voice CODEC and PLL for Audio DAC can be operated independently.

When Power down control of PLL for Voice is set, Digital Voice codec block also goes to power-down mode.

When Power down control of PLL for Audio is set, Digital Audio DAC block also goes power-down mode.

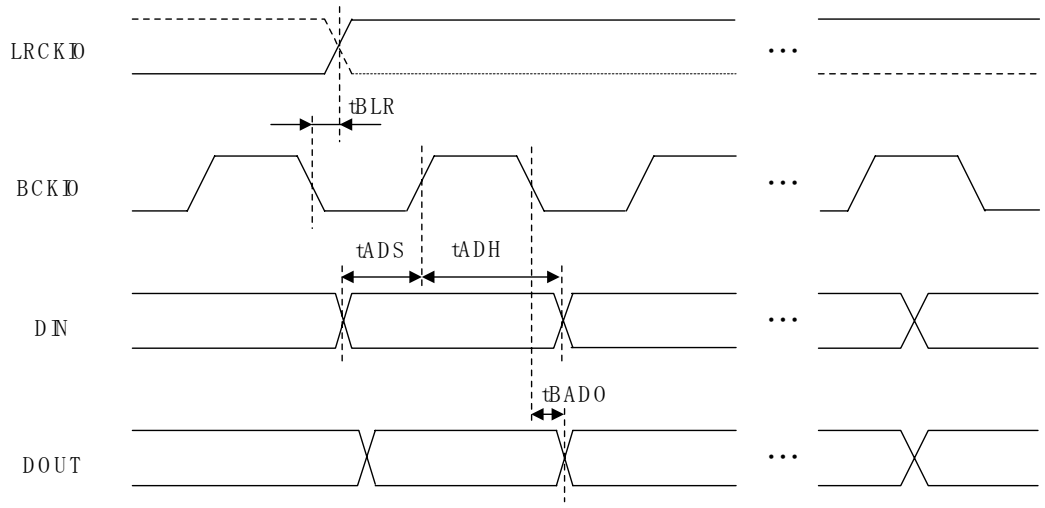
5.8.9 Jack Detector

AT73C206 integrates an input port (with 200 kOhm of pull-up resistor) and an output port for detecting headset insertion. The detection signal will be output through the output port after perform chattering rejection (1ms x 4). When the insertion/removal of the headset jack is detected, AT73C206 will generate an interrupt. Permit/prohibit of the interrupt is controllable by register.

5.8.10 Interface Timing Data Format

5.8.10.1 Voice Interface Timing

Figure 5-24. Voice Interface Timing



Operating Conditions (unless otherwise specified): VDD=2.8V, T_a = 25° C, fs:16 kHz, 8 kHz

Table 5-26. Voice Interface Electrical Characteristics

Parameter		Condition	Min	Typ	Max	Unit
BCKIO Frequency	tBCLK			32* fs		kHz
LRCKIO Delay Time	tBLR	BCKIO falling	-10		100	ns
DIN Setup Time	tADS	BCKIO rising	50			ns
DIN Hold Time	tADH	BCKIO rising	50			ns
DOUT Delay Time	tBADO	BCKIO falling	-		50	ns

Note: fs: 16kHz, 8kHz

5.8.10.2 Voice Interface Data Format

Linear<TX 16bit_Linear/ RX 16bit_Linear >

Figure 5-25. Voice Interface Data Format: IIS Format

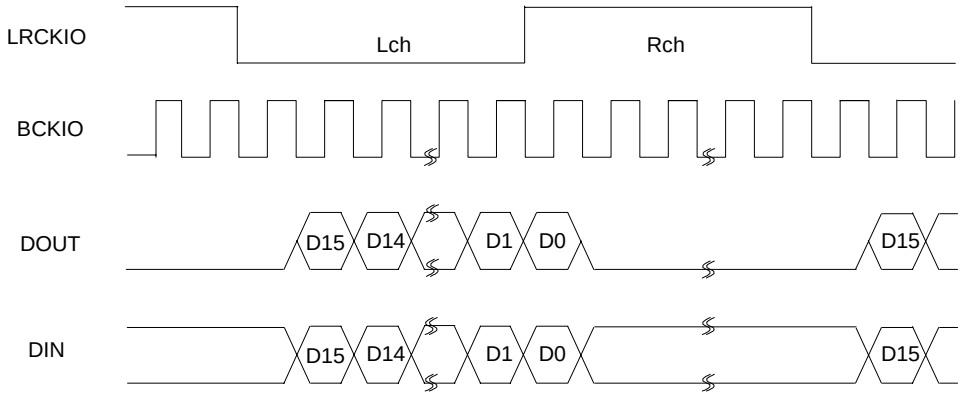
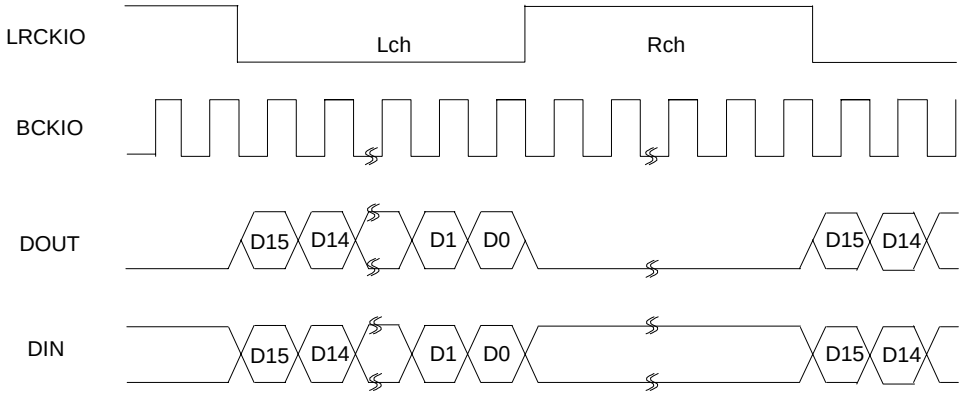
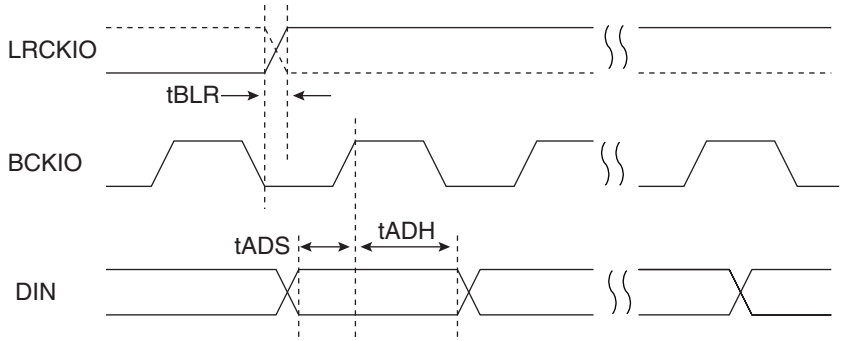


Figure 5-26. Voice Interface Data Format: Left justify Format



5.8.10.3 *Audio Interface Timing - Slave and Master Modes*

Figure 5-27. Audio Interface Timing (Slave mode)



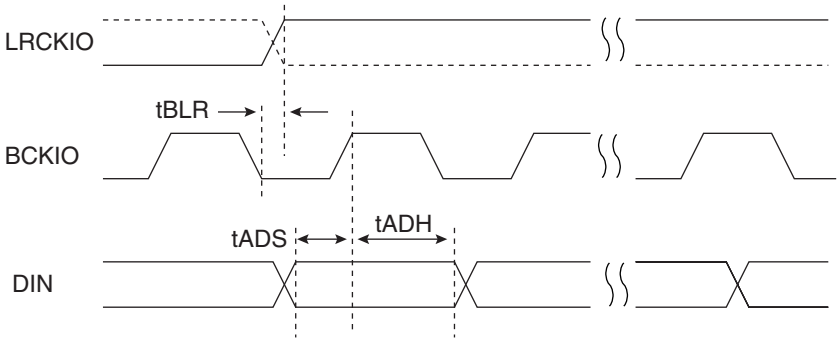
Operating Conditions (unless otherwise specified) VDD =2.8V, T_a = 25° C.

Table 5-27. Audio Interface (Slave mode) Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
BCKIO Frequency	tBCLK		32*fs		64*fs	kHz
LRCLKO Delay Time	tBLR	BCKIO falling	-100		100	ns
DIN Setup Time	tADS	BCKIO rising	50			ns
DIN Hold Time	tADH	BCKIO rising	50			ns

Note: fs: 48 kHz, 44.1 kHz, 32 kHz, 24 kHz, 22.05 kHz, 16 kHz, 11.025 kHz, 8 kHz

Figure 5-28. Audio Interface Timing (Master mode)



Operating Conditions (unless otherwise specified): VDD=2.8V T_a = 25° C.

Table 5-28. Audio Interface (Master mode) Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
BCKIO Frequency	tBCLK			64*fs		kHz
LRCKIO Delay Time	tBLR	BCKIO falling	-10		100	ns
DIN Setup Time	tADS	BCKIO rising	50			ns
DIN Hold Time	tADH	BCKIO rising	50			ns

Note: fs: 48 kHz, 44.1 kHz, 32 kHz, 24 kHz, 22.05 kHz, 16 kHz, 11.025 kHz, 8 kHz

5.8.10.4 Audio Interface Format - IIS, Left Justify, Right Justify

Figure 5-29. Audio Interface Format - IIS

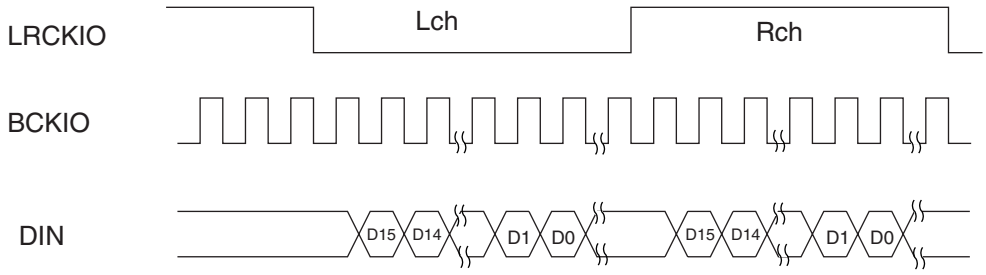


Figure 5-30. Audio Interface Format - Left Justify Format

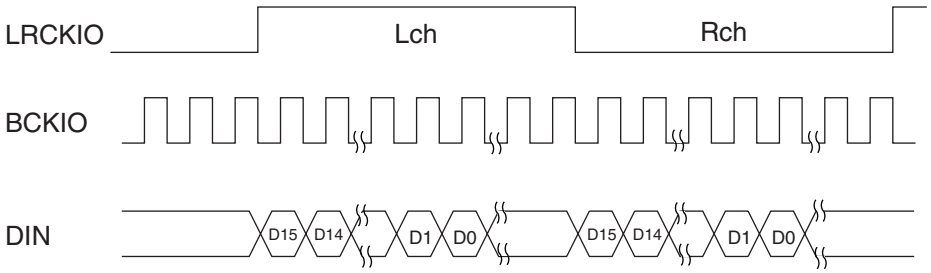
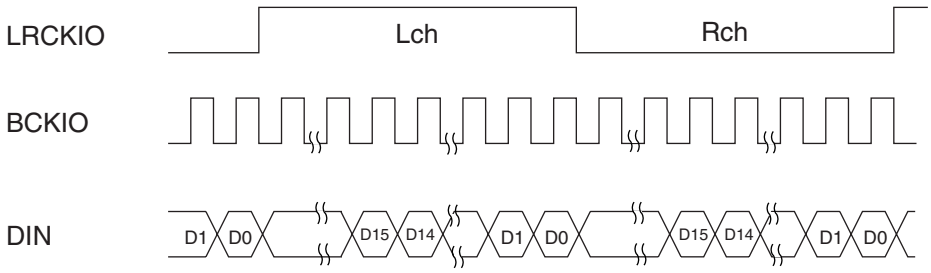


Figure 5-31. Audio Interface Format - Right justify Format



where:

LRCKIO: Audio interface L/R select input/output

BCKIO: Audio interface serial bit clock input/output

DIN: Audio interface serial data input

Note: Input/output mode of LRCKIO and BCKIO pins is controllable by register set. (Slave Mode/Master Mode)

5.8.11 Audio Electrical Characteristics

Operating Conditions (unless otherwise specified): VDD=2.8V, VDDANA = 2.8V, VBSP=3.6V, VDDHP=2.8V, VDDPLL=2.8V, T_a = 25° C.

Table 5-29. Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units	Comment
Digital Power Supply Current	Audio playback mode, fs=48kHz		12	15	mA	
Analog Power Supply Quiescent Current	No Load, No Signal		12	15	mA	
Speaker Driver Quiescent Current	No Load, No Signal		3	6	mA	
Digital Power down Current			1.0	5	uA	
Analog Power down Current			0.5	3	uA	
Micamp Input impedance			60		kohm	
Headphone Amplifier Output Power	THD+N = 0.5%, fOUT = 1kHz RL=32 ohm		22		mW	
Mono Receiver Amplifier Output Power	THD+N = 1%, fOUT = 1kHz RL=32 ohm		60		mW	
Mono Speaker Amplifier Output Power	THD+N = 1%, fOUT = 1kHz RL=8ohm		300		mW	
Headphone Amplifier Total Harmonic Distortion + Noise1	fIN = 1kHz, POUT = 16 mW RL=32 ohm Audio DAC path		0.01		%	
Mono Receiver Amplifier Total Harmonic Distortion + Noise	fIN = 1kHz, POUT = 40 mW RL=32 ohm Audio DAC path		0.01		%	
Mono Speaker Amplifier Total Harmonic Distortion + Noise	fIN = 1kHz, POUT = 200 mW RL=8 ohm		0.2		%	
Signal-to-Noise Ratio (Voice Playback Path)	Signal=0dBFS@1 kHz; Noise=digital zero, A-weighted; 0dB gain setting fs = 8KHz		85		dB	
Signal-to-Noise Ratio (Audio Playback Path)	Signal=0dBFS@1 kHz; Stereo Load; Noise=digital zero, A-weighted; 0dB gain setting		90		dB	
Dynamic Range (Voice Playback Path)	Signal=-60dBFS@1 kHz; Stereo Load; A-weighted; 0dB gain setting fs = 8 kHz		85		dB	
Dynamic Range (Audio Playback Path)	Signal=-60dBFS@1 kHz; Stereo Load; A-weighted; 0dB gain setting fs = 44.1kHz		90		dB	

Table 5-29. Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units	Comment
Signal-to-Noise Ratio (Voice ADC Path)	Reference signal = 0dBFS; MICP, MICM terminated with 2uF to ground; 20 dB MICAMP gain setting fs = 8 kHz		75		dB	
Dynamic Range (Voice ADC Path)	MICP, MICM terminated with Signal=-60dBFS@1 kHz 0dB MIC preamp gain setting fs = 8 kHz		75		dB	
Stereo Channel-to-Channel Crosstalk	fS=44.1 kHz, fIN=1 kHz sine wave at –3dBFS		-75		dB	
Maximum Voltage Differential MIC Input Voltage	0dB MIC Preamp gain setting		2		VP-P	
MICBIAS Output Voltage	10uA ⊴IOUT ⊴IOUTmax	2.1	2.2	2.3	V	

Note: Conditions of Dynamic Range: +60dB SINAD at –60dB FS digital input.

5.8.11.1 Voice ADC CODEC Electrical Characteristics

Operating Conditions (unless otherwise specified) VDD=2.8V, VDDANA = 2.8V, VBSP=3.6V, VDDHP=2.8V, VDDPLL=2.8V, T_a = 25° C.

Table 5-30. Voice ADC Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit	Comment
Absolute Gain	0dBm0@1020Hz, Gain=0dB	-1		1	dB	
Gain Tracking	-10dBm0@1020Hz					
	3dBm0 to 40dBm0	-0.3		0.3	dB	
	-40dBm0 to 55dBm0	-0.5		0.5	dB	
S/N 8kHz: C-Message	1020Hz, Analog Gain=0dB 3dBm0	73	83		dB	
THD+N BW= C-Message	1020Hz, Analog Gain=0dB					
	3dBm0		-50	-40	dB	
	0dBm0		-50	-40	dB	
	-5dBm0		-60	-50	dB	
	-10dBm0		-60	-50	dB	
	-20dBm0		-50	-40	dB	
	-30dBm0		-45	-35	dB	
	-40dBm0		-40	-30	dB	
Speech Delay			0.5		ms	
Idle Channel Noise8kHz:C-Message	Analog Gain=0dB			-86	dBV	

5.8.11.2 Voice DAC CODEC Electrical Characteristics

Operating Conditions (unless otherwise specified) VDD=2.8V, VDDANA = 2.8V, VBSP=3.6V, VDDHP=2.8V, VDDPLL=2.8V, T_a = 25° C.

Table 5-31. Voice DAC Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit	Comment
Absolute Gain	0dBm0@1020Hz, Gain=0dB	-1		1	dB	
Gain Tracking	-10dBm0@1020Hz, Gain=0dB					
	3dBm0 to 40dBm0	-0.3		0.3	dB	
	-40dBm0 to 55dBm0	-0.5		0.5	dB	
S/N HPOL Output 8kHz: C-Message	1020Hz, Gain=0dB 3dBm0	73	83		dB	
THD+N HPOL Output 8kHz:C-Message	1020Hz, Gain=0dB					
	3dBm0		-60	-50	dB	
	0dBm0		-60	-50	dB	
	-5dBm0		-70	-60	dB	
	-10dBm0		-70	-60	dB	
	-20dBm0		-60	-50	dB	
	-30dBm0		-50	-40	dB	
	-40dBm0		-40	-30	dB	
Speech Delay			0.5		ms	
Idle Channel Noise 8kHz:C-Message	HPOL Output			-90	dBV	

5.8.11.3 Audio DAC Electrical Characteristics

Operating Conditions (unless otherwise specified): VDD=2.8V, VDDANA=2.8V, VBSP=3.6V, VDDHP=2.8V, VDDPLL=2.8V, T_a = 25° C, Gain:0dB, fs =44.1kHz

Table 5-32. Audio DAC Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit	Comment
Absolute Gain	-3dBFS@1020Hz, Gain=0dB	-1		1	dB	
Gain Tracking	-10dBFS@1020Hz					
	0dBFS to 35dBFS	-0.3		0.3	dB	
	-35dBFS to 50dBFS	-0.5		0.5	dB	
S/N	0dBFS@1020Hz	84	90			
	A-Weight				dB	
THD+N	Gain=0dB		-80	-70		
	0dBFS@1020Hz					
	BW=20Hz to 20kHz					
Crosstalk			-75		dB	

Operating Conditions (unless otherwise specified) VDD=2.8V, VDDANA = 2.8V, VBSP=3.6V, VDDHP=2.8V, VDDPLL=2.8V, T_a = 25° C.

Table 5-33. Audio DAC Digital Filter Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit	Comment
Pass Band		0.445			fs	
Pass Band Ripple	0Fs to 0.445 fs	-0.3	0	0.3	dB	
Stop Band			0.555		fs	
Stop Band attenuation	0.555 fs to 1 fs		-50		dB	48/44.1/32kHz
Stop Band attenuation	0.555 fs to 1 fs		-75		dB	24/22.05/16/11.025/8 kHz

5.8.11.4 TONE Generator Electrical Characteristics

Operating Conditions (unless otherwise specified) VDD=2.8V, VDDANA = 2.8V, VBSP=3.6V, VDDHP=2.8V, VDDPLL=2.8V, T_a = 25° C.

Table 5-34. Tone Generator Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit	Comment
Signal Output Level	Gain=0dB Setting		3.17		dBm0	
Frequency Deviation	50Hz to 3.4kHz	-2		2	Hz	
THD+N	HPOL(ToneGain=0dB)			-40	dB	

5.8.11.5 MICBIAS, SMICBIAS Electrical Characteristics

Operating Conditions (unless otherwise specified) VDD=2.8V, VDDANA = 2.8V, VBSP=3.6V, VDDHP=2.8V, VDDPLL=2.8V, Ta = 25° C.

Table 5-35. MIC(SMIC)BIAS Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOUT	Output Voltage	10uA ≤IOUT ≤IOUTmax	2.1	2.2	2.3	V
IOUT	Output Current				1	mA
Iss	Consumption Current on Operation-mode	IOUT=0mA		200		uA
Istnby	Consumption Current on OFF-mode	MICBIAS on OFF-mode		0.01	1	uA
RR	Ripple Rejection Rate	2.8V+0.1Vp-p IOUT=IOUTmax/2=217Hz		65		dB
VOUT/ topt	Output Voltage Temperature Efficiency	-30° C ≤Ta ≤85° C		±100		ppm/
en	Output Noise Level	BW=20Hz to 6.6kHz(with C-Message), IOUT=IOUTmax/2		10		uVrms
tu	Rise Time	Cout=0.1uF, IOUT=IOUTmax, VOUT > 90%			100	us
td	Fall Time	Cout=0.1uF, IOUT=0mA, VOUT < 0.5V			500	us

5.8.12 CLK

Voice PLL generates the clock for Voice block.

Audio PLL generates the clock for Audio block.

5.8.12.1 Block Diagram

Figure 5-32. Clock Block Diagram

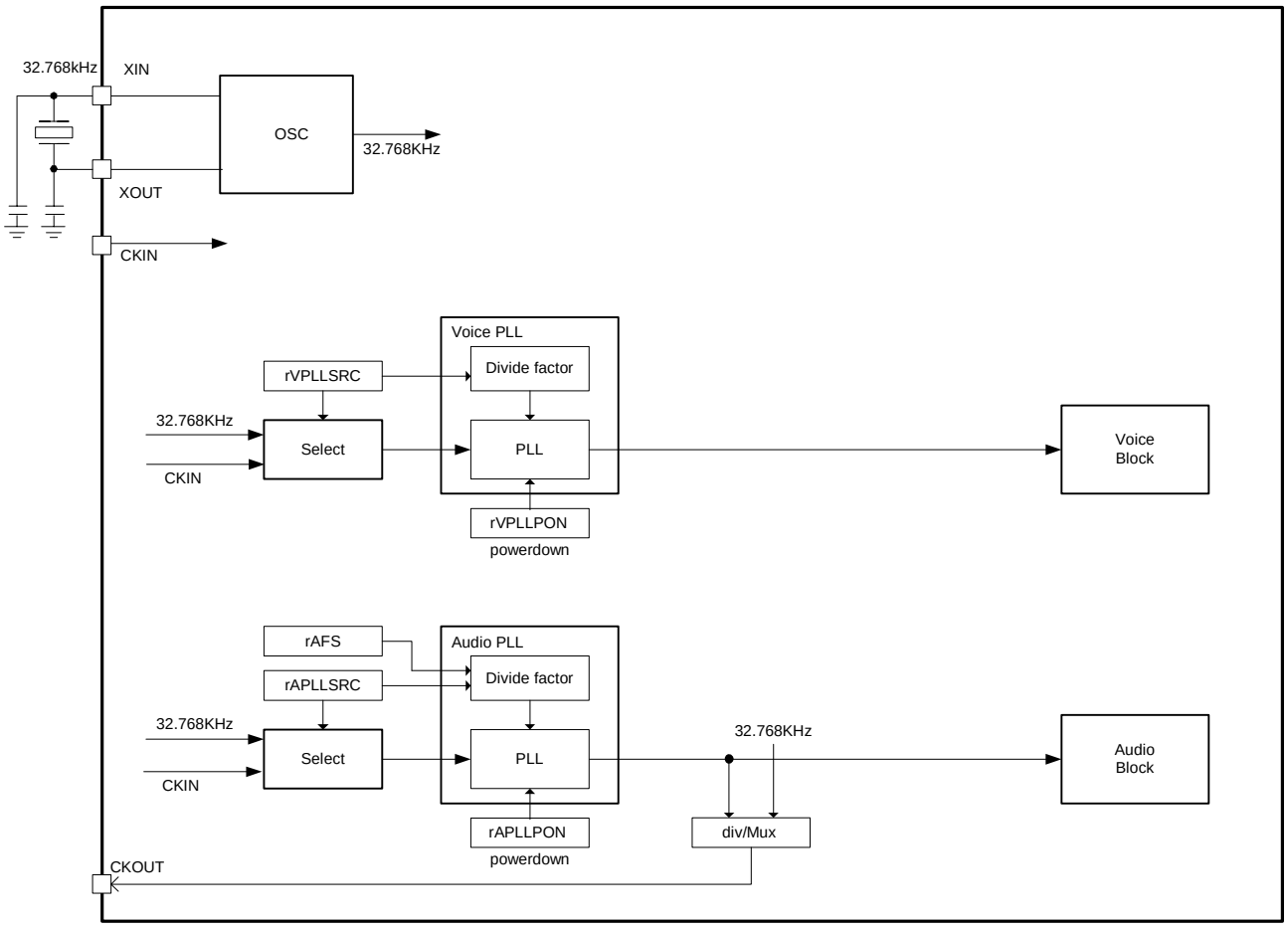
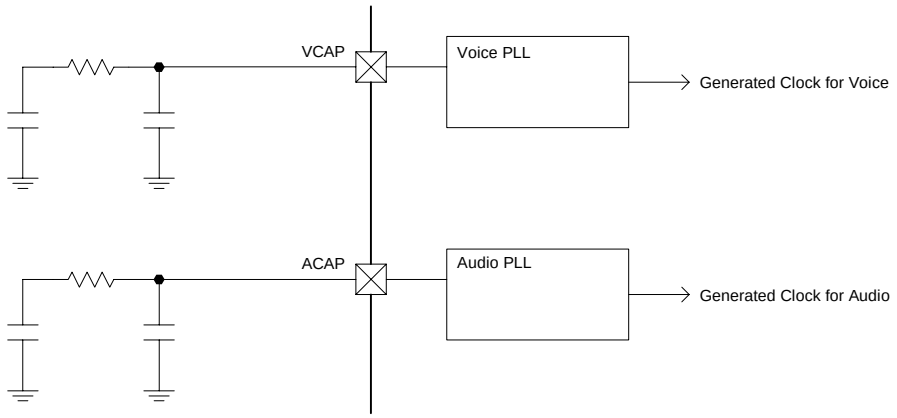


Figure 5-33. PLL Block Diagram



5.8.13 Voice PLL

The internally generated clock frequency for voice PLL should be:

fv=53.248MHz.

If input clock=XIN (When XIN selected, it is automatically multiplied by 1625.)

The internally generated clock fv= 32.768kHz x 1625=53.248MHz.

If input clock = CKIN, the internally generated clock can be calculated by:

$$fv=CKIN \times \frac{MV}{NV} \quad (MV= VDIVM +1, NV=VDIVN+1)$$

Example: If CKIN=26 MHz,

$$fv=26MHz \times \frac{256}{125} = 53.248MHz$$

5.8.14 Audio PLL

The internally generated clock frequency for Audio PLL should be:

$f_A = fs \times 512$

If input clock = XIN (When XIN selected, it is automatically multiplied by AFS bit value).

Table 5-36. Audio PLL (Input clock = XIN)

fs (kHz)	NA	MA	Internally generated f_A(MHz)
48	1	750	24.576
44.1	1	689	22.577152
32	1	500	16.384

Note: MA = ADIVM + 1, NA = ADIVN + 1

If input clock=CKIN (This does not exist in AFS bit.)

$$f_A=CKIN \times \frac{MA}{NA}$$

Example: If CKIN = 26MHz:

Table 5-37. Audio PLL (Input clock = CKIN)

fs (kHz)	NA	MA	Internally generated f_A(MHz)
48	347	328	24.576369
44.1	114	99	22.578947
32	411	259	16.384428

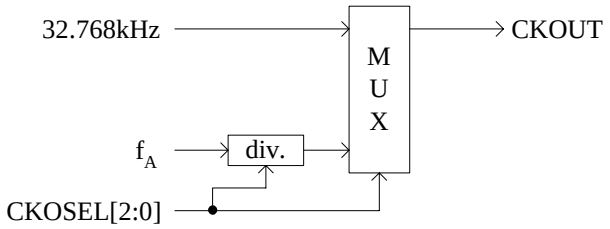
Note: Set each register value considering the relation between the main system clock and Audio codec clock when the Audio codec clock needs to synchronize with the main system clock.

Note: Sampling Rate Setting: When using CKIN for input clock, set NV(NA) at CKIN ÷ NV(NA) > 30 kHz.

5.8.15 Clock Output Function

Each clock can be output through CKOUT pin. The output clock is selectable by CKOSEL bit.

Figure 5-34. Clock Output Diagram



5.8.16 PLL

5.8.16.1 AUDIO PLL/VOICE PLL

Electrical Characteristics: VDDPLL=2.8V, T_a = 25° C.

Table 5-38. PLL Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit	Comment
Input Frequency	CKIN pin	0.1		30	MHz	
	XIN pin		32.768		KHz	
Output jitter	Short term, δ		200		ps	No impact on Audio DAC
Output Duty Cycle		40	50	60	%	No impact on Audio DAC
Lock Time			5	10	ms	
Supply Current (Voice)	Input Clock = 19.2 MHz		1	3	mA	
Supply Current (Audio)	Input Clock = 19.2 MHz		1		mA	

5.9 Keypad LED

KEYLED driver has Nch open-drain type large current output pin. And, the LED ON/OFF is controllable by register set and the brightness is settable by external current control resistor

5.9.1 Block Diagram

Figure 5-35. Keypad LED Driver Block Diagram

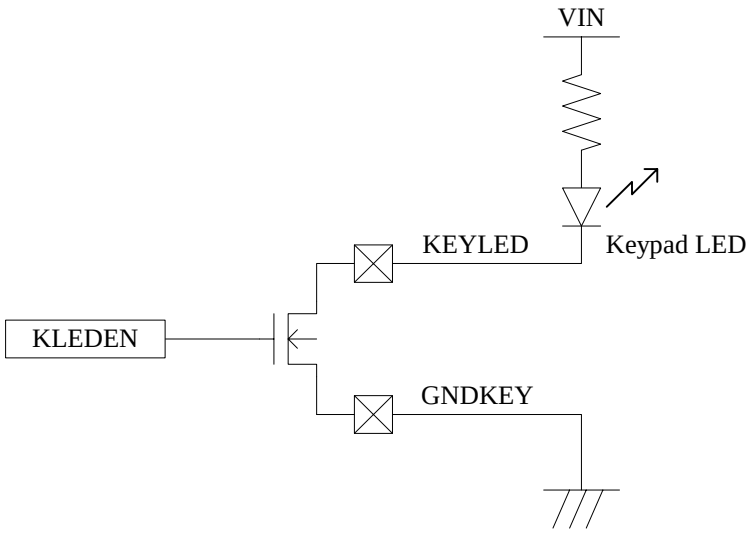


Table 5-39. Keypad LED Driver Pin Description

Pin Name	I/O	Function
KEYLED	O	KEYLED driver
GNDKEY	G	GND only for KEYLED driver

5.9.2 Explanation of Operation

KEYLED ON/OFF is controllable by KLEDEN bit. When KLEDEN bit is “1”, KEYLED is enabled.

5.9.3 Electrical Characteristics

VIN=3.6V, T_a = 25° C.

Table 5-40. Keypad LED Driver Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VOL	Output voltage “L” Level	Iout = -100 mA			0.5	V
IOZ	Output OFF leakage	VIN=04.2V			1	uA

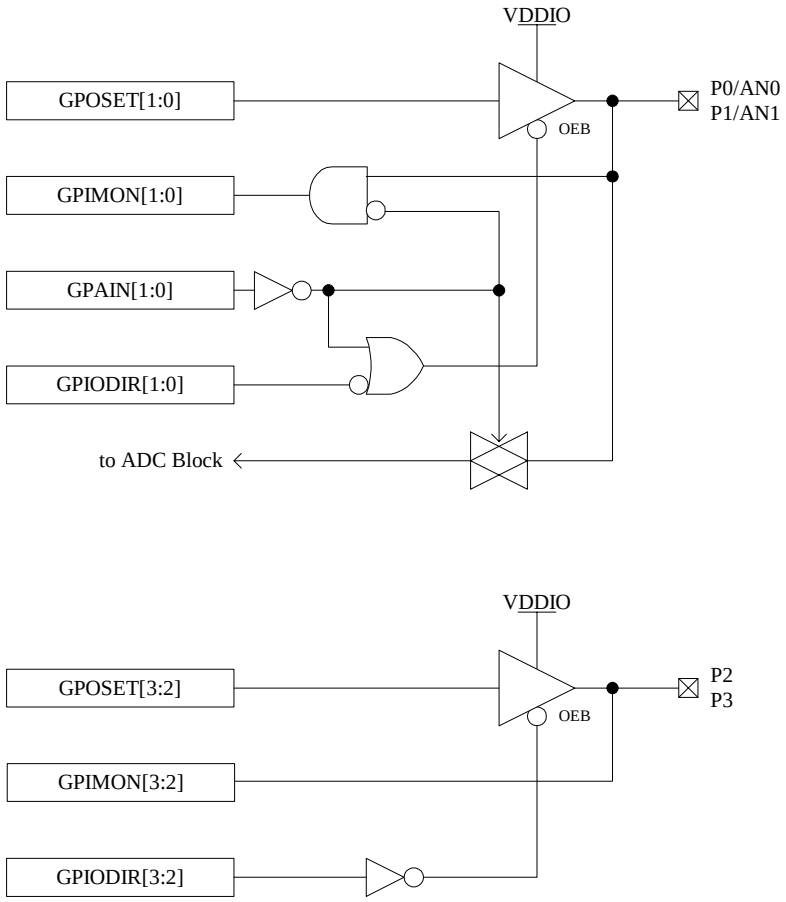
5.10 General Purpose I/O

AT73C206 supports 4-channel GPIO.

All GPIO input/output are controlled by register configure independently.

5.10.1 Block Diagram

Figure 5-36. General Purpose IO Block Diagram



5.10.2 Explanation of Operation

The GPIO has 4-channel I/O function. With pin control, it is possible to control input or output setting of each channel individually. When it is set in output modeGPIODIR= “1”, the output data, which is written in GPOSET register, is output. When it is set in input mode GPIODIR= “0”, the pin level is readable from GPIMON register. I/O voltage varies by VDDIO voltage.

Set GPAIN= “0” when connect analog signal to P0/AN0 and P1/AN1. Then, GPIODIR becomes invalid and GPIO starts operating in analog input mode. And, the GPIMONI will be set to “0”.

Table 5-41. GPIO Truth Table

Setting Register				Reading Register
GPAIN	**GPIODIR**	**GPOSET**	**GPIO Terminal**	**GPIMON**
0 (Analog input mode)	Don't care	Don't care	Analog signal input -> ADC 8-bit	L
1	1 (Output mode)	1	H	1
		0	L	0
	0 (Input mode)	Don't care	H	1
			L	0
			Hi-z[1]	X

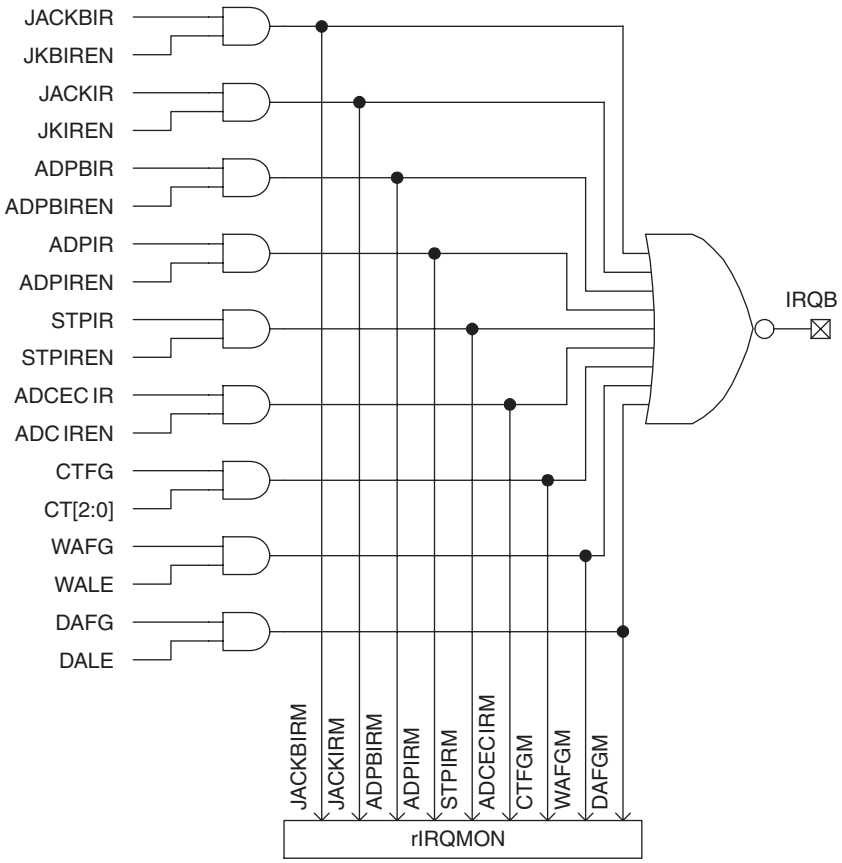
Note: 1. Hi-z is prohibited.

5.11 IRQ Monitor

With IRQ monitor, AT73C206 can read all the permitted interrupt request flags coming from different functional blocks

When interrupt occurred, CPU is informed it by asserting IRQB and read register rIRQMON register to identify which block is producing the interrupt. The rIRQMON is read only register. NOR gate signal of each permitted interrupt request flags will be output from IRQB.

Figure 5-37. IRQ Monitor Block Diagram



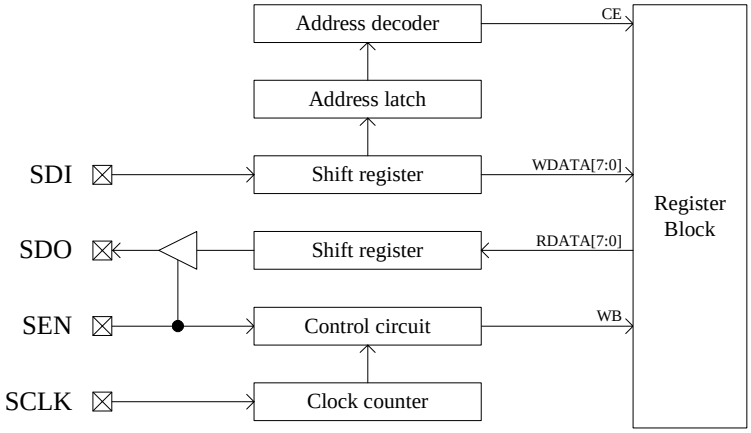
5.12 CPU Interface

AT73C206 employs a synchronous SPI for interfacing to CPU.

5.12.1 SEN and Data Read Write Timing

AT73C206 interfaces with CPU using 4 signal lines. SDI is data input (Write) from CPU and SDO is data output (Read) to CPU. SCLK is synchronous clock and CPU outputs data at falling edge of SCLK and inputs at rising edge of SCLK. AT73C206 CPU interface consists of Address decoder, Address latch, Shift register, Control circuit and Clock counter. Refer to the diagram below.

Figure 5-38. CPU Interface Configuration



5.12.2 Data Transmission Format

An “H” to “L” transition on SEN line asserts data transmission and an “L” to “H” transition deasserts data transmission. The data is transmitted by byte. The first 7 bits contains register address and the last bit determines Read or Write. When writing mode, the following 1 byte will be the data. When read mode, the following 8-bit is ignored and an appointed address data (8-bit) is output from SDO pin. CPU needs to deassert SEN everytime after read and write data.

Figure 5-39. Writing Data

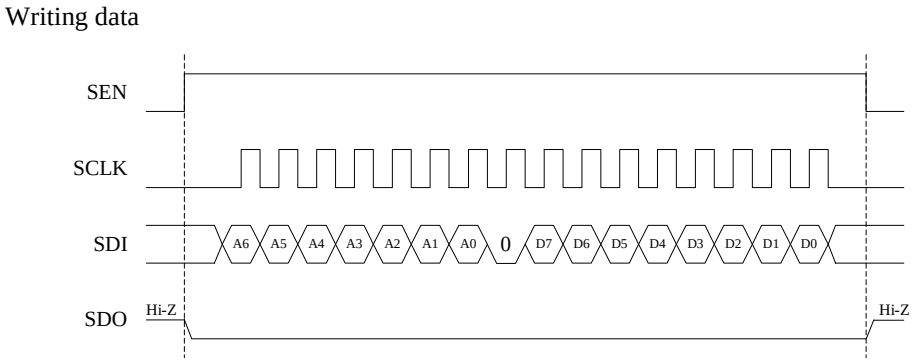
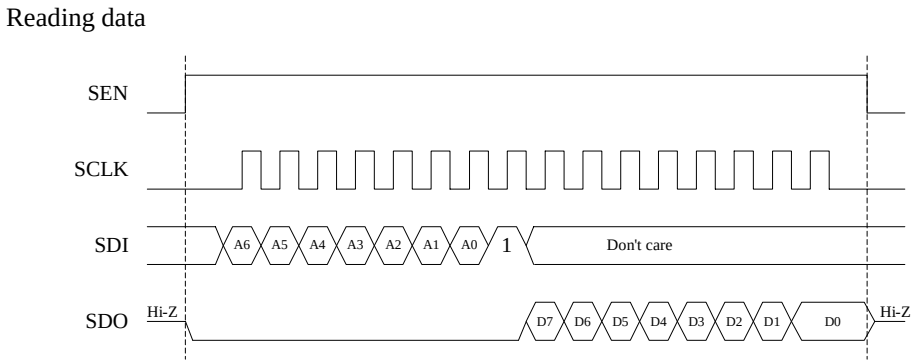


Figure 5-40. Reading Data



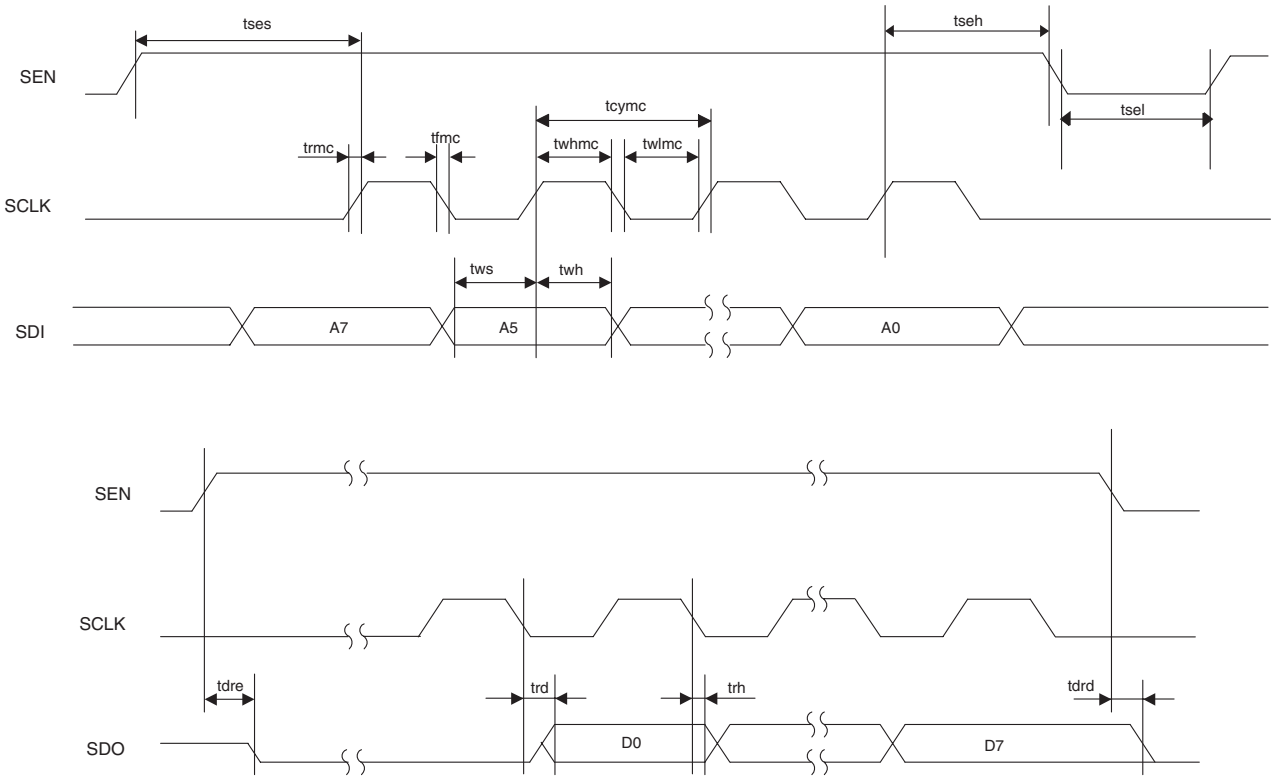
5.12.3 Target Electrical Characteristics

AC characteristics: Ta = -30° C to 85° C

Table 5-42. AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
tcymc	CLK cycle time	100			ns
twhmc	CLK cycle high interval	50			ns
twlmc	CLK cycle low interval	50			ns
trmc	CLK rise time			20	ns
tfmc	CLK fall time			20	ns
tws	Write data setup time	20			ns
twh	Write data hold time	10			ns
trd	Read data delay time			25	ns
trh	Read data hold time	0			ns
tdre	Read data output enable delay time			25	ns
tdrd	Read data output disable delay time			25	ns
tses	Time from SEN “H” to a SCK input	50			ns
tseh	SEN “H” hold time	100			ns
tsel	SEN Minimum “L” time	100			ns

Figure 5-41. CPU Interface Timing Chart



6. Registers

Name	Address	Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LDO	00	LDOEN	R/W	-	LDO10ON	LDO9ON	LDO8ON	LDO7ON	LDO6ON	LDO5ON	LDO4ON
	01	LDO1CNT	R/W	OPMODEV	-	-	OPMODE1	-	-	LDO1DAC[1]	LDO1DAC[0]
	02	LDO3CNT	R/W	RESDET DAC[1]	RESDET DAC[0]	-	OPMODE3	-	-	LDO3DAC[1]	LDO3DAC[0]
	03	LDO4CNT	R/W	-	-	-	-	-	-	LDO4DAC[1]	LDO4DAC[0]
	04	LDO5CNT	R/W	-	-	-	-	-	-	LDO5DAC[1]	LDO5DAC[0]
	05	LDO8CNT	R/W	-	-	-	-	-	-	-	LDO8SEL
White LED Driver	06	LEDCNT	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Charger	07	CHGCNT1	R/W	-	-	TP[1]	TP[0]	RPC[2]	RPC[1]	RPC[0]	CHGONB
	08	CHGCNT2	R/W	-	-	-	-	ADPBIREN	ADPIREN	ADPBIR	ADPIR
ADC	09	ADCCNT	R/W	-	-	BUFEN	BTMEN	ADCECIR	ADCIREN	ADSEL[1]	ADSEL[0]
	0A	ADSTART	R/W	-	-	-	-	-	-	ADEND	ADSTART
	0B	ADCDATA	R	ADDATA[7]	ADDATA[6]	ADDATA[5]	ADDATA[4]	ADDATA[3]	ADDATA[2]	ADDATA[1]	ADDATA[0]
Keypad LED	0C	KLED	R/W	-	-	-	-	-	-	-	KLEDEN
CLK	0D	CLKCNT	R/W	-	-	-	-	-	STPIREN	STPCLKIR	CK32EN
IRQ	0E	IRQMON1	R	-	-	-	-	JACKBIRM	JACKIRM	ADPBIRM	ADPIRM
	0F	IRQMON2	R	-	-	-	CLKSTPM	ADCECIRM	CTFGM	WAFGM	DAFGM
RTC	10	SEC	R/W	-	S40	S20	S10	S8	S4	S2	S1
	11	MIN	R/W	-	M40	M20	M10	M8	M4	M2	M1
	12	HOUR	R/W	-	-	H20PA	H10	H8	H4	H2	H1
	13	WEEK	R/W	-	-	-	-	-	W4	W2	W1
	14	DAY	R/W	-	-	D20	D10	D8	D4	D2	D1
	15	MONTH	R/W	-	-	-	MO10	MO8	MO4	MO2	MO1
	16	YEAR	R/W	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	17	RTCADJ	R/W	-	F6	F5	F4	F3	F2	F1	F0
	18	WAL_MIN	R/W	-	WM40	WM20	WM10	WM8	WM4	WM2	WM1
	19	WAL_HOUR	R/W	-	-	WH20PA	WH10	WH8	WH4	WH2	WH1
	1A	WAL_WEEK	R/W	-	WW6	WW5	WW4	WW3	WW2	WW1	WW0
	1B	DAL_MIN	R/W	-	DM40	DM20	DM10	DM8	DM4	DM2	DM1
	1C	DAL_HOUR	R/W	-	-	DH20PA	DH10	DH8	DH4	DH2	DH1
	1D	-	-	-	-	-	-	-	-	-	-
	1E	RTCCNT1	R/W	WALE	DALE	Z1224	SCRA	TEST	CT2	CT1	CT0
	1F	RTCCNT2	R/W	-		XSTZ	PON	SCRB	CTFG	WAFG	DAFG

	Address	Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Audio/Voice	20	PWRCNT	R/W	-	-	SMICPON	MICPON	-	-	DAUON	DVOON
	21	VMODE	R/W	VASEL	MSSEL	IFEN	VFS	-	-	-	VFORMAT
	22	AMODE	R/W	-	AFS[2]	AFS[1]	AFS[0]	-	-	AFORMAT[1]	AFORMAT[0]
	23	OMODE	R/W	-	-	-	-	MODECO[3]	MODECO[2]	MODECO[1]	MODECO[0]
	24	MUTE	R/W	-	-	MUTEDA	MUTESIDE	-	MUTEDRV	MUTESMIC	MUTEMIC
	25	DRVAG	R/W	-	-	-	DRVAG[4]	DRVAG[3]	DRVAG[2]	DRVAG[1]	DRVAG[0]
	26	MICAG	R/W	-	-	-	-	MICAG[3]	MICAG[2]	MICAG[1]	MICAG[0]
	27	MICDG	R/W	-	-	-	MICDG[4]	MICDG[3]	MICDG[2]	MICDG[1]	MICDG[0]
	28	Reserved	R/W	-	-	-	-	-	-	-	-
	29	Reserved	R/W	-	-	-	-	-	-	-	-
	2A	SIDEDG	R/W	-	-	SIDEDG[5]	SIDEDG[4]	SIDEDG[3]	SIDEDG[2]	SIDEDG[1]	SIDEDG[0]
	2B	RECDG	R/W	-	-	-	RECDG[4]	RECDG[3]	RECDG[2]	RECDG[1]	RECDG[0]
	2C	DATTL	R/W	-	-	DATTL[5]	DATTL[4]	DATTL[3]	DATTL[2]	DATTL[1]	DATTL[0]
	2D	DATTR	R/W	-	-	DATTR[5]	DATTR[4]	DATTR[3]	DATTR[2]	DATTR[1]	DATTR[0]
	2E	Reserved	R/W	-	-	-	-	-	-	-	-
	2F	TNCNT	R/W	TNCON	VRTNSW	VTTNSW	-	TNTIME[3]	TNTIME[2]	TNTIME[1]	TNTIME[0]
	30	TNSET	R/W	TNG3[2]	TNG3[1]	TNG3[0]	FREQSEL[4]	FREQSEL[3]	FREQSEL[2]	FREQSEL[1]	FREQSEL[0]
	31	TNGAIN	R/W	TNG2[3]	TNG2[2]	TNG2[1]	TNG2[0]	TNG1[3]	TNG1[2]	TNG1[1]	TNG1[0]
	32	PTN1SETL	R/W	PTN1[7]	PTN1[6]	PTN1[5]	PTN1[4]	PTN1[3]	PTN1[2]	PTN1[1]	PTN1[0]
	33	PTN1SETH	R/W	-	-	-	-	-	-	-	PTN1[8]
	34	PTN2SETL	R/W	PTN2[7]	PTN2[6]	PTN2[5]	PTN2[4]	PTN2[3]	PTN2[2]	PTN2[1]	PTN2[0]
	35	PTN2SETH	R/W	-	-	-	-	-	-	-	PTN2[8]
	36	APLLCNT	R/W	APLLPON	CKOSEL[2]	CKOSEL[1]	CKOSEL[0]	-	-	-	APLLSRC
	37	VPLLCNT	R/W	VPLLPON	-	-	-	-	-	-	VPLLSRC
	38	ADIVNL	R/W	ADIVN[7]	ADIVN[6]	ADIVN[5]	ADIVN[4]	ADIVN[3]	ADIVN[2]	ADIVN[1]	ADIVN[0]
	39	ADIVNH	R/W	-	-	-	-	ADIVN[11]	ADIVN[10]	ADIVN[9]	ADIVN[8]
	3A	ADIVML	R/W	ADIVM[7]	ADIVM[6]	ADIVM[5]	ADIVM[4]	ADIVM[3]	ADIVM[2]	ADIVM[1]	ADIVM[0]
	3B	ADIVMH	R/W	-	-	-	-	ADIVM[11]	ADIVM[10]	ADIVM[9]	ADIVM[8]
	3C	VDIVNL	R/W	VDIVN[7]	VDIVN[6]	VDIVN[5]	VDIVN[4]	VDIVN[3]	VDIVN[2]	VDIVN[1]	VDIVN[0]
	3D	VDIVNH	R/W	-	-	-	-	VDIVN[11]	VDIVN[10]	VDIVN[9]	VDIVN[8]
	3E	VDIVML	R/W	VDIVM[7]	VDIVM[6]	VDIVM[5]	VDIVM[4]	VDIVM[3]	VDIVM[2]	VDIVM[1]	VDIVM[0]
	3F	VDIVMH	R/W	-	-	-	-	VDIVM[11]	VDIVM[10]	VDIVM[9]	VDIVM[8]
STATUS	40	STMON	R	-	-	-	-	-	JACKMON	CLKSTPMON	ONSWMON

GPIO	41	GPIODIR	R/W	-	-	GPAIN1	GPAIN0	GPIODIR3	GPIODIR2	GPIODIR1	GPIODIR0
	42	GPOSET	R/W	-	-	-	-	GPOSET3	GPOSET2	GPOSET1	GPOSET0
	43	GPIMON	R	-	-	-	-	GPIMON3	GPIMON2	GPIMON1	GPIMON0
JACK	44	JACKCNT	R/W	-	-	-	-	JKBIREN	JKIREN	JACKBIR	JACKIR

Notes: 1. Don't set "1" to reserved bits.
2. Don't write "1" or "0" to undefined registers.
3. The registers 07h08h are power supplied from CHGADP. When not connected to AC adaptor, these registers(07h08h)will be cleared.
4. The registers 10h1Fh are power supplied from VSB. When there is no sub-battery, these registers(10h1Fh) will be cleared.
5. The registers 20H3Fh are power supplied from VDD. If turn off LDO10, registers 20H3Fh will be cleared. At this time, writing in these registers will not be available.

6.1 Regulators Registers

6.1.1 LDOEN: LDOs Output Control Register (Address 00h)

Bit	Symbol	R/W	Function	1	0	Initial value	
						GSP=L	GSP=H
7	-----	-----	Reserved	-----	-----	-----	-----
6	LDO10ON	R/W	LDO10 ON/OFF control bit	ON	OFF	0	0
5	LDO9ON	R/W	LDO9 ON/OFF control bit	ON	OFF	0	0
4	LDO8ON	R/W	LDO8 ON/OFF control bit	ON	OFF	0	1
3	LDO7ON	R/W	LDO7 ON/OFF control bit	ON	OFF	1	0
2	LDO6ON	R/W	LDO6 ON/OFF control bit	ON	OFF	1	1
1	LDO5ON	R/W	LDO5 ON/OFF control bit	ON	OFF	0	1
0	LDO4ON	R/W	LDO4 ON/OFF control bit	ON	OFF	0	0

6.1.2 LDO1CNT: LDO1 Control Register (Address 01h)

Bit	Symbol	R/W	Function	1	0	Initial value
7	OPMODEV	R/W	VREF ECO/Normal control bit	ECO Mode	Normal Mode	0
6-5	-----	-----	Reserved	-----	-----	-----
4	OPMODE1	R/W	LDO1 ECO/Normal control bit	ECO Mode	Normal Mode	0
3-2	-----	-----	Reserved	-----	-----	-----
1-0	LDO1DAC[1:0]	R/W	Setting the output voltage to LDO1	See the LDO1 output voltage table below		(Note)

Output voltage for LDO1

LDO1DAC [1:0]	Output voltage
11	1.5V
10	1.3V
01	1.0V
00	0.9V

Initial value select for LDO1

LDO1SEL	LDO1DAC Initial Value
H	11
L	10

Note: The Initial value is selectable by LDO1SEL pin.
VREF ECO-mode (OPMODEV= “1”) is settable only when LDO1 and LDO3 are in ECO-mode (OPMODE1, OPMODE3) and LDO4~10 are disabled. In other case, set it in Normal-mode (OPMODEV= “0”).

6.1.3 LDO3CNT: LDO3 Control Register (Address 02h)

Bit	Symbol	R/W	Function	1	0	Initial value	
						GSP=L	GSP=H
7-6	RESDETDAC[1:0]	R/W	Setting the RESDET Voltage	As below		00	01
5	-----	-----	Reserved	-----	-----	-----	
4	OPMODE3	R/W	LDO3 ECO/Normal control bit	ECO Mode	Normal Mode	0	
3-2	-----	-----	Reserved	-----	-----	-----	
1-0	LDO3DAC[1:0]	R/W	Setting the output voltage to LDO3	As below		00	01

RESDET detection voltage

RESDETDAC [1:0]	Detection voltage
11	-----
10	For 3.0V
01	For 2.8V
00	For 2.5V

Output voltage of LDO3

LDO3DAC [1:0]	Output voltage
11	-----
10	3.0V
01	2.8V
00	2.5V

6.1.4 LDO4CNT: LDO4 Control Register (Address 03h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-2	-----	-----	Reserved	-----	-----	-----
1-0	LDO4DAC[1:0]	R/W	Setting the output voltage to LDO4	As below		00

Output voltage of LDO4

LDO4DAC [1:0]	Output voltage
11	3.1V
10	3.0V
01	2.8V
00	1.8V

6.1.5 LDO5CNT: LDO5 Control Register (Address 04h)

Bit	Symbol	R/W	Function	1	0	Initial value	
						GSP=L	GSP=H
7-2	-----	-----	Reserved	-----	-----	-----	-----
1-0	LDO5DAC[1:0]	R/W	Setting the output voltage to LDO5	As below		10	01

Output voltage of LDO5

LDO5DAC [1:0]	Output voltage
11	3.3V
10	3.0V
01	2.8V
00	2.7V

6.1.6 LDO8CNT: LDO8 Control Register (Address 05h)

Bit	Symbol	R/W	Function	1	0	Initial value	
						GSP=L	GSP=H
7-1	-----	-----	Reserved	-----	-----	-----	-----
0	LDO8SEL	R/W	Setting the output voltage to LDO8	2.8V	1.8V	0	1

6.2 White LED Driver Register

6.2.1 LEDCNT: White LED Brightness (Address 06h)

Each sink current of DIN1-4 can be set by the code of D4-D0. Defaults shown in **bold**.

LED Current (mA)	Data								Charge Pump
White LED	D7	D6	D5	D4	D3	D2	D1	D0	
25.0	-----	-----	-----	1	1	1	1	1	ON
24.2	-----	-----	-----	1	1	1	1	0	ON
23.4	-----	-----	-----	1	1	1	0	1	ON
22.6	-----	-----	-----	1	1	1	0	0	ON
21.8	-----	-----	-----	1	1	0	1	1	ON
21.0	-----	-----	-----	1	1	0	1	0	ON
20.2	-----	-----	-----	1	1	0	0	1	ON
19.4	-----	-----	-----	1	1	0	0	0	ON
18.5	-----	-----	-----	1	0	1	1	1	ON
17.7	-----	-----	-----	1	0	1	1	0	ON
16.9	-----	-----	-----	1	0	1	0	1	ON
16.1	-----	-----	-----	1	0	1	0	0	ON
15.3	-----	-----	-----	1	0	0	1	1	ON
14.5	-----	-----	-----	1	0	0	1	0	ON
13.7	-----	-----	-----	1	0	0	0	1	ON
12.9	-----	-----	-----	1	0	0	0	0	ON
12.1	-----	-----	-----	0	1	1	1	1	ON
11.3	-----	-----	-----	0	1	1	1	0	ON
10.5	-----	-----	-----	0	1	1	0	1	ON
9.7	-----	-----	-----	0	1	1	0	0	ON
8.9	-----	-----	-----	0	1	0	1	1	ON
8.1	-----	-----	-----	0	1	0	1	0	ON
7.3	-----	-----	-----	0	1	0	0	1	ON
6.5	-----	-----	-----	0	1	0	0	0	ON
5.6	-----	-----	-----	0	0	1	1	1	ON
4.8	-----	-----	-----	0	0	1	1	0	ON
4.0	-----	-----	-----	0	0	1	0	1	ON
3.2	-----	-----	-----	0	0	1	0	0	ON
2.4	-----	-----	-----	0	0	0	1	1	ON
1.6	-----	-----	-----	0	0	0	1	0	ON
0.8	-----	-----	-----	0	0	0	0	1	ON
off	**-----**	**-----**	**-----**	**0**	**0**	**0**	**0**	**0**	**OFF**

6.3 Charger Control Registers

6.3.1 CHGCNT1 : Charger Control Register1 (Address 07h)

Bit	Name	R/W	Function	1	0	Initial value
7-6	-----	-----	Reserved	-----	-----	-----
5-4	TP[1:0]	R/W	Chip temperature detection threshold	As below		01
3-1	RPC [2:0]	R/W	Rapid Charge current select bits	As below		000
0	CHGONB	R/W	Charger ON/OFF control bit	OFF	ON	0

- **TP1, TP0 (bit5, 4) [W]: Chip temperature detection threshold select bits**

TP [1:0]	Chip temperature detection threshold
11	135
10	115
01	105
00	95

- **RPC [2:0] (bit3, 2, 1) [W]: Rapid Charge current select bits**

RPC [2:0]	Rapid Charge current
111	850 mA
110	800 mA
101	750 mA
100	700 mA
011	650 mA
010	600 mA
001	550 mA
000	500 mA

6.3.2 CHGCNT2 : Charger Control Register2 (Address 08h)

Bit	Name	R/W	Function	1	0	Initial value
7-4	-----	-----	Reserved	-----	-----	-----
3	ADPBIREN	R/W	Over voltage adaptor disconnection interrupt enable	Enable	Disable	0
2	ADPIREN	R/W	Over voltage adaptor connection interrupt enable	Enable	Disable	0
1	ADPBIR	R	Over voltage adaptor disconnection interrupt flag	Generated	None	---
0	ADPIR	R	Over voltage adaptor connection interrupt flag	Generated	None	---

6.4 A/D Converter Registers

6.4.1 ADCCNT: A/D Converter Control Register (Address 09h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-6	-----	-----	Reserved	-----	-----	-----
5	BUFEN	R/W	Buffer enable bit	Enable	Disable	0
4	BTMEN	R/W	Battery monitor enable bit	Enable	Disable	0
3	ADCECIR	R/W	ADC “End of Conversion” interrupt request bit (1)	Generated	None	0
2	ADCIREN	R/W	ADC interrupt enable bit	Enable	Disable	0
1-0	ADSEL [1:0]	R/W	ADC input select	As below	As below	00

Note: 1. This bit can be cleared by writing “0” but can not set flag by writing “1”.

ADSEL: Selecting ADC input	
11	P1/AN1
10	P0/AN0
01	IMONI
00	BATMON

6.4.2 ADSTART: A/D Converter Conversion Start Register (Address 0Ah)

Bit	Symbol	R/w	Function	1	0	Initial Value
7-2	-----	-----	Reserved	-----	-----	-----
1	ADEND	R	End of the AD conversion bit	As below		0
0	ADSTART	W	Start of the AD conversion command	As below		0

- **ADEND: End of the AD conversion bit**

1: AD conversion is completed.

This bit is cleared by reading the converted data.

- **ADSTART: Start of the AD conversion command**

1: Start AD conversion

This bit is automatically cleared after conversion starts.

6.4.3 ADCDATA: Conversion Data Register (Address 0Bh)

Bit	Symbol	R/w	Function	1	0	Initial Value
7-0	ADDATA [7:0]	R	Conversion Data	Conversion Data		0

Result ADC	AN0	AN1	IMONI(V)	BATMONI(V)
255	VDDIO	VDDIO	VDDIO	VDDIO x 2
0	0.000	0.000	0.000	0.000

6.5 Keypad LED Registers

6.5.1 KLED: Keypad LED Control Register (Address 0Ch)

Bit	Symbol	R/W	Function	1	0	Initial value	
						GSP=L	GSP=H
7-1	-----	-----	Reserved	-----	-----	-----	-----
0	KLEDEN	R/W	Enable KEYLED Driver	ON	OFF	0	0

6.6 Clock Control Register

6.6.1 CLKCNT: Clock Control Register (Address 0Dh)

Bit	Symbol	R/W	Function	1	0	Initial value	
						GSP=L	GSP=H
-3	-----	-----	Reserved	-----	-----	-----	-----
2	STPIREN	R/W	Clock stop interrupt enable	Enable	Disable	0	0
1	STPIR	R/W	Clock stop interrupt request flag (Note)	Generated	None	0	0
0	CK32EN	R/W	OUT32K output enable	Enable	Disable	1	0

Note: This bit can be cleared by writing “0” but can not set flag by writing “1”.

6.7 Interrupt Request Flag Monitor Registers

6.7.1 IRQMON1: Interrupt Request Flag Monitor 1 Register (Address 0Eh)

Bit	Symbol	R/W	Function	1	0	Initial value
7-4	-----	-----	Reserved	-----	-----	-----
3	JACKBIRM	R	Jack disconnection interrupt flag monitor	Requested	None	0
2	JACKIRM	R	Jack connection interrupt flag monitor	Requested	None	0
1	ADPBIRM	R	Over voltage adaptor disconnection interrupt flag monitor	Requested	None	0
0	ADPIRM	R	Over voltage adaptor connection interrupt flag monitor	Requested	None	0

Note: The bit, whose interrupt is prohibited from generating by each interrupt enable/disable register bit, has “0”.

6.7.2 IRQMON2: Interrupt Request Flag Monitor 2 Register (Address 0Fh)

Bit	Symbol	R/W	Function	1	0	Initial value
7-5	-----	---	Reserved	-----	-----	-----
4	STPIRM	R	Clock stop detection interrupt flag monitor	Requested	None	0
3	ADCECIRM	R	ADC “End of conversion” interrupt flag monitor	Requested	None	0
2	CTFGM	R	RTC CTFG flag monitor	Requested	None	0
1	WAFGM	R	RTC WAFG flag monitor	Requested	None	0
0	DAFGM	R	RTC DAFG flag monitor	Requested	None	0

Note: The bit, whose interrupt is prohibited from generating by each interrupt enable/disable register bit, has “0”.

6.8 RTC Registers

6.8.1 RTC Counter Registers

6.8.1.1 SEC: Second Counter Register (Address 10h)

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved	S40	S20	S10	S8	S4	S2	S1
R/W	---	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	---	---	---	---	---	---	---	---

6.8.1.2 MIN: Minute Counter Register (Address 11h)

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved	M40	M20	M10	M8	M4	M2	M1
R/W	---	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	---	---	---	---	---	---	---	---

6.8.1.3 HOUR: Hour Counter Register (Address 12h)

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved	Reserved	H20PA	H10	H8	H4	H2	H1
R/W	---	---	R/W	R/W	R/W	R/W	R/W	R/W
Default	---	---	---	---	---	---	---	---

Digit display(BCD code)

Second:

Range is 00 to 59. The second digit is rounded up to the minute digit when the count changes from 59 to 00.

Minute:

Range is 00 to 59. The minute digit is rounded up to the hour digit when the count changes from 59 to 00.

Hour:

The hour digit is rounded up to the day or day of the week when the count changes from PM11 to PM12 or from 23 to 00.

The lower-order counter than one second counter is reset when the writing second counter is conducted.

Rounding up from any incorrect and invalid data in the counter register results in unpredictable behavior. Only valid and correct data must be written to the counter register.

6.8.1.4 *WEEK: A Day of a Week Counter Register (Address 13h)*

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved	Reserved	Reserved	Reserved	Reserved	W4	W2	W1
R/W	---	---	---	---	---	R/W	R/W	R/W
Default	---	---	---	---	---	---	---	---

When the day digit is rounded up, the digit is incremented by 1.

Day of week display (septet incremental count): (W4W2W1)=(000) -> (001) -> ...(110) -> (000)

Correspondence between day of the week and count value are user programmable. (e.g. Sunday=000)

Writing (W4W2W1)=(111) is prohibited except when day of the week is unused.

6.8.1.5 *DAY: Day Counter Register (Address 14h)*

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved	Reserved	D20	D10	D8	D4	D2	D1
R/W	---	---	R/W	R/W	R/W	R/W	R/W	R/W
Default	---	---	---	---	---	---	---	---

6.8.1.6 *MONTH: Month Counter and 100year bit Register (Address 15h)*

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved	Reserved	Reserved	MO10	MO8	MO4	MO2	MO1
R/W	---	---	---	R/W	R/W	R/W	R/W	R/W
Default	---	---	---	---	---	---	---	---

6.8.1.7 *YEAR: Year Counter Register (Address 16h)*

Bit	7	6	5	4	3	2	1	0
Symbol	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	---	---	---	---	---	---	---	---

Digit display (BCD code) is as follows according to the auto calendar function.

Day digit:

1 to 31 (January, March, May, July, August, October, and December)

1 to 30 (April, June, September, and November)

1 to 29 (February in a leap year)

1 to 28 (February in regular year)

(The day digit is rounded up to the month digit when the count value returns to 1.)

Month digit:

Range is 1 to 12. The month digit is rounded up to the year digit when the count value returns to 1.

Year digit:

Range is 00 to 99. Years 00, 04, 08, …, 92, 96 are leap years (corresponding to the year 2000 to 2099).

Rounding up from any incorrect and invalid data in the counter register results in unpredictable behavior of the chip. Only valid and correct data must be written to the counter register.

6.8.1.8 RTCADJ: RTC Adjustment Register (Address 17h)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Reserved	F6	F5	F4	F3	F2	F1	F0
R/W	---	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	---	---	---	---	---	---	---	---

F6 ~ F0

The count value of one second is changed by the value of this register. Normally, the second count is incremented by 32768 clock pulses generated by the oscillator. The clock error offset circuit functions by writing data to this register.

Register value F6=“0”: The count value is incremented by ((F5,F4,F3,F2,F1,F0)-1) x 2.

Register value F6=“1”: The count value is decremented by((/F5,/F4,/F3,/F2,/F1,/F0)+1) x 2.

When F6,F5,F4,F3,F2,F1,F0= (*,0,0,0,0,0,*), there is no change in the count value.

/F5, /F4, /F3, /F2, /F1, /F0 indicate reversed F5, F4, F3, F2, F1, F0.

Example

When (F6,F5,F4,F3,F2,F1,F0)=(0,0,0,0,1,1,1) and second digit is 00, 20 or 40, the count value becomes 32768+(7-1)Þ2=32780.It puts clock back.

When (F6,F5,F4,F3,F2,F1,F0)=(0,0,0,0,0,0,1) and second digit is 00, 20 or 40, count value is hold at 32768 without making any change.

When 2 pulses are added to clock every 20sec, the count value becomes 2/(32768 x 20)=3.051 ppm and the clock will be put back around 3ppm. Likewise, when 2 pulses are reduced, 3ppm will be put forward. The clock error can be regulated in maximum ±1.5ppm.

But the clock error offset corrects only clock not oscillator frequency. (32k clock output not guaranteed.)

6.8.2 RTC Alarm_W Registers

6.8.2.1 WAL_MIN: Alarm_W Minute Register (Address 18h)

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved	WM40	WM20	WM10	WM8	WM4	WM2	WM1
R/W	---	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	---	---	---	---	---	---	---	---

6.8.2.2 WAL_HOUR: Alarm_W Hour Register (Address 19h)

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved	Reserved	WH20PA	WH10	WH8	WH4	WH2	WH1
R/W	---	---	R/W	R/W	R/W	R/W	R/W	R/W
Default	---	---	---	---	---	---	---	---

6.8.2.3 WAL_WEEK: Alarm_W A Day of a Week Register (Address 1Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved	WW6	WW5	WW4	WW3	WW2	WW1	WW0
R/W	---	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	---	---	---	---	---	---	---	---

Alarm_W hour register:

Register D5 indicates AM/PM on 12-hour format (AM:0, PM: 1) and 20 WH20PA on 24-hour format.

Set the alarm register only to correct time for proper alarm operation since incorrect data to the alarm register results in no match between the counter and alarm register.

Hour digit on 12-hour format:

AM 0 o'clock -> 12, PM 0 o'clock -> 32

WW0 ~ WW6 correspond to day of the week counter (W4,W2,W1) = (0,0,0) ~ (1,1,0)

When WW0 ~ WW6 are all "0", Alarm_W will not be output.

6.8.3 RTC Alarm_D Registers

6.8.3.1 DAL_MIN : Alarm_D Minute Register (Address 1Bh)

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved	DM40	DM20	DM10	DM8	DM4	DM2	DM1
R/W	---	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	---	---	---	---	---	---	---	---

6.8.3.2 DAL_HOUR : Alarm_D Hour Register (Address 1Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved	Reserved	DH20PA	DH10	DH8	DH4	DH2	DH1
R/W	---	---	R/W	R/W	R/W	R/W	R/W	R/W
Default	---	---	---	---	---	---	---	---

Alarm_D hour Register: D5 indicates AM/PM on 12-hour format(AM:0, PM:1) and DH20PA on 24-hour format.

Set the alarm register only to correct time for proper alarm operation since incorrect data to the alarm register results in no match occurring between the counter and alarm register.

Hour digit on 12-hour format: AM 0 o'clock -> 12, PM 0 o'clock -> 32

6.8.4 RTCCNT1 : RTC Control Register 1 (Address 1Eh)

Bit	Name	R/W	Function	1	0	Initial value
7	WALE	R/W	ALARM_W enable bit	Enable	Disable	0
6	DALE	R/W	ALARM_D enable bit	Enable	Disable	0
5	Z1224	R/W	Selecting 12-hour/24-hour format	As below		0
4	SCRA	R/W	Scratch bit (for user)	1	0	0
3	TEST	W	TEST control bit	As below		0
2-0	CT [2:0]	R/W	Constant cycle interrupt select bit	As below		000

- **Z1224 (bit5) [R/W] : 12-hour/24-hour format select bit**

Z1224	Selecting 12-hour/24-hour format
1	24-hour format
0	AM/PM display 12hour format

Setting 12-hour /24-hour must be preceded writing of time data. Time-digit display table is shown below.

24-hour format	12-hour format	24-hour format	12-hour format
00	12 (AM12)	12	32 (PM12)
01	01 (AM 1)	13	21 (PM 1)
02	02 (AM 2)	14	22 (PM 2)
03	03 (AM 3)	15	23 (PM 3)
04	04 (AM 4)	16	24 (PM 4)
05	05 (AM 5)	17	25 (PM 5)
06	06 (AM 6)	18	26 (PM 6)
07	07 (AM 7)	19	27 (PM 7)
08	08 (AM 8)	20	28 (PM 8)
09	09 (AM 9)	21	29 (PM 9)
10	10 (AM10)	22	30 (PM10)
11	11 (AM11)	23	31 (PM11)

- **SCRA (bit4) [R/W]**

The written value in SCRA (scratch bit) has no effect on RTC operation. And, it is not initialized even at power-off and hold by VSB power.

- **TEST (bit3) [W]**

It is prohibited to write “1” to the Test bit.

TEST	TEST bit
1	Test Mode (Note) Read data is fixed “0”.
0	Normal Mode

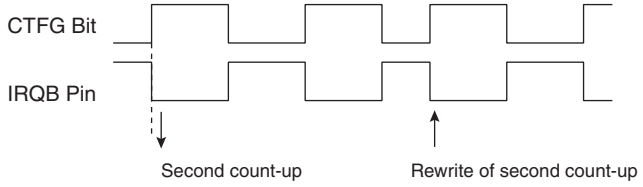
- **CT [2:0] (bit 2,1,0): Constant Cycle Interrupt select bit**

CT [2:0]	Description	
	Waveform mode	**Cycle and falling timing**
111	Level mode *2)	1 time/1 month (every month 1day AM 00 o’clock 00 minute 00 second)
110	Level mode *2)	1 time/1 hour (every hour, 00 minute 00 second)
101	Level mode *2)	1 time/1 min. (every minute, 00 second)
100	Level mode *2)	1 time/ 1sec. (simultaneous with second count-up)
011	Pulse mode *1)	1Hz (Duty50%)
010	Pulse mode *1)	2Hz (Duty50%)
001	-	“L” fixed
000	-	OFF(H)

1. Pulse mode

2 Hz, 1 Hz for clock is provided. See diagram below for second count-up.

Figure 6-1. Pulse Mode Diagram



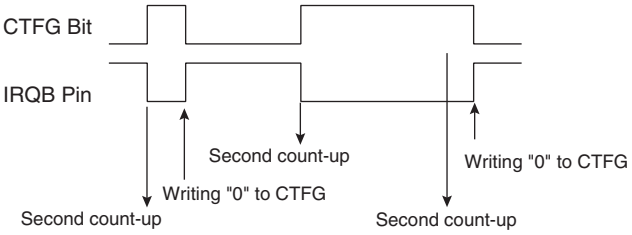
There is a delay from falling edge of output in second count-up. And about 1 sec delayed time than RTC will be readable right after the falling edge of output.

Even though second counter is re-written, IRQB goes “L” once since lower-order counter than one second sec is reset.

2. Level mode

Interrupt cycle is selectable from 1 second, 1 minute, 1 hour or 1 month. Second count-up is synchronous with falling of interrupt output. See the timing chart with interrupt cycle set at 1 second below.

Figure 6-2. Level Mode Diagram



The interrupt cycle varies 1 time/20 sec or 1 time/1 min when use Clock Error Offset circuit

Pulse mode:

The period of “L” output pulse fluctuates in maximum ±3.784 ms. For example, duty is 50±0.3784% at 1Hz.

Level mode:

The cycle/1 sec fluctuates in maximum ±3.784 ms.

6.8.5 RTCCNT2 : RTC Control Register 2 (Address 1Fh)

Bit	Name	R/W	Function	1	0	Initial value
7-6	-----	-----	Reserved	-----	-----	-----
5	XSTZ	R/W	Oscillator stop detection monitor bit	As below		-----
4	PON	R/W	Power-on reset bit	As below		1
3	SCRB	R/W	Scratch bit (for user)	1	0	0
2	CTFG	R/W	Constant cycle interrupt flag bit	As below		0
1	WAFG	R/W	Alarm_W flag bit	As below		0
0	DAFG	R/W	Alarm_D flag bit	As below		0

- **XSTZ (bit5) [R/W]: Oscillator stop detection monitor bit**

XSTZ	Oscillator stop detection monitor bit
1	Normal operation of oscillator
0	Oscillator stop detected

When AT73C206 detects oscillator stop at XSTZ="1", it clears "1" to "0". By reading this bit, host judges whether oscillator has stopped.

- **PON (bit4) [R/W]: Power-on reset bit**

PON	Power-on reset bit
1	Power-on reset detected
0	Normal operation

Once Power-supply becomes 0V, PON becomes "1" and it is kept at "1" even though power-supply voltage returns to normal operation voltage. The validity of clock and calendar data can be judged by XSTZ.

When PON = "1", clock error offset register, control register1 and control register2 (except PON and XSTZ) become "0" so that IRQB and OUT32K pins stop outputting. "0"is only valid value in PON. Writing "1" makes no change.

When PON = "1", writing to control register 1,2, second counter register and clock error offset register is not possible. (But, PON can be cleared.)

- **SCRB (bit3) [R/W]**

The written value in the SCRB (Scratch bit) has no effect on RTC operation. It will not be initialized even at power-off and hold by VSB power.

- **CTFG (bit2) [R/W]: Constant cycle interrupt flag bit**

CTFG	Constant cycle interrupt flag bit
1	Constant cycle interrupt output on (L)
0	Constant cycle interrupt output off (H)

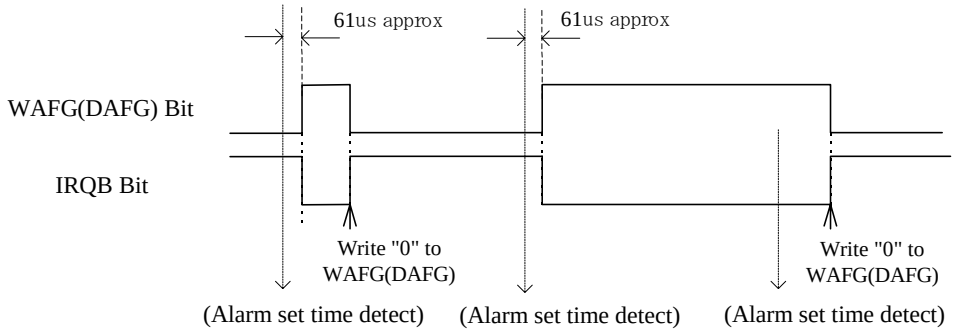
CTFG becomes “1” when constant clock cycle interrupt outputs (IRQB pin).

“0” is only valid data in CTFG when constant cycle interrupt is on level mode. Writing “0” disables IRQB pin ("H"). In next cycle, it will become “L” again. “0” is only valid data in CTFG. Writing “1” makes no change.

- **WAFG, DAFG (bit1, 0): Alarm_W flag bit, Alarm_D flag bit**

WAFG	Alarm_W flag bit	DAFG	Alarm_D flag bit
1	Alarm set time detected	1	Alarm set time detected
0	Alarm set time not detected	0	Alarm set time detected

WAFG and DAFG are valid only when both WALE and DALE bits are “1”. It becomes “1” and keeps it for about 61us when each alarm set time and present time coincide.Only writing “0” to these bits is valid. By writing “0”, IRQB becomes “H”(OFF) and returns “L” at next alarm set time. Writing “1” makes no change. When both WALE and DALE bits are “0”, alarm function is disabled and the reading values of WAFG and DAFG bits are “0”. See the below diagram for relation of WAFG/ DAFG and IRQB output.



6.9 Audio Registers

6.9.1 PWRCNT: Power Control Register (Address 20h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-6	-----	-----	Reserved	-----	-----	-----
5	SMICPON	R/W	SMICBIAS Power-On	ON	OFF	0
4	MICPON	R/W	MICBIAS Power- On	ON	OFF	0
3-2	-----	-----	Reserved	-----	-----	-----
1	DAUON	R/W	Audio digital block enable bit	ON	OFF	0
0	DVOON	R/W	Voice digital block enable bit	ON	OFF	0

6.9.2 VMODE: Voice Mode Setting Register (Address 21h)

Bit	Symbol	R/W	Function	1	0	Initial value
7	VASEL	R/W	Voice/Audio mode select of audio serial interface	Voice	Audio	0
6	MSSEL	R/W	Setting Slave/Master mode of Audio interface	Slave	Master	1
5	IFEN	R/W	Interface enable bit	As below		0
4	VFS	R/W	Setting sampling rate of Voice Codec	As below		0
3-1	-----	-----	Reserved	-----	-----	-----
0	VFORMAT	R/W	Setting Voice interface format	As below	0	0

- **IFEN: Interface enable bit**

1: Enable interface

0: Disable interface

Note: LRCKIO and BCKIO are “L” fixed. (But, only when Master mode)

- **VFS: Setting sample rate of Voice Codec**

VFS	Sampling rate
1	16KHz
0	8KHz

- **VFORMAT : Setting Voice interface format**

VFORMAT	Format
1	Left Justify
0	IIS

6.9.3 AMODE: Audio Mode Setting Register (Address 22h)

Bit	Symbol	R/W	Function	1	0	Initial value
7	-----	-----	Reserved	-----	-----	-----
6-4	AFS [2:0]	R/W	Setting sampling rate of Audio DAC	As below		000
3-2	-----	-----	Reserved	-----		-----
1-0	AFORMAT [1:0]	R/W	Setting Audio interface format	As below		00

- **AFS [2:0]: Setting sample rate of Audio DAC**

AFS [2:0]	Sampling rate	AFS [2:0]	Sampling rate
111	8KHz	011	24KHz
110	11.025KHz	010	32KHz
101	16KHz	001	44.1KHz
100	22.05KHz	000	48KHz

- **AFORMAT [1:0]: Setting Audio interface format**

AFORMAT [1:0]	Format	AFORMAT [1:0]	Format
11	Don't use	01	Left Justify
10	Right Justify	00	IIS

6.9.4 OMODE: CODEC Output Mode Control Register (Address 23h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-4	-----	-----	Reserved	-----	-----	-----
3-0	MODECO [3:0]	R/W	Controlling CODEC output mode	As below		0000

- **MODECO [3:0]: Controlling CODEC output mode**

	Driver Amplifier			Function	
MODECO[3:0]	Receiver	Speaker	Headphone	Receiver	Speaker
1111 to 1001	-	-	-	Reserved	Reserved
1000	OFF	OFF	ON	Audio	Mono
0111	OFF	OFF	ON	Audio	Stereo
0110	OFF	ON	OFF	Audio	Mono
0101	ON	OFF	OFF	Audio	Mono
0100	OFF	OFF	ON	Voice	-
0011	OFF	ON	OFF	Voice	-
0010	ON	OFF	OFF	Voice	-
0001	OFF	OFF	OFF	Standby mode	
0000	OFF	OFF	OFF	Power down mode	

6.9.5 MUTE: MUTE Setting Register (Address 24h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-6	-----	-----	Reserved	-----	-----	-----
5	MUTEDA	R/W	AUDIO DAC MUTE	ON	OFF	1
4	MUTESIDE	R/W	SIDETONE MUTE	ON	OFF	1
3	-----	-----	Reserved	-----	-----	-----
2	MUTEDRV	R/W	Driver AMP MUTE	ON	OFF	1
1	MUTESMIC	R/W	SMIC MUTE	ON	OFF	1
0	MUTEMIC	R/W	MIC MUTE	ON	OFF	1

Note: When set MUTE(only for MUTEDA and MUTESIDE), the gain changes to MUTE(gain=0) with 1dB decrement per fs. When cancel MUTE, the gain returns back to former gain value with 1dB increment per fs as the former gain value is maintained during mute mode.

6.9.6 DRVAG: Analog Driver Gain Setting Register (Address 25h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-5	-----	-----	Reserved	-----	-----	-----
4-0	DRVAG [4:0]	R/W	Analog Driver Gain	As below		0000

DRVAG [4:0]	Gain (dB)	DRVAG [4:0]	Gain (dB)
11111	6	01111	-18
11110	4.5	01110	-19.5
11101	3	01101	-21
11100	1.5	01100	-22.5
11011	0	01011	-24
11010	-1.5	01010	-25.5
11001	-3	01001	-27
11000	-4.5	01000	-28.5
10111	-6	00111	-30
10110	-7.5	00110	-31.5
10101	-9	00101	-33
10100	-10.5	00100	-34.5
10011	-12	00011	-36
10010	-13.5	00010	-37.5
10001	-15	00001	-39
10000	-16.5	00000	-40.5

6.9.7 MICAG: Analog MIC Gain Setting Register (Address 26h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-4	-----	-----	Reserved	-----	-----	-----
3-0	MICAG [3:0]	R/W	Analog MIC Gain	As below		0000

MICAG [3:0]	Gain (dB)	MICAG [3:0]	Gain (dB)
1111	30	0111	14
1110	28	0110	12
1101	26	0101	10
1100	24	0100	8
1011	22	0011	6
1010	20	0010	4
1001	18	0001	2
1000	16	0000	0

6.9.8 MICDG: Voice CODEC TX-DATA1(MIC Path) Digital Gain Setting Register (Address 27h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-5	-----	-----	Reserved	-----	-----	-----
4-0	MICDG [4:0]	R/W	Voice CODEC TX-DATA1 Digital Gain	As below		00000

MICDG [4:0]	Gain (dB)
11111	20
11110	19
11101	18
11100	17
-	-
(-1dB Step)	
-	-
00011	-8
00010	-9
00001	-10
00000	MUTE

Note: Gain changes to the current set value by Smoothing Gain control at 1dB/fs.

6.9.9 SIDEDG: Voice CODEC SIDETONE-DATA Digital Gain Setting Register (Address 2Ah)

Bit	Symbol	R/W	Function	1	0	Initial value
7-6	-----	-----	Reserved	-----	-----	-----
5-0	SIDEDG [5:0]	R/W	Voice CODEC SIDETONEDATA Digital Gain	As below		111111

SIDEDG [5:0]	Gain (dB)
111111	MUTE
111110	-62
111101	-61
111100	-60
-	-
(-1dB Step)	
-	-
000011	-3
000010	-2
000001	-1
000000	0

Note: Gain changes to the current set value by Smoothing Gain control at 1dB/fs.

6.9.10 RECDG: Voice CODEC RX-DATA Digital Gain Setting Register (Address 2Bh)

Bit	Symbol	R/W	Function	1	0	Initial value
7-5	-----	-----	Reserved	-----	-----	-----
4-0	RECDG [4:0]	R/W	Voice CODEC RX-DATA Digital Gain	As below		00000

RECDG [4:0]	Gain (dB)
11111	0
11110	-1
11101	-2
11100	-3
-	-
(-1dB Step)	
-	-
00011	-28
00010	-29
00001	-30
00000	MUTE

Note: Gain changes to the current set value by Smoothing Gain control at 1dB/fs.

6.9.11 DATTL: Audio DAC L-channel Digital Gain Setting Register (Address 2Ch)

Bit	Symbol	R/W	Function	1	0	Initial value
7-6	-----	-----	Reserved	-----	-----	-----
5-0	DATTL [5:0]	R/W	Audio DAC L-channel Digital Gain	As below		111111

6.9.12 DATTR: Audio DAC R-channel Digital Gain Setting Register (Address 2Dh)

Bit	Symbol	R/W	Function	1	0	Initial value
7-6	-----	-----	Reserved	-----	-----	-----
5-0	DATTR [5:0]	R/W	Audio DAC R-channel Digital Gain	As below		111111

DATTL [5:0] DATTR [5:0]	Gain (dB)
111111	MUTE
111110	-62
111101	-61
111100	-60
-	-
(-1dB Step)	
-	-
000011	-3
000010	-2
000001	-1
000000	0

Gain changes to the current set value by Smoothing Gain control at 1dB/fs.

6.9.13 TNCNT: Tone Control Register (Address 2Fh)

Bit	Symbol	R/W	Function	1	0	Initial value
7	TNCON	R/W	Controlling Tone Generator	ON	OFF	0
6	VRTNSW	R/W	Mixing RX voice data and Tone data	Mix	Not Mix	0
5	VTTNSW	R/W	Mixing TX voice data and Tone data	Mix	Not Mix	0
4	-----	-----	Reserved	-----	-----	-----
3-0	TNTIME [3:0]	R/W	Setting time of hardware tone timer	As below		0010

Note: Setting TNCON bit lets the Tone Generator generate tone for the time set by TNTIME bits. After timer overflows, it stops tone and clears TNCON bit automatically. Setting TNCON is available when Voice block and PLL block for voice are powered-on.

TNTIME [3:0]	Time (mS)	TNTIME [3:0]	Time (mS)
1111	Continuous output	0111	150
1110	Don't use (100)	0110	140
1101	Don't use (100)	0101	130
1100	200	0100	120
1011	190	0011	110
1010	180	0010	100
1001	170	0001	90
1000	160	0000	80

6.9.14 TNSET: Type of Generated Tone& Tone Gain Setting Register (Address 30h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-5	TNG3 [2:0]	R/W	Setting TONE3 gain	As below		111
4-0	FREQSEL [4:0]	R/W	Setting type of generated tone	As below		00000

- **TNG3: Setting Tone3 gain**

TNG3 [2:0]	Gain (dB)	TNG3 [2:0]	Gain (dB)
111	-42	011	-18
110	-36	010	-12
101	-30	001	-6
100	-24	000	0

- **FREQSEL: Setting type of generated tone**

FREQSEL [4:0]	DTMF	TONE1 Frequency	TONE2 Frequency
0 0000	DTMF “1”	1209 Hz	697 Hz
0 0001	DTMF“2”	1336 Hz	
0 0010	DTMF“3”	1477 Hz	
0 0011	DTMF“A”	1633 Hz	
0 0100	DTMF“4”	1209 Hz	770 Hz
0 0101	DTMF“5”	1336 Hz	
0 0110	DTMF“6”	1477 Hz	
0 0111	DTMF“B”	1633 Hz	
0 1000	DTMF“7”	1209 Hz	852 Hz
0 1001	DTMF“8”	1336 Hz	
0 1010	DTMF“9”	1477 Hz	
0 1011	DTMF“C”	1633 Hz	
0 1100	DTMF”*”	1209 Hz	941 Hz
0 1101	DTMF“0”	1336 Hz	
0 1110	DTMF“#”	1477 Hz	
0 1111	DTMF“D”	1633 Hz	
1 xxxx	-	Programmable Tone1	Programmable Tone2

6.9.15 TNGAIN: Tone Gain Setting Register (Address 31h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-4	TNG2 [3:0]	R/W	Setting TONE2 gain	As below		1111
3-0	TNG1 [3:0]	R/W	Setting TONE1 gain	As below		1111

TNG1, 2 [3:0]	Gain (dB)	TNG1, 2 [3:0]	Gain (dB)
1111	-15	0111	-7
1110	-14	0110	-6
1101	-13	0101	-5
1100	-12	0100	-4
1011	-11	0011	-3
1010	-10	0010	-2
1001	-9	0001	-1
1000	-8	0000	0

6.9.16 PTN1SETL: Programmable Tone 1 Frequency Setting Register L (Address 32h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-0	PTN1 [7:0]	R/W	Setting frequency of Programmable Tone1	As below		00000000

6.9.17 PTN1SETH: Programmable Tone 1 Frequency Setting Register H (Address 33h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-1	-----	-----	Reserved	-----		-----
0	PTN1 [8]	R/W	Setting frequency of Programmable Tone1	As below		0

6.9.18 PTN2SETL: Programmable Tone 2 Frequency Setting Register L (Address 34h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-0	PTN2 [7:0]	R/W	Setting frequency of Programmable Tone2	As below		00000000

6.9.19 PTN2SETH: Programmable Tone 2 Frequency Setting Register H (Address 35Fh)

Bit	Symbol	R/W	Function	1	0	Initial value
7-1	-----	-----	Reserved	-----		-----
0	PTN2 [8]	R/W	Setting frequency of Programmable Tone2	As below		0

Frequency of programmable tone1 = 7.8125Hz x PTONE1 from 0Hz to 3992.1875Hz

Frequency of programmable tone2 = 7.8125Hz x PTONE2 from 0Hz to 3992.1875Hz

6.9.20 APLLCNT: Audio PLL Control Register (Address 36h)

Bit	Symbol	R/W	Function	1	0	Initial value
7	APLLPON	R/W	Audio PLL Power-On	ON	OFF	0
6-4	CKOSEL [2:0]	R/W	Output Clock Select	As below		000
3-1	-----	-----	Reserved	-----	-----	-----
0	APLLSRC	R/W	Setting input clock to PLL for Audio	As below		0

- **CKOSEL: Output Clock select**

CKOSEL [2:0	CKOUT Pin Output Clock
000	"L" fixed.
001	32.768kHz
010	f_A
011	f_A / 2
100	f_A / 4
101	f_A / 8
110	-
111	-

- **APLLSRC: Setting input clock to PLL for Audio**

APLLSRC	Mode
1	External clock input and programmable mode (Note)
0	Internal X'tal (32.768KHz) mode

Note: Use this mode with setting ADIVN and ADIVM.

6.9.21 VPLLCNT: Voice VPLL Control Register (Address 37h)

Bit	Symbol	R/W	Function	1	0	Initial value
7	VPLLPON	R/W	Voice PLL Power-On	ON	OFF	0
6-1	-----	-----	Reserved	-----	-----	-----
0	VPLLSRC	R/W	Setting input clock to PLL for voice	As below		0

VPLLSRC	Mode
1	External clock input and programmable mode (Note)
0	Internal X'tal (32.768KHz) mode

Note: Use this mode with setting VDIVN and VDIVM.

6.9.22 ADIVNL: Divide factor-N for Audio Setting Register L (Address 38h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-0	ADIVN[7:0]	R/W	Setting divide factor-N for Audio	As below		00000000

6.9.23 ADIVNH: Divide factor-N for Audio Setting Register H (Address 39h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-4	-----	-----	Reserved	-----	-----	-----
3-0	ADIVN[11:8]	R/W	Setting divide factor-N for Audio	As below		0000

NA= ADIVN + 1

6.9.24 ADIVML: Divide factor-M for Audio Setting Register L (Address 3Ah)

Bit	Symbol	R/W	Function	1	0	Initial value
7-0	ADIVM[7:0]	R/W	Setting divide factor-M for Audio	As below		00000000

6.9.25 ADIVMH: Divide factor-M for Audio Setting Register H (Address 3Bh)

Bit	Symbol	R/W	Function	1	0	Initial value
7-4	-----	-----	Reserved	-----	-----	-----
3-0	ADIVM[11:8]	R/W	Setting divide factor-M for Audio	As below		0000

MA= ADIVM + 1

6.9.26 VDIVNL: Divide factor-N for Voice Setting Register L (Address 3Ch)

Bit	Symbol	R/W	Function	1	0	Initial value
7-0	VDIVN[7:0]	R/W	Setting divide factor-N for voice	As below		00000000

6.9.27 VDIVNH: Divide factor-N for Voice Setting Register H (Address 3Dh)

Bit	Symbol	R/W	Function	1	0	Initial value
7-4	-----	-----	Reserved	-----	-----	-----
3-0	VDIVN[11:8]	R/W	Setting divide factor-N for voice	As below		0000

NV= VDIVN + 1

6.9.28 VDIVML: Divide factor-M for Voice Setting Register L (Address 3Eh)

Bit	Symbol	R/W	Function	1	0	Initial value
7-0	VDIVM[7:0]	R/W	Setting divide factor-M for voice	As below		00000000

6.9.29 VDIVMH : Divide factor-M for Voice Setting Register H (Address 3Fh)

Bit	Symbol	R/W	Function	1	0	Initial value
7-4	-----	-----	Reserved	-----	-----	-----
3-0	VDIVM[11:8]	R/W	Setting divide factor-M for voice	As below		0000

MV= VDIVM + 1

6.10 Status Monitor Register

6.10.1 STMON: Status Monitor Register (Address 40h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-3	-----	-----	Reserved	-----	-----	-----
2	JACKMON	R	JACK detector monitor bit	Inserted	Removed	-----
1	CLKSTPMON	R	32KHz OSC stop detection monitor bit	Stop	Oscillate	-----
0	ONSWMON	R	ONSW pin input monitor bit	H	L	-----

6.11 General Purpose I/O Registers

6.11.1 GPIODIR: GPIO Direction Control Register (Address 41h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-6	-----	-----	Reserved	-----	-----	-----
5	GPAIN1	R/W	Input signal mode	Digital	Analog	0
4	GPAIN0	R/W	Input signal mode	Digital	Analog	0
3	GPIODIR3	R/W	GPIO3 direction control bit	Out	In	0
2	GPIODIR2	R/W	GPIO2 direction control bit	Out	In	0
1	GPIODIR1	R/W	GPIO1 direction control bit	Out	In	0
0	GPIODIR0	R/W	GPIO0 direction control bit	Out	In	0

Note: GPIODIR becomes invalid by selecting analog input mode.

6.11.2 GPOSET: GPIO Output Setting Register (Address 42h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-4	-----	-----	Reserved	-----	-----	-----
3	GPOSET3	R/W	GPIO3output logic setting bit	H	L	0
2	GPOSET2	R/W	GPIO2 output logic setting bit	H	L	0
1	GPOSET1	R/W	GPIO1 output logic setting bit	H	L	0
0	GPOSET0	R/W	GPIO0 output logic setting bit	H	L	0

6.11.3 GPIMON: GPIO Input Status Register (Address 43h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-4	-----	-----	Reserved	-----	-----	-----
3	GPIMON3	R	GPIO3 input status bit	H	L	-
2	GPIMON2	R	GPIO2 input status bit	H	L	-
1	GPIMON1	R	GPIO1 input status bit	H	L	-
0	GPIMON0	R	GPIO0 input status bit	H	L	-

Note: When analog input mode is selected, this register will be set to “0”.

6.12 Jackdet Control Register

6.12.1 JACKCNT : Jackdet control register (Address 44h)

Bit	Symbol	R/W	Function	1	0	Initial value
7-4	-----	-----	Reserved	-----	-----	-----
3	JKBIREN	R/W	Jack disconnection interrupt enable	Enable	Disable	0
2	JKIREN	R/W	Jack connection interrupt enable	Enable	Disable	0
1	JACKBIR	R	Jack disconnection interrupt flag	Generated	None	-----
0	JACKIR	R	Jack connection interrupt flag	Generated	None	-----

7. DC Electrical Characteristics

7.1 Absolute Maximum Ratings

The operation exceeding the below “Absolute Maximum Ratings” may cause permanent damage to the device.

The operation of the device within the below stated ratings is not guaranteed.

VCC = V_{BAT},V_{DD}

Table 7-1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Units
V_{BAT}	VBAT Power Pin Voltage	VIN1 to 6, VBSP	-0.3 to 6.0	V
V_{CHG}	AC-Adaptor Voltage Input Pins	VCHGADP	-0.3 to 7.0	V
V_{DD}	VDD Power Pin Voltage	VDDPLL, VDD, VDDHP, VDDANA, VDDIO	-0.3 to 4.5	V
V_{SB}	Backup Part (RTC)	VSB	-0.3 to 4.5	V
V_{DC}	LDO1 Power Pin Voltage	VDC1	-0.3 to 3.6	V
V_{DIN}	DIN Pin Input Voltage	DIN1 to 4	-0.3 to 7.0	V
V_{PIN}	Input Voltage Range	All Input Pins	-0.3 to VCC + 0.3	V
PD	Package Allowable Dissipation(1)	Mounted on Board, T_a = 70° C	1500	mW
T_{stg}	Storage Temperature	-----	-55 to +125	° C

Note: 1. Derating 36[mW/° C] above +70° C.

7.2 Recommendation Operating Conditions

Table 7-2. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{BAT}	VBAT Power Pin Voltage	VIN16, VBSP	3.1	3.6	4.2	V
V_{CHG}	AC-Adaptor Voltage Input Pins	VCHGADP	4.5	5.0	5.5	V
V_{DD}	VDD Power Pin Voltage	VDDPLL, VDD, VDDHP, VDDANA	-3%	2.8	+3%	V
V_{DD2}	VDD Power Pin Voltage	VDDIO	-3%	2.5	+3%	V
V_{SB}	Backup Part (RTC)	VSB	1.6		3.0	V
V_{DC}	LDO1 Power Pin Voltage	VDC1	-3%	1.8	+3%	V
T_a	Temperature of Operation		-30		+85	

7.3 VBAT CMOS Input Pin

Application: LDO1SEL, GSP

Table 7-3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ILI	Input Leakage Current	VIN =0VIN	-1		1	uA
VIH	Input Voltage “H” level		VIN x 0.7			V
VIL	Input Voltage “L” level				VIN x 0.3	V

7.4 VBAT CMOS Schmitt Input Pin with Pull-down

Application: ONSW

Table 7-4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IIL	“L” Input Leakage Current	VIN =0	-1		1	uA
Rpd	Pull-down Resistance			1		MΩ
VT+	Input Rise Threshold Voltage		VIN x 0.5		VIN x 0.8	V
VT-	Input Fall Threshold Voltage		VIN x 0.2		VIN x 0.5	V
VT	Hysteresis		VIN x 0.15			V

7.5 VBAT CMOS Schmitt Input Pin with Pull-down

Application: SMPL

Table 7-5. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IIL	“L” Input Leakage Current	VIN =0	-1		1	uA
Rpd	Pull-down Resistance			1		MΩ
VT+	Input Rise Threshold Voltage			1.4		V
VT-	Input Fall Threshold Voltage			0.6		V
VT	Hysteresis			0.8		V

7.6 VDDIO CMOS Input Pin

Application: PSHOLD, SDI, SEN, SCLK

Table 7-6. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ILI	Input Leakage Current	VIN =0VDDIO	-1		1	uA
VIH	Input Voltage “H” level		VDDIOÞ0.7			V
VIL	Input Voltage “L” level				VDDIOÞ0.3	V

7.7 VDDIO CMOS Output Pin

Application: SDO, ADPINB, IRQB, OUT32K, RSTB, ONOB

Table 7-7. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VOH	Output Voltage “H” level	Iout=-2mA	VDDIO - 0.4			V
VOL	Output Voltage “L” level	Iout=2mA			0.4	V

7.8 VDDIO CMOS I/O Pin

Application: P3, P2, P1/AN1, P0/AN0

Table 7-8. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ILI	Input Leakage Current	VIN =0VDDIO	-1		1	uA
VIH	Input Voltage “H” level		VDDIO x 0.7			V
VIL	Input Voltage “L” level				VDDIO x 0.3	V
VOH	Output Voltage “H” level	Iout=-2mA	VDDIO - 0.4			V
VOL	Output Voltage “L” level	Iout=2mA			0.4	V

7.9 VDD CMOS Input Pin

Application: DIN, CKIN

Table 7-9. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ILI	Input Leakage Current	VIN =VDD	-1		1	uA
VIH	Input Voltage “H” level		VDD x 0.7			V
VIL	Input Voltage “L” level				VDD x 0.3	V

7.10 VDD CMOS Schmitt Input Pin with Pull-up

Application: JKDETI

Table 7-10. Electrical Characteristic

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IIH	“H” Input Leakage Current	VIN =VDD	-1		1	uA
Rpu	Pull-up Resistance			200		kΩ
VT+	Input Rise Threshold Voltage		VDD x 0.5		VDD x 0.8	V
VT-	Input Fall Threshold Voltage		VDD x 0.2		VDD x 0.5	V
VT	Hysteresis		VDD x 0.1			V

7.11 VDD CMOS Output Pin

Application: JKDETO, DOUT, CKOUT

Table 7-11. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VOH	Output Voltage “H” level	Iout=-2mA	VDD – 0.4			V
VOL	Output Voltage “L” level	Iout=2mA			0.4	V

7.12 VDD CMOS I/O Pin

Application: LRCKIO, BCKIO

Table 7-12. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ILI	Input Leakage Current	VIN =0VDD	-1		1	uA
VIH	Input Voltage “H” level		VDD x 0.7			V
VIL	Input Voltage “L” level				VDD x 0.3	V
VOH	Output Voltage “H” level	Iout=-2mA	VDD – 0.4			V
VOL	Output Voltage “L” level	Iout=2mA			0.4	V

8. Revision History

Table 8-1.

Document Ref.	Comments	Change Request Ref.
6329A	First issue	

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com
www.atmel.com/PowerMgmt

Technical Support
pmaac@atmel.com

Sales Contacts
www.atmel.com/contacts/

Literature Requests
www.atmel.com/literature