ADVANCE INFORMATION

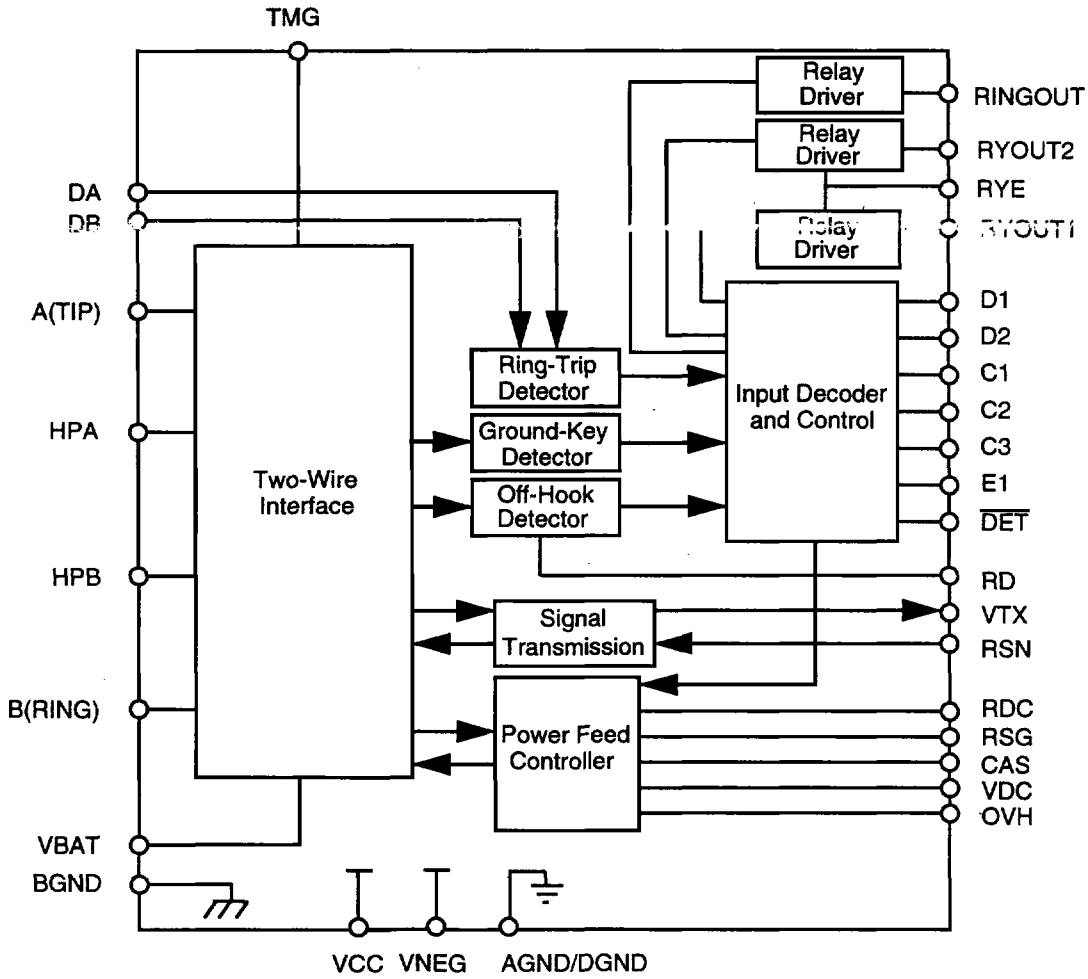
Am7946

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- Ideal for long loop applications
- On-hook transmission
- –40-V to –58-V battery operation
- Internal V_{EE} regulator
- Low standby power
- On-chip Thermal Management (TMG)
- Scaled line voltage (VAB) output
- Supports 2.2-V metering applications
- Two-wire impedance set by scaled external impedance
- Programmable constant current feed
- Programmable overhead
- Programmable loop detect threshold
- Current gain = 500
- Ground key detector
- Tip open state for ground start lines
- Polarity reversal option available
- Three on-chip relay drivers and snubber circuits (32-PLCC only)

BLOCK DIAGRAM



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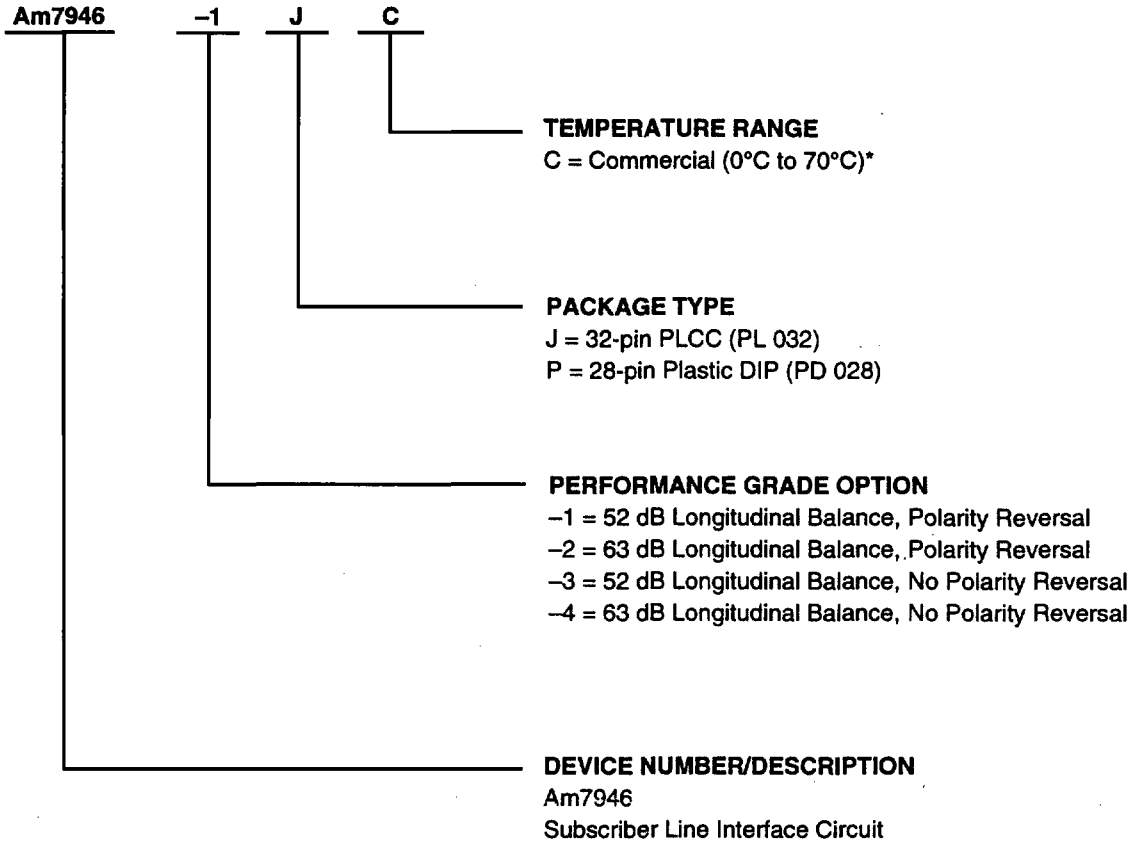
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below



Valid Combinations		
Am7946	–1 –2 –3 –4	JC PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

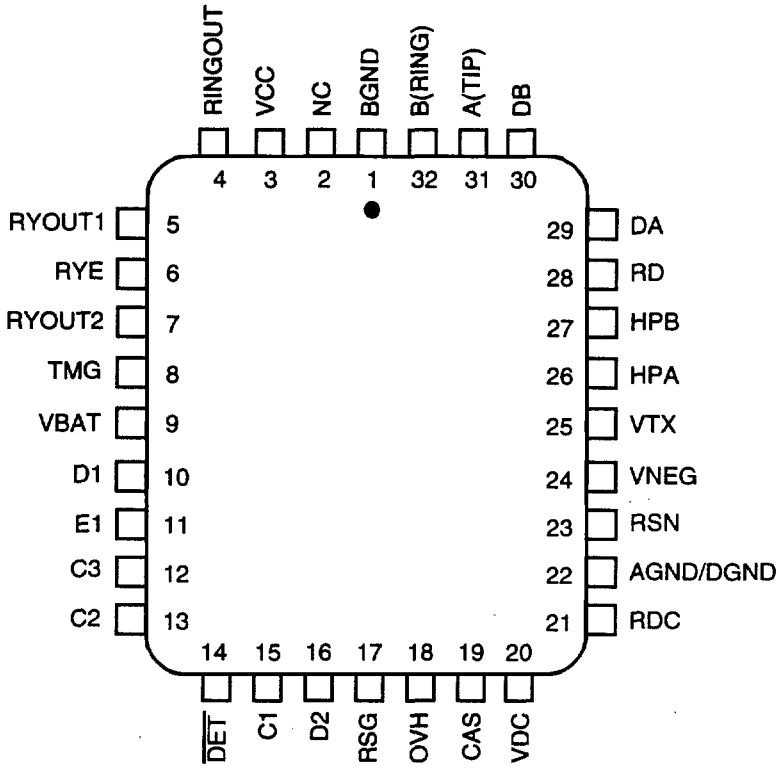
Notes:

**Specifications in this data sheet are guaranteed by testing from 0°C to +70°C. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

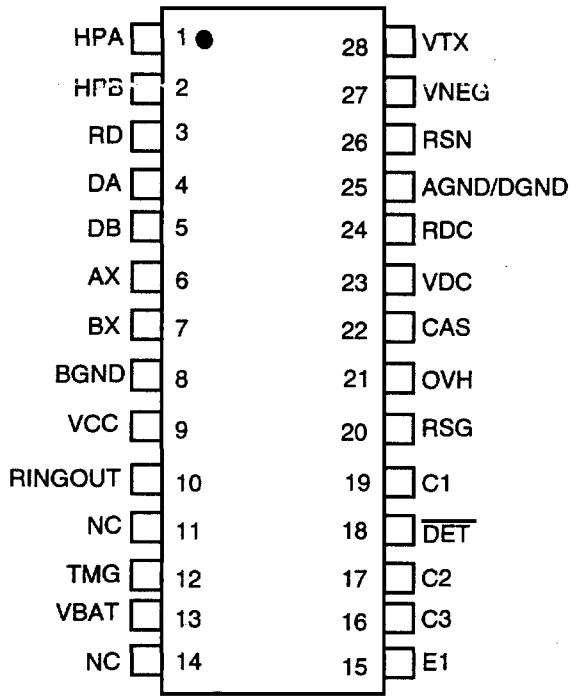
1. Contact the factory for PDIP options.

CONNECTION DIAGRAMS

32-Pin PLCC



28-Pin DIP



Notes:

1. Pin 1 is marked for orientation.

2. NC = not connected.

PIN DESCRIPTIONS

AGND/DGND

(Ground)

Analog and digital ground.

A(TIP)

(Output)

Output of A(TIP) power amplifier.

BGND

(Ground)

Battery (power) ground.

B(RING)

(Output)

Output of B(RING) power amplifier.

CAS

Reference Filter Capacitor

A capacitor should be connected to this pin to filter the internal antisaturation reference voltage when operating from a VBAT1 potential more positive than –50 V.

C3, C2, C1

Decoder (Inputs)

SLIC control pins. C3 is MSB and C1 is LSB. TTL compatible.

D1, D2

Relay Driver Control (Input)

D1 and D2 control the relay drivers RYOUT1 and RYOUT2. A logic Low on D1 activates the RYOUT1 relay driver. A logic Low on D2 activates the RYOUT2 relay driver. TTL compatible.

DA

Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB

Ring Trip Positive (Input)

Positive input to ring trip comparator.

$\overline{\text{DET}}$

Switchhook Detector (Output)

When enabled, a logic Low indicates that a selected condition is detected. The detect condition is selected by the logic inputs (C1, C2, C3, and E1). The output is open collector with a built-in 15-kΩ pull-up resistor.

E1

Ground Key Enable (Input)

A logic High selects the off-hook detector. A logic Low selects the ground key detector. TTL compatible.

HPA

A(TIP) side of the high-pass filter capacitor.

HPB

B(RING) side of the high-pass filter capacitor.

OVH

Overhead Voltage Control (Input)

A logic High enables nonmetering overhead. A logic Low enables 2.2-V metering DC overhead. TTL compatible.

RD

Detector threshold set and filter pin.

RDC

(Output)

Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). The sign of VRDC is negative for normal polarity and positive for reverse polarity.

RINGOUT

Ring Relay Driver (Output)

Open collector driver with emitter internally connected to BGND.

RYE

Common Emitter of RYOUT1/2 (Output)

Emitter output of RYOUT1 and RYOUT2. Normally connected to relay ground.

RYOUT1

Relay/Switch Driver (Output) (Option)

Open collector driver with emitter internally connected to RYE.

RYOUT2

Relay/Switch Driver (Output) (Option)

Open collector driver with emitter internally connected to RYE.

RSG

Saturation Guard (Input)

A resistor from this pin to VEE allows the saturation cut in voltage to be increased while maintaining AC transmission overhead voltage.

RSN

Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 500 times the current into this pin. The networks which program receive gain, two-wire impedance, and feed resistance all connect to this node.

TMG

Thermal Management

An external resistor connects between this pin and VBAT to off-load power dissipation from the Am7946 SLIC. Functions during Normal Polarity and Reverse Polarity states.

VBAT

Battery supply and connection to substrate.

VCC

+5-V power supply.

VDC

(Output)

Scaled VAB output. VDC = |(VAB/20)|. Range of 0 V to 2.5 V. This output is filtered by CHP.

VNEG

–4.75 to VBAT negative supply. This pin is the return for the internal VEE regulator.

VTX

Transmit Audio (Output)

The voltage at this output is equal to the metallic voltage across A(TIP) and B(RING). VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –55°C to +150°C

VCC with respect to AGND/DGND ..... –0.4 V to +7 V

VNEG with respect to AGND/DGND... +0.4 V to VBAT

VBAT with respect to AGND/DGND:

- Continuous ..... +0.4 V to –80 V
- 10 ms ..... +0.4 V to –85 V

BGND with respect to AGND/DGND..... +3 V to –3 V

A(TIP) or B(RING) to BGND:

- Continuous ..... –70 V to +1 V
- 10 ms (F = 0.1 Hz) ..... –70 V to +5 V
- 1 µs (F = 0.1 Hz) ..... –80 V to +8 V
- 250 ns (F = 0.1 Hz) ..... –90 V to +12 V

Current from A(TIP) or B(RING)..... ±150 mA

RINGOUT or RYOUT1 or RYOUT2 current..... 75 mA

RINGOUT voltage..... BGND to +7 V

RINGOUT transient..... BGND to +10 V

RYE voltage ..... BGND to V_{BAT}

RYOUT1 or RYOUT2 voltage ..... RYE to +7 V

RYOUT1 or RYOUT2 transient..... RYE to +10 V

DA and DB inputs

- Voltage on ring trip inputs ..... VBAT to 0 V
- Current into ring trip inputs ..... ±10 mA

C1, C2, C3, D1, D2, E1, OVH

- Input voltage ..... –0.4 V to VCC +0.4 V

Maximum power dissipation, continuous, T_A = 85°C, No heat sink (See note):

- In 32-pin PLCC package..... 1.33 W
- In 28-pin PDIP package..... 1.13 W

Thermal Data..... θ_{JA}

- In 32-pin PLCC package..... 45°C/W typical
- In 28-pin PDIP package..... 53°C/W typical

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Device

Ambient Temperature..... 0°C to +70°C *

VCC ..... +4.75 V to +5.25 V

VNEG ..... –4.75 V to VBAT

VBAT ..... –40 V to –58 V

AGND/DGND..... 0 V

BGND with respect to AGND/DGND ..... –100 mV to +100 mV

Load resistance on VTX to ground.....20 kΩ minimum

The Operating Ranges define those limits between which the functionality of the device is guaranteed.

** Specifications in this data sheet are guaranteed by testing from 0°C to +70°C. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL SPECIFICATIONS (See Note 1)

Description		Test Conditions		Min	Typ	Max	Unit	Note
Transmission Performance								
2-wire return loss		200 Hz to 3.4 kHz (Test Circuit D)		26			dB	1, 4, 7
ZVTX, Analog output impedance					3	20	Ω	4
VVTX, Analog output offset voltage			0°C to +70°C	–35		+35	mV	
			–40°C to +85°C	–40		+40	mV	4
Overload level, 2-wire		Active state, OVH = High		2.5			Vpk	2.1
Overload level, 2-wire		Active state, OVH = Low		6.0			Vpk	2.1
Overload level		On-hook, RLAC = 600 Ω, OVH = High		1.06			Vrms	2.2
THD (Total Harmonic Distortion)		0 dBm			–64	–50	dB	
		+7 dBm			–55	–40	dB	
THD, On-hook		0 dBm, RLAC = 600 Ω				–36	dB	5
Longitudinal Performance (See Test Circuit C)								
Longitudinal to Metallic L-T, L-4 balance	–1, –3	200 Hz to 3.4 Hz		52	70		dB	
	–1, –3	200 Hz to 1 kHz		52			dB	
	–2, –4	normal polarity		63			dB	
	–2	reverse polarity		58			dB	
	–2, –4	normal polarity,	–40°C to +85°C	58			dB	4
	–1, –3	1 kHz to 3.4 kHz		58			dB	
	–2, –4	normal polarity		58			dB	
	–2	reverse polarity		54			dB	
	–2, –4	normal polarity,	–40°C to +85°C	54			dB	4
Longitudinal signal generation 4-L		200 Hz to 800 Hz normal polarity		40			dB	
Longitudinal current per pin (A or B)		Active or OHT state		27	35		mArms	
Longitudinal impedance at A or B		0 to 100 Hz			10	35	Ω/pin	
Idle Channel Noise								
C-message weighted noise		RLDC = 600 Ω	+25°C to +85°C		+7	+10	dBrnC	
		RLDC = 600 Ω	–40°C to +25°C			+12	dBrnC	4
Psophometric weighted noise		RLDC = 600 Ω	+25°C to +85°C		–83	–80	dBmp	4
		RLDC = 600 Ω	–40°C to +25°C			–78	dBmp	4
Insertion Loss and Balance Return Signal (See Test Circuits A and B)								
Gain accuracy 2-wire to 4-wire, 4-wire to 4-wire		0 dBm, 1 kHz nonmetering		–6.22	–6.02	–5.82	dB	
		0 dBm, 1 kHz 2.2-V metering		–6.12	–5.92	–5.72	dB	
		On-hook, OHT		–6.37	–6.02	–5.67	dB	4
Gain accuracy 4-wire to 2-wire		0 dBm, 1 kHz nonmetering		–0.20	0	+0.20	dB	
		0 dBm, 1 kHz 2.2-V metering		–0.20	0	+0.20	dB	
		On-hook, OHT		–0.35	0	+0.35	dB	
Gain accuracy over frequency		300 to 3400 Hz	0°C to +70°C	–0.10		+0.10	dB	
		relative to 1 kHz	–40°C to +85°C	–0.15		+0.15	dB	4
Gain tracking Relative to 0 dBm		+3 dBm to –55 dBm	0°C to +70°C	–0.10		+0.10	dB	4
			–40°C to +85°C	–0.15		+0.15	dB	4

ELECTRICAL SPECIFICATIONS (continued)

Description	Test Conditions	Min	Typ	Max	Unit	Note
Gain tracking, on-hook, OHT Relative to 0 dBm	0 dBm to –37 dBm 0°C to +70°C	–0.10		+0.10	dB	4
	–40°C to +85°C	–0.15		+0.15	dB	4
	+3 dBm to 0 dBm	–0.35		+0.35	dB	4
Group delay	0 dBm, 1 kHz		3		µs	1, 4, 6
Line Characteristics						
I_L, Loop current accuracy	I_L in constant current region	$0.915I_L$	I_L	$1.085I_L$	mA	
I_L, Long loops, active	RLDC = 1840, VBAT = –50 V, OVH = Low	20.5				
	RLDC = 2030, VBAT = –50 V, OVH = High	20.5				
I_L, Accuracy, standby state	$I_L = \frac{\lvert VBAT\rvert - 3\ V}{R_L + 400}$ $T_A = 25°C$	$0.8I_L$	I_L	$1.2I_L$	mA	
	Constant Current Region	16	22	39	mA	
I_LLIM	Active, A and B to ground		100	130	mA	
	OHT, A and B to ground		50		mA	4
I_L, Loop current, open circuit state	$R_L = 0$			100	µA	
I_A, pin A leakage, tip open state	$R_L = 0$			100	µA	
I_B, pin B current, tip open state	B to ground		26		mA	
	B to VBAT + 6 V		15		mA	
VA, Standby, ground start signaling	A to –48 V = 7 kΩ, B to ground = 100 Ω	–7.5	–5			4
VAB, Open circuit voltage	BAT = –50 V	42.75	44.5		V	8
Power Supply Rejection Ratio (Vripple = 100 mVrms), Active Normal State						
VCC	50 Hz to 3400 Hz	30	40		dB	5
VNEG	50 Hz to 3400 Hz	30	50		dB	5
VBAT	50 Hz to 3400 Hz	28	55		dB	5
Effective internal resistance	CAS pin to ground	85	170	255	kΩ	4
Power Dissipation						
On-hook, open circuit			30	70	mW	
On-hook, standby state			60	85	mW	
On-hook, OHT state			120	180	mW	
On-hook, active state	RTMG = 2500 Ω		180	270	mW	
Off-hook, standby state	R_L = 600 Ω		860	1300	mW	
Off-hook, active state	R_L = 300 Ω, RTMG = 2500 Ω		550	800	mW	

ELECTRICAL SPECIFICATIONS (continued)

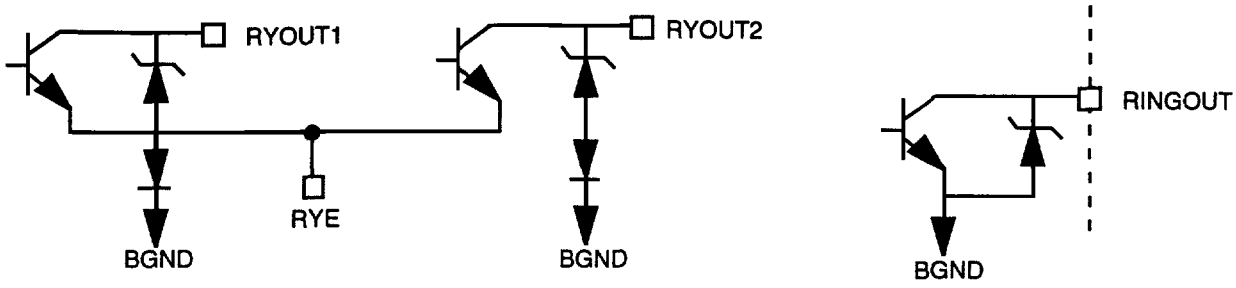
Description	Test Conditions	Min	Typ	Max	Unit	Note
Supply Currents, Battery = –58 V						
ICC, On-hook VCC supply current	Open circuit state		2.7	3.8	mA	
	Standby state		3.3	4.4	mA	
	OHT state		4.9	7.5	mA	
	Active normal state		6.3	8.5	mA	
INEG, On-hook VNEG supply current	Open circuit state		0	0.1	mA	
	Standby state		0	0.1	mA	
	OHT state		0.70	1.1	mA	
	Active normal state		0.70	1.1	mA	
IBAT, On-hook VBAT supply current	Open circuit state		0.35	1.0	mA	
	Standby state		1.0	1.5	mA	
	OHT state		1.9	4.7	mA	
	Active normal state		3.0	5.7	mA	
RFI Rejection						
RFI rejection	100 kHz to 30 MHz, (See Figure E)			1.0	mVrms	4
Logic Inputs (C1, C2, C3, D1, D2, E1, OVH)						
VIH, Input High voltage		2.0			V	
VIL, Input Low voltage				0.8	V	
IIH, Input High current		–75		40	µA	
IIL, Input Low current		–400			µA	
Logic Output ($\overline{DET}$)						
VOL, Output Low voltage	Iout = 10 mA			1.0	V	
VOL, Output Low voltage	Iout = 0.8 mA			0.40	V	
VOH, Output High voltage	Iout = –0.1 mA	2.4			V	
Ring Trip Detector Input (DA, DB)						
Bias current		–500	–50		nA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6
Loop Detector						
IT, Loop detect threshold	RD = 35.4 kΩ, active	330/RD	375/RD	420/RD	mA	
	RD = 35.4 kΩ, standby	380/RD	430/RD	480/RD	mA	
	RD = 35.4 kΩ, tip open	380/RD	430/RD	480/RD	mA	
Ground Key Detector Thresholds						
Ground key resistive threshold	B to ground	2	5	10	kΩ	
Ground key current threshold	B to ground		10		mA	

Table 1. SLIC Decoding

State	C3	C2	C1	Two-Wire Status	($\overline{DET}$) Output E1 = 1	($\overline{DET}$) Output E1 = 0
0	0	0	0	Open circuit	Ring Trip	Ring Trip
1	0	0	1	Ringing	Ring Trip	Ring Trip
2	0	1	0	Active	Loop Det	Ground Key
3	0	1	1	On-hook TX (OHT)	Loop Det	Ground Key
4	1	0	0	Tip open	Loop Det	Ground Key
5	1	0	1	Standby	Loop Det	Ground Key
6	1	1	0	Active polarity reversal	Loop Det	Ground Key
7	1	1	1	OHT polarity reversal	Loop Det	Ground Key

Note:
Only –1 and –2 performance grade devices support polarity reversal.

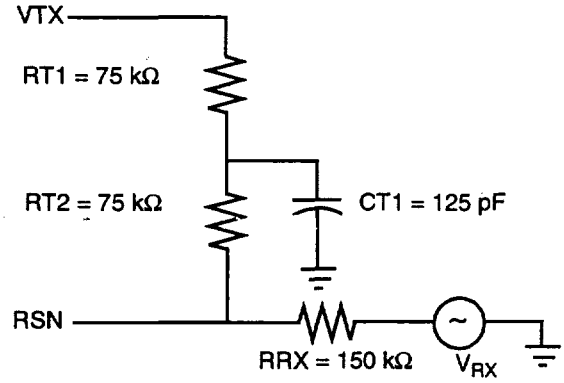
RELAY DRIVER SCHEMATICS



Description		Test Conditions	Min	Typ	Max	Unit	Note
Relay Driver Output (RYOUT1, RYOUT2, and RINGOUT)							
VOL, On voltage	(each output)	IOL = 30 mA		+0.25	+0.4	V	
VOL, On voltage	(each output)	IOL = 40 mA		+0.35	+0.6	V	4
IOH, Off leakage	(each output)	VOH = +5 V			100	µA	
Zener break over	(each output)	IZ = 100 µA	6.6	7.9		V	
Zener ON voltage	(each output)	IZ = 30 mA		11		V	

Notes:

1. *Unless otherwise noted, test conditions are: BAT = –52 V, VCC = +5 V, VNEG = –5 V, R_L = 600 Ω, RDC1 = RDC2 = 28.4 kΩ, RD = 35.4 kΩ, RSG = 0 Ω to GND, RTMG = 2.5 kΩ, no fuse resistors, CHP = 0.22 µF, CDC = 0.1 µF, CCAS = 0.1 µF, D1 = 1N400x, two-wire AC input impedance is a 600-Ω resistance synthesized by the programming network shown below.*



2.1 Overload level is defined when THD = 1%.

2.2 Overload level is defined when THD = 1.5%.

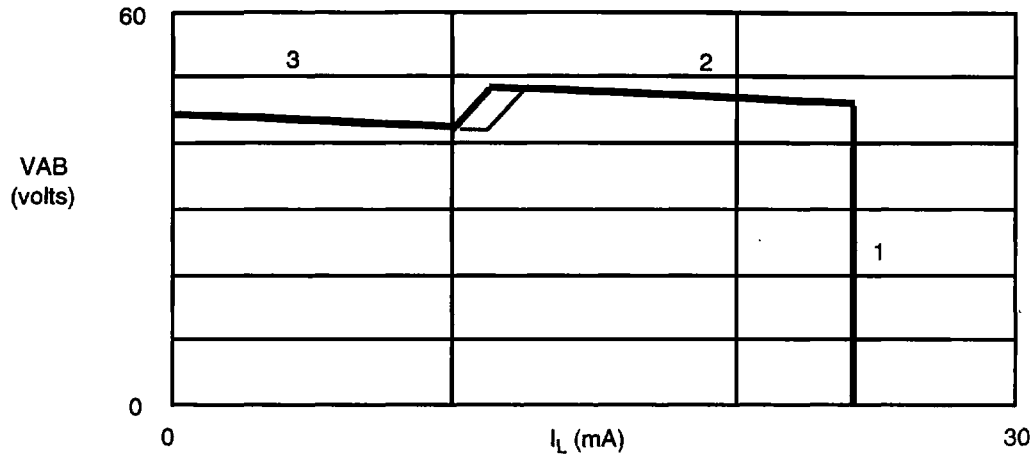
3. *Balance return signal is the signal generated at VTX by VRX. This specification assumes that the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0-Ω source impedance. 2-MΩ specified for system design only.*
7. *Group delay can be greatly reduced by using a ZT network such as that shown in Note 1 above. The network will reduce the group delay to less than 2 µs and increase 2WRL. The effect of group delay on linecard performance may also be compensated for by synthesizing complex impedance with the SLAC™ or DSLAC™ device.*
8. *If |BAT| drops below 50 V, the VAB voltage will track the battery to preserve transmission capability. Open-circuit VAB can be modified using RSG.*

Table 2. User-Programmable Components

$ZT = 250(Z_{2WIN} - 2R_F)$	ZT is connected between the VTX and RSN pins. The fuse resistors are R_F and Z_{2WIN} is the desired 2-wire AC input impedance. When computing ZT, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{500Z_T}{Z_T + 250(Z_L + 2R_F)}$	Z_{RX} is connected from VRX to RSN. ZT is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{1280}{I_{LOOP}}$ $C_{DC} = 1.5\ ms \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1}R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. RDC1 and RDC2 are approximately equal. I_{LOOP} is the desired loop current in the constant current region.
$R_D = \frac{375}{I_T}$, $C_D = \frac{0.5\ ms}{R_D}$	R_D and C_D form the network connected from R_D to GND and I_T is the threshold current between on hook and off hook.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi Fc}$	C_{CAS} is the filter regulator filter capacitor and Fc is the desired filter cutoff frequency.
$I_{OHT} = \frac{1280}{RDC1 + RDC2}$	OHT loop current (constant current region).
Thermal Management Equations (Normal Active and Tip Open States)	
$RTMG \geq \frac{\lvert VBAT\rvert - 6\ V}{I_{LOOP}}$	RTMG is connected from TMG to VBAT and is used to limit power dissipation within the SLIC in active and tip open modes only.
$P_{RTMG} = \frac{(\lvert VBAT\rvert - 6\ V - (I_L \bullet R_L))^2}{RTMG}$	Power dissipated in the thermal management resistor, RTMG, during active and tip open states.
$P_{SLIC} = VBAT \bullet I_L - P_{RTMG} - R_L(I_L)2 + 0.12W$	Power dissipated in the SLIC while in active and tip open states.

DC FEED CHARACTERISTICS

$R_{DC} = R_{DC1} + R_{DC2} = 56.8\ k\Omega$



VBAT < 48 V,OVH = 1

$$VAB_1 = \frac{1280}{RDC} \bullet R_L$$

$$VAB_2 = 0.818 \bullet |VBAT| + 5.356 - I_L \bullet \frac{RDC}{369}$$

$$VAB_3 = 0.818 \bullet |VBAT| + 2.740 - I_L \bullet \frac{RDC}{359}$$

VBAT ≥ 48 V, OVH = 1

$$VAB_1 = \frac{1280}{RDC} \bullet R_L$$

$$VAB_2 = 0.818 \bullet |VBAT| - 2.276 - I_L \bullet \frac{RDC}{369} + \frac{18587 + \left(RSG + \frac{35500}{|VBAT| - 48}\right)}{1777 + 0.131 \bullet \left(RSG + \frac{35500}{|VBAT| - 48}\right)}$$

$$VAB_3 = 0.818 \bullet |VBAT| - 4.894 - I_L \bullet \frac{RDC}{359} + \frac{18587 + \left(RSG + \frac{35466}{|VBAT| - 48}\right)}{1777 + 0.131 \bullet \left(RSG + \frac{35466}{|VBAT| - 48}\right)}$$

VBAT < 52 V, OVH = 0

$$VAB_1 = \frac{1280}{RDC} \bullet R_L$$

$$VAB_2 = 0.904 \bullet |VBAT| - 3.397 - I_L \bullet \frac{RDC}{369}$$

$$VAB_3 = 0.904 \bullet |VBAT| - 6.015 - I_L \bullet \frac{RDC}{359}$$

Figure 1. Load Line (Typical)

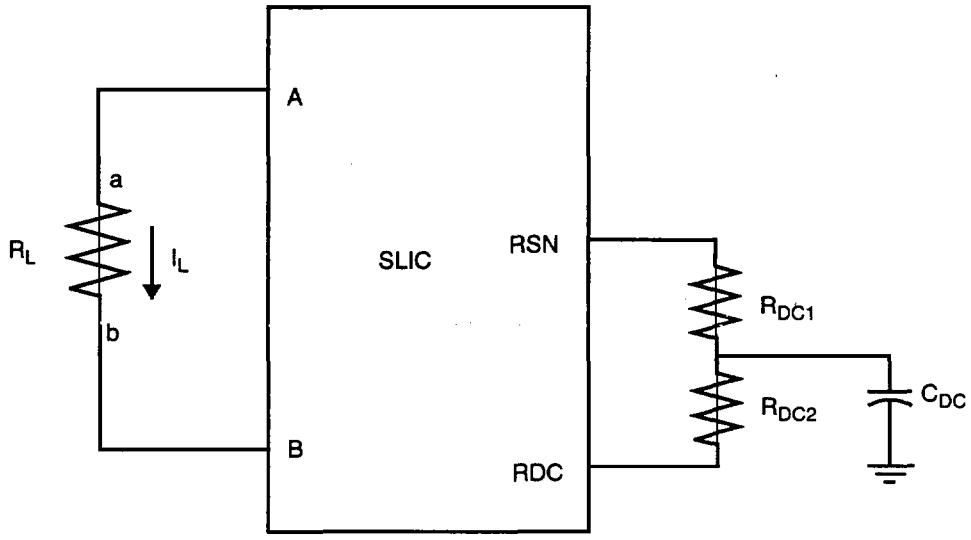
VBAT ≥ 52 V, OVH = 0

$$VAB_1 = \frac{1280}{RDC} \bullet R_L \text{ where } R_L = R_{LOAD} + R_{FUSE}$$

$$VAB_2 = 0.904 \bullet |VBAT| - 11.031 - I_L \bullet \frac{RDC}{369} + \frac{18587 + \left(RSG + \frac{174000}{|VBAT| - 48}\right)}{1777 + 0.131 \bullet \left(RSG + \frac{174000}{|VBAT| - 48}\right)}$$

$$VAB_3 = 0.904 \bullet |VBAT| - 13.649 - I_L \bullet \frac{RDC}{359} + \frac{18587 + \left(RSG + \frac{174000}{|VBAT| - 48}\right)}{1777 + 0.131 \bullet \left(RSG + \frac{174000}{|VBAT| - 48}\right)}$$

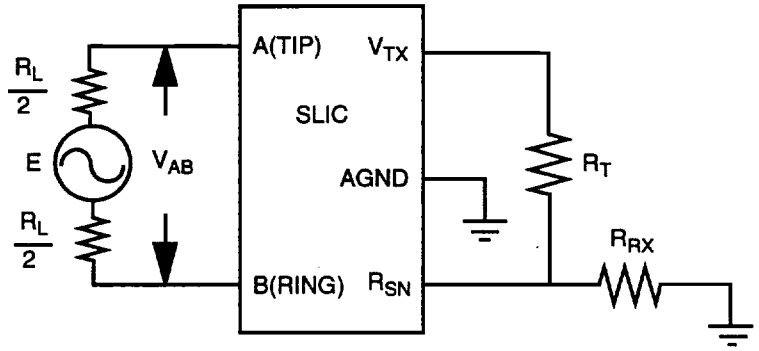
Figure 1. Load Line (Typical) (continued)



Feed current programmed by R_{DC1} and R_{DC2}

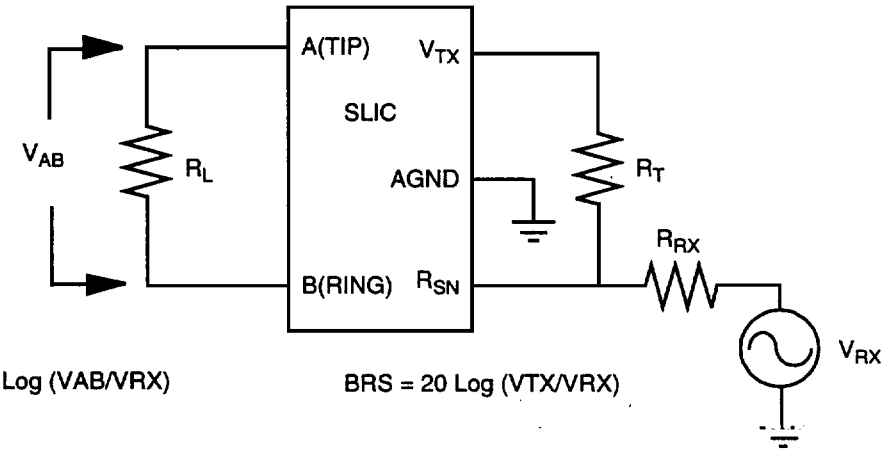
Figure 2. Feed Programming

TEST CIRCUITS



IL2-4 = 20 Log (VTX/VAB)

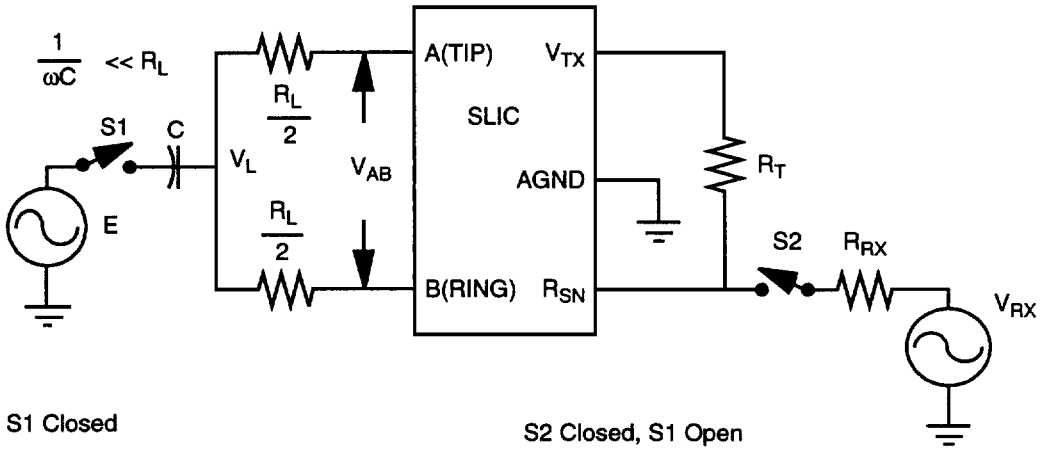
A. Two- to Four-Wire Insertion Loss



IL4-2 = 20 Log (VAB/VRX)

BRS = 20 Log (VTX/VRX)

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed

L-T Long. Bal. = 20 log (VAB/E)

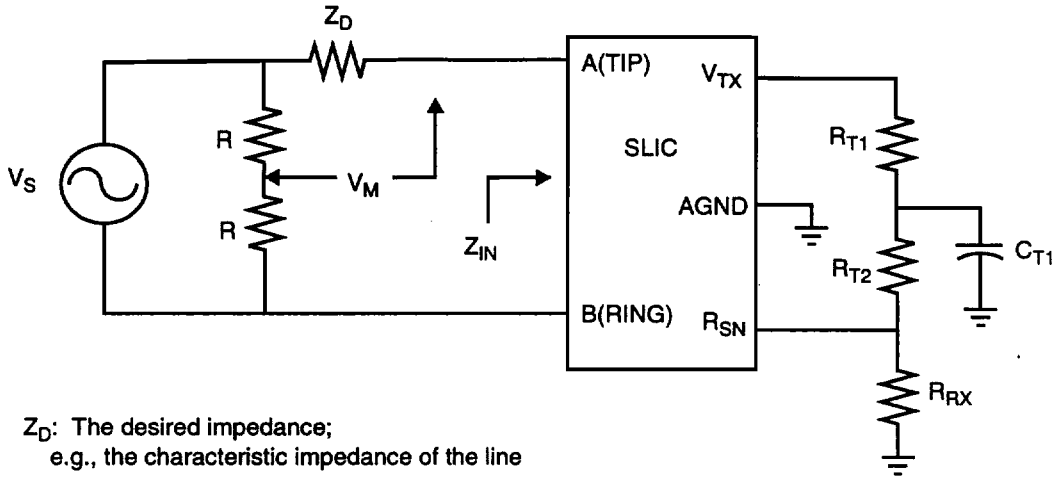
L-T Long. Rej. = 20 log (VTX/E)

S2 Closed, S1 Open

4-L Long. Sig. Gen. = 20 log (VL/VRX)

C. Longitudinal Balance (IEEE 455-1984)

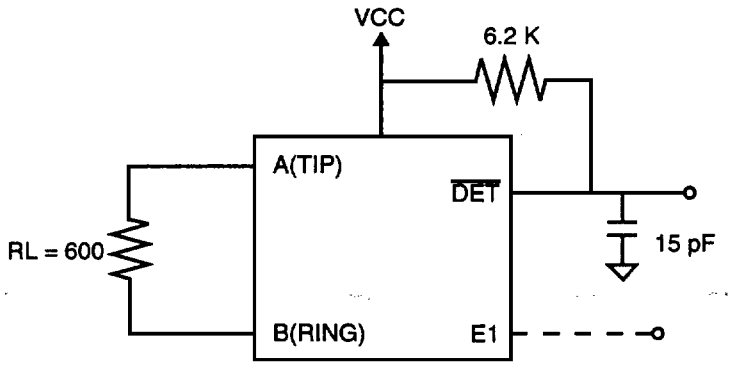
TEST CIRCUITS (continued)



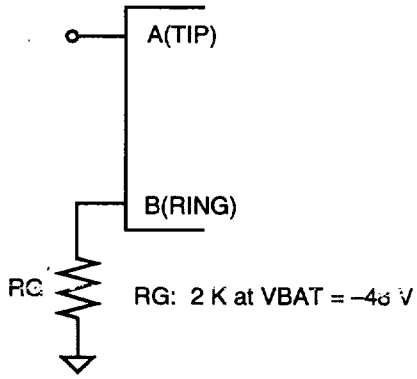
Z_D: The desired impedance;
e.g., the characteristic impedance of the line

Return loss = –20 log(2VM/VS)

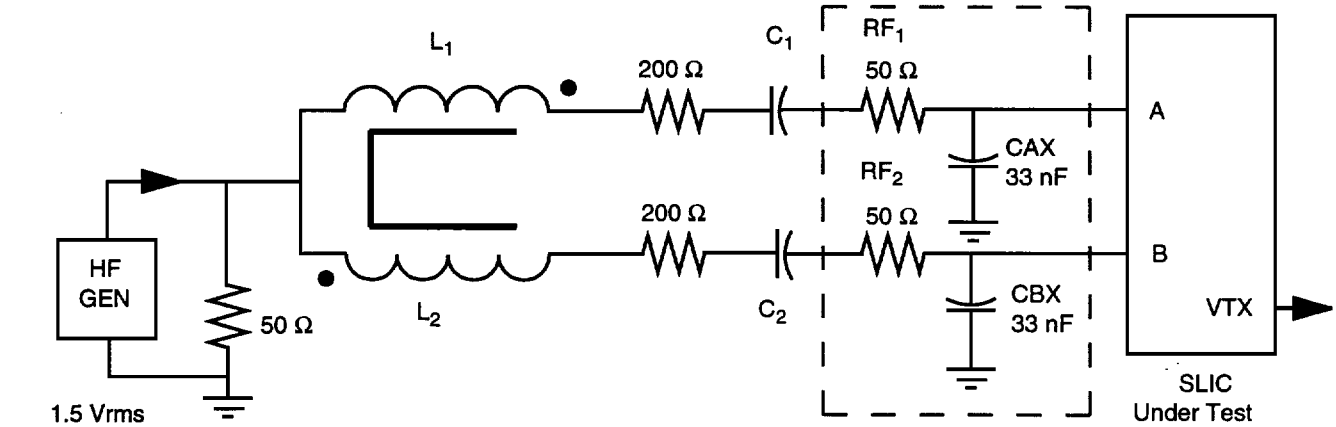
D. Two-Wire Return Loss Test Circuit



E. Loop Detector Switching



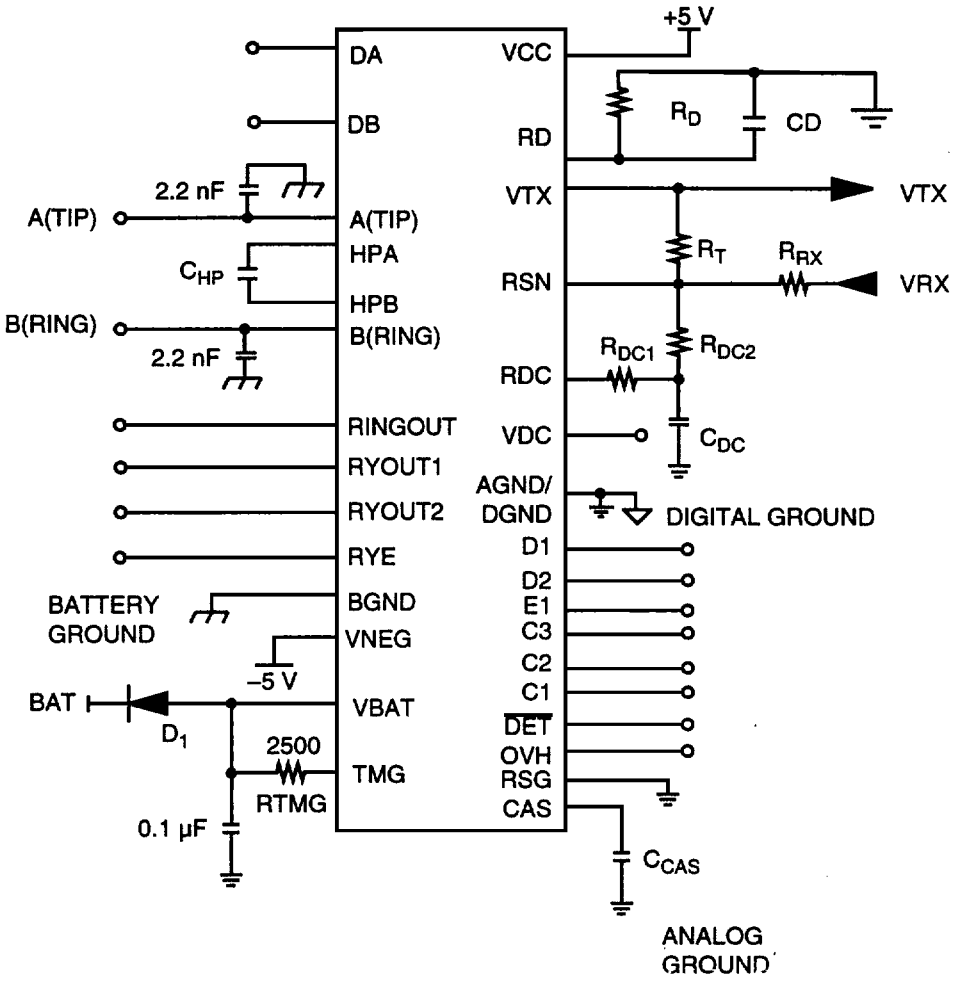
F. Ground-Key Switching



1.5 Vrms
80% Amplitude
Modulated
100 kHz to 30 MHz

G. RFI Test Circuit

TEST CIRCUITS (continued)



H. Am7946 Test Circuit