Advance v0.4

# IGLOO nano Low-Power Flash FPGAs
## with Flash*Freeze Technology

FlashLock®

## Features and Benefits

### Low Power

- nanoPower Consumption—Industry's Lowest Power
- 1.2 V to 1.5 V Core Voltage Support for Low Power
- Supports Single-Voltage System Operation
- Low-Power Active FPGA Operation
- Flash*Freeze Technology Enables Ultra-Low Power Consumption while Maintaining FPGA Content
- Easy Entry to / Exit from Ultra-Low-Power Flash*Freeze Mode

### Small Footprint Packages

- As Small as 3x3 mm in Size

### Wide Range of Features

- 10 k to 250 k System Gates
- Up to 36 kbits of True Dual-Port SRAM
- Up to 71 User I/Os

### Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design When Powered Off

### In-System Programming (ISP) and Security

- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532–compliant)
- FlashLock® to Secure FPGA Contents

### High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure

### Advanced I/Os

- 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 4 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V
- Wide Range Power Supply Voltage Support per JESD8-B, Allowing I/Os to Operate from 2.7 V to 3.6 V
- Wide Range Power Supply Voltage Support per JESD8-12, Allowing I/Os to Operate from 1.14 V to 1.575 V
- I/O Registers on Input, Output, and Enable Paths
- Selectable Schmitt Trigger Inputs
- Hot-Swappable and Cold-Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the IGLOO Family

### Clock Conditioning Circuit (CCC) and PLL†

- Up to Six CCC Blocks, One with an Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz up to 250 MHz)

### Embedded Memory

- 1 kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations)†
- True Dual-Port SRAM (except × 18 organization)†

### Enhanced Commercial Temperature Range

- –20°C to +70°C

**IGLOO nano Devices**

| IGLOO nano Devices | AGLN010 | AGLN015 | AGLN020 | AGLN030[1] | AGLN060 | AGLN125 | AGLN250 |
|---|---|---|---|---|---|---|---|
| System Gates | 10 k | 15 k | 20 k | 30 k | 60 k | 125 k | 250 k |
| Typical Equivalent Macrocells | 86 | 128 | 172 | 256 | 512 | 1,024 | 2,048 |
| VersaTiles (D-flip-flops) | 260 | 384 | 520 | 768 | 1,536 | 3,072 | 6,144 |
| Flash*Freeze Mode (typical, µW) | 2 | 4 | 4 | 5 | 10 | 16 | 24 |
| RAM kbits (1,024 bits)[2] | – | – | – | – | 18 | 36 | 36 |
| 4,608-Bit Blocks[2] | – | – | – | – | 4 | 8 | 8 |
| FlashROM Bits | 1 k | 1 k | 1 k | 1 k | 1 k | 1 k | 1 k |
| Secure (AES) ISP[2] | – | – | – | – | Yes | Yes | Yes |
| Integrated PLL in CCCs[2] | – | – | – | – | 1 | 1 | 1 |
| VersaNet Globals[3] | 4 | 4 | 4 | 6 | 18 | 18 | 18 |
| I/O Banks | 2 | 3 | 3 | 2 | 2 | 2 | 4 |
| Maximum User I/Os | 34 | 49 | 52 | 81 | 71 | 71 | 68 |
| Maximum User I/Os (Known Good Die) | 34 | – | 52 | 83 | 71 | 71 | 68 |
| Package Pins | | | | | | | |
| UC/CS | UC36 | | UC81, CS81 | UC81, CS81 | CS81 | CS81 | CS81 |
| QFN | QN48 | QN68 | QN68 | QN48, QN68 | QN100 | QN100 | QN100 |
| VQFP | | | | VQ100 | VQ100 | VQ100 | VQ100 |

*Notes:*

1. *AGLN030 is available in the Z feature grade only and offers package compatibility with the lower density nano devices. Refer to "IGLOO nano Ordering Information" on page III.*
2. *AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs. AGLN030 and smaller devices do not support this feature.*
3. *Six chip (main) and three quadrant global networks are available for AGLN060 and above.*
4. *For higher densities and support of additional features, refer to the IGLOO and IGLOOe handbooks.*

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† *AGLN030 and smaller devices do not support this feature.*

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# I/Os Per Package

| IGLOO nano Devices | AGLN010 | AGLN015 | AGLN020 | AGLN030 [1] | AGLN060 | AGLN125 | AGLN250 |
|---|---|---|---|---|---|---|---|
| Known Good Die | 34 | – | 52 | 83 | 71 | 71 | 68 |
| UC36 | 23 | | | | | | |
| QN48 | 34 | | | 34 | | | |
| QN68 | | 49 | 49 | 49 | | | |
| UC81 | | | 52 | 66 | | | |
| CS81 | | | 52 | 66 | 60 | 60 | 60 |
| QN100 | | | | | 71 | 71 | 68 |
| VQ100 | | | | 77 | 71 | 71 | 68 |

*Notes:*

1. *AGLN030 is available in the Z feature grade only and offers package compatibility with the lower density nano devices. Refer to "IGLOO nano Ordering Information" on page III.*
2. *When considering migrating your design to a lower- or higher-density device, refer to the* IGLOO Handbook *to ensure compliance with design and board migration requirements.*
3. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*
4. *"G" indicates RoHS-compliant packages. Refer to "IGLOO nano Ordering Information" on page III for the location of the "G" in the part number. For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only.*

**IGLOO FPGAs Package Sizes Dimensions**

| Packages | UC36 | UC81 | CS81 | QN48 | QN68 | QN100 | VQ100 |
|---|---|---|---|---|---|---|---|
| **Length × Width (mm\mm)** | 3 x 3 | 4 x 4 | 5 x 5 | 6 x 6 | 8 x 8 | 8 x 8 | 14 x 14 |
| **Nominal Area (mm$^2$)** | 9 | 16 | 36 | 36 | 64 | 64 | 196 |
| **Pitch (mm)** | 0.4 | 0.4 | 0.5 | 0.4 | 0.4 | 0.5 | 0.5 |
| **Height (mm)** | 0.80 | 0.80 | 0.80 | 0.90 | 0.90 | 0.85 | 1.20 |

# IGLOO nano Ordering Information

AGLN250 V2 – Z ___ VQ G 100 I

Application (Temperature Range)
Blank = Commercial (–20°C to +70°C Ambient Temperature)
I = Industrial (–40°C to +85°C Ambient Temperature)
PP = Pre-Production
ES = Engineering Sample (Room Temperature Only)

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G= RoHS-Compliant Packaging

Package Type
UC = Micro Chip Scale Package (0.4 mm pitch)
CS = Chip Scale Package (0.5 mm pitch)
QN = Quad Flat Pack No Leads (0.4 mm and 0.5 mm pitches)
VQ = Very Thin Quad Flat Pack (0.5 mm pitch)
DIELOT = Known Good Die

Speed Grade
F = 20% Slower than Standard[2]
Blank = Standard

Feature Grade
Z = nano devices without enhanced features[3]
Blank = Standard

Supply Voltage
2 = 1.2 V to 1.5 V
5 = 1.5 V only

Part Number

**IGLOO nano Devices**
AGLN010 = 10,000 System Gates
AGLN015 = 15,000 System Gates
AGLN020 = 20,000 System Gates
AGLN030 = 30,000 System Gates
AGLN060 = 60,000 System Gates
AGLN125 = 125,000 System Gates
AGLN250 = 250,000 System Gates

*Notes:*

1. *Marking Information: IGLOO nano V2 devices do not have V2 marking, but IGLOO nano V5 devices are marked with a V5 designator.*
2. *The DC and switching characteristics for the –F speed grade targets are based only on simulation. The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.*
3. *For the AGLN060, AGLN125, and AGLN250, the Z feature grade does not support the enhanced nano features of Schmitt trigger input, bus hold, cold-sparing, and hot-swap I/O capability. The AGLN030 Z feature grade does not support Schmitt trigger input and bus hold. For the VQ100, CS81, UC81, QN68, and QN48 packages, the Z feature grade and the N part number are not marked on the device.*

## IGLOO nano Product Available in the Z Feature Grade

| **Devices** | **AGLN030** | **AGLN060** | **AGLN125** | **AGLN250** |
|---|---|---|---|---|
| **Packages** | QN48 | – | – | – |
| | QN68 | – | – | – |
| | UC81 | – | – | – |
| | CS81 | CS81 | CS81 | – |
| | – | QN100 | QN100 | – |
| | VQ100 | VQ100 | VQ100 | VQ100 |

## Temperature Grade Offerings

| **Package** | **AGLN010** | **AGLN015** | **AGLN020** | **AGLN030** | **AGLN060** | **AGLN125** | **AGLN250** |
|---|---|---|---|---|---|---|---|
| UC36 | C, I | – | – | – | – | – | – |
| QN48 | C, I | – | – | C, I | – | – | – |
| QN68 | – | C, I | C, I | C, I | – | – | – |
| UC81 | – | – | C, I | C, I | – | – | – |
| CS81 | – | – | C, I | C, I | C, I | C, I | C, I |
| QN100 | – | – | – | – | C, I | C, I | C, I |
| VQ100 | – | – | – | C, I | C, I | C, I | C, I |

*Notes:*

1. *C = Commercial temperature range: –20°C to 70°C ambient temperature.*
2. *I = Industrial temperature range: –40°C to 85°C ambient temperature.*

## Speed Grade and Temperature Grade Matrix

| **Temperature Grade** | **–F** [1] | **Std.** |
|---|---|---|
| C [2] | ✓ | ✓ |
| I [3] | – | ✓ |

*Notes:*

1. *The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is supported only in the commercial temperature range.*
2. *C = Commercial temperature range: –20°C to 70°C ambient temperature.*
3. *I = Industrial temperature range: –40°C to 85°C ambient temperature.*

Contact your local Actel representative for device availability: http://www.actel.com/contact/default.aspx.

# 1 – IGLOO nano Device Overview

## General Description

The IGLOO family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO nano devices enables entering and exiting an ultra-low-power mode that consumes nanoPower while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low-power consumption while the IGLOO nano device is completely functional in the system. This allows the IGLOO nano device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO nano devices the advantage of being a secure, low-power, single-chip solution that is live at power-up (LAPU). The IGLOO nano device is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO nano devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The AGLN030 and smaller devices have no PLL or RAM support. IGLOO nano devices have up to 250 k system gates, supported with up to 36 kbits of true dual-port SRAM and up to 71 user I/Os.

IGLOO nano devices increase the breadth of the IGLOO product line by adding new features and packages for greater customer value in high volume consumer, portable, and battery-backed markets. Features such as smaller footprint packages designed with two-layer PCBs in mind, power consumption measured in nanoPower, Schmitt trigger, and bus hold functionality make these devices ideal for deployment in applications that require high levels of flexibility and low cost.

### Flash*Freeze Technology

The IGLOO nano device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low-power Flash*Freeze mode. IGLOO nano devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO nano V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

During Flash*Freeze mode, each I/O can be set to the following configurations: hold previous state, tristate, HIGH, or LOW.

The availability of low-power modes, combined with reprogrammability, a single-chip and single-voltage solution, and small-footprint packages make IGLOO nano devices the best fit for portable electronics.

## Flash Advantages

### *Low Power*

Flash-based IGLOO nano devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO nano devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO nano devices also have low dynamic power consumption to further maximize power savings; power is reduced even further by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO nano device the lowest total system power offered by any FPGA.

### *Security*

Nonvolatile, flash-based IGLOO nano devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO nano devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO nano devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO nano devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO nano devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO nano devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed IGLOO nano device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of IGLOO nano devices. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. IGLOO nano devices, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. An IGLOO nano device provides the most impenetrable security for programmable logic designs.

### *Single Chip*

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO nano FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

### *Live at Power-Up*

Actel flash-based IGLOO nano devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based IGLOO nano devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO nano device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO nano devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO nano flash FPGAs enable the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 µs) and the device retains configuration and data in registers and RAM.

Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead it retains all necessary information to resume operation immediately.

## Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based IGLOO nano devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO nano device architecture mitigates the need for ASIC migration at higher user volumes. This makes IGLOO nano devices cost-effective ASIC replacement solutions, especially for applications in the consumer, networking/communications, computing, and avionics markets.

With a variety of devices under $1, Actel IGLOO nano FPGAs enable cost-effective implementation of programmable logic and quick time to market.

## Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO nano flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO nano FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

## Advanced Flash Technology

The IGLOO nano device offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO nano FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

## Advanced Architecture

The proprietary IGLOO nano architecture provides granularity comparable to standard-cell ASICs. The IGLOO nano device consists of five distinct and programmable architectural features (Figure 1-3 on page 1-5 to Figure 1-4 on page 1-5):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO nano core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC® family of third-generation-

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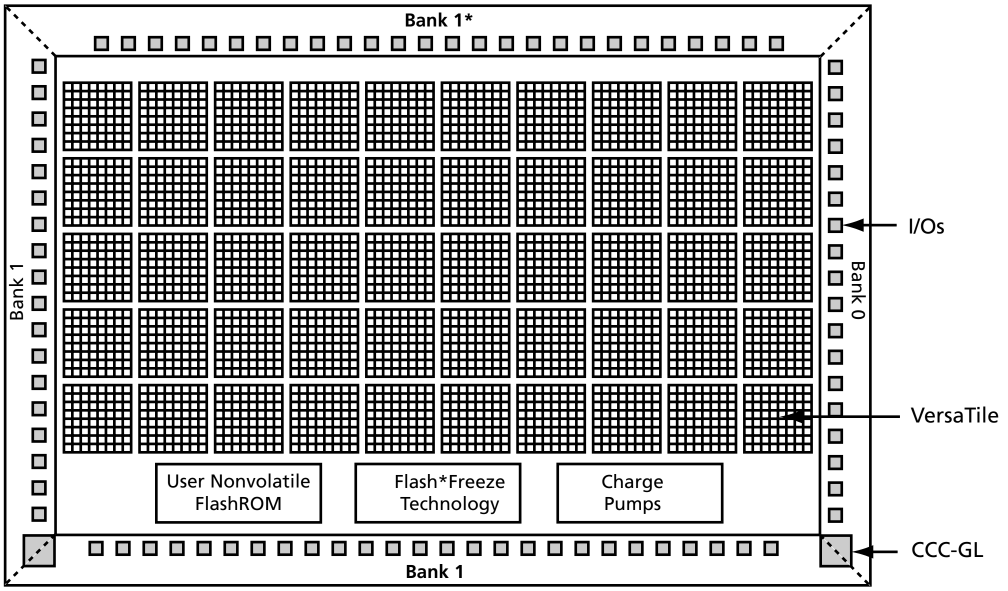
† *The AGLN030 and smaller devices do not support PLL or SRAM.*

architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry enables rapid, single-voltage (3.3 V) programming of IGLOO nano devices via an IEEE 1532 JTAG interface.



*Note:* **Bank 0 for the AGLN030 device*

*Figure 1-1 •* **IGLOO Device Architecture Overview with Two I/O Banks and No RAM (AGLN010 and AGLN030)**

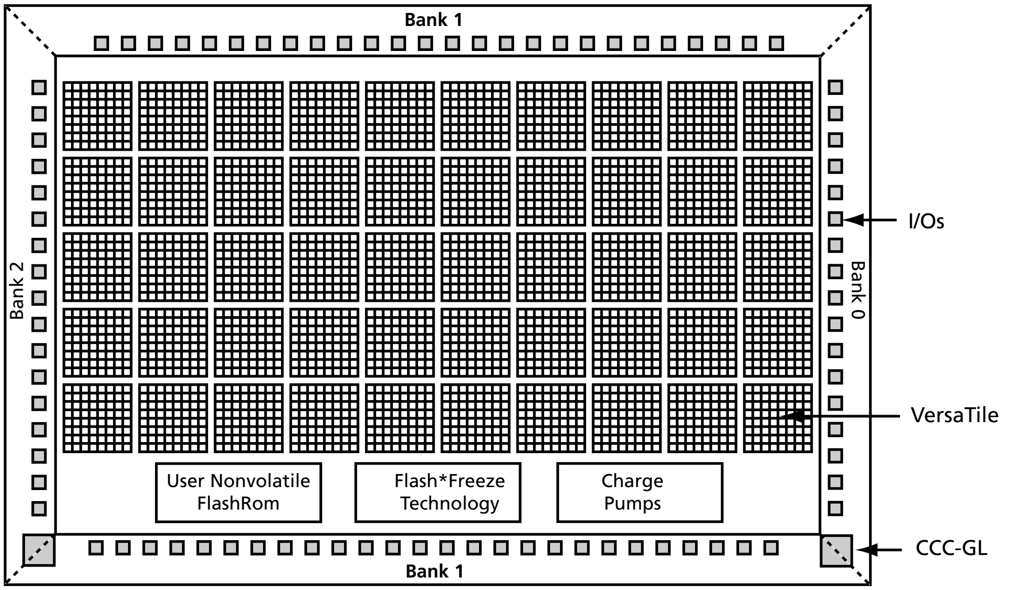


*Figure 1-2 •* **IGLOO Device Architecture Overview with Three I/O Banks and No RAM (AGLN015 and AGLN020)**

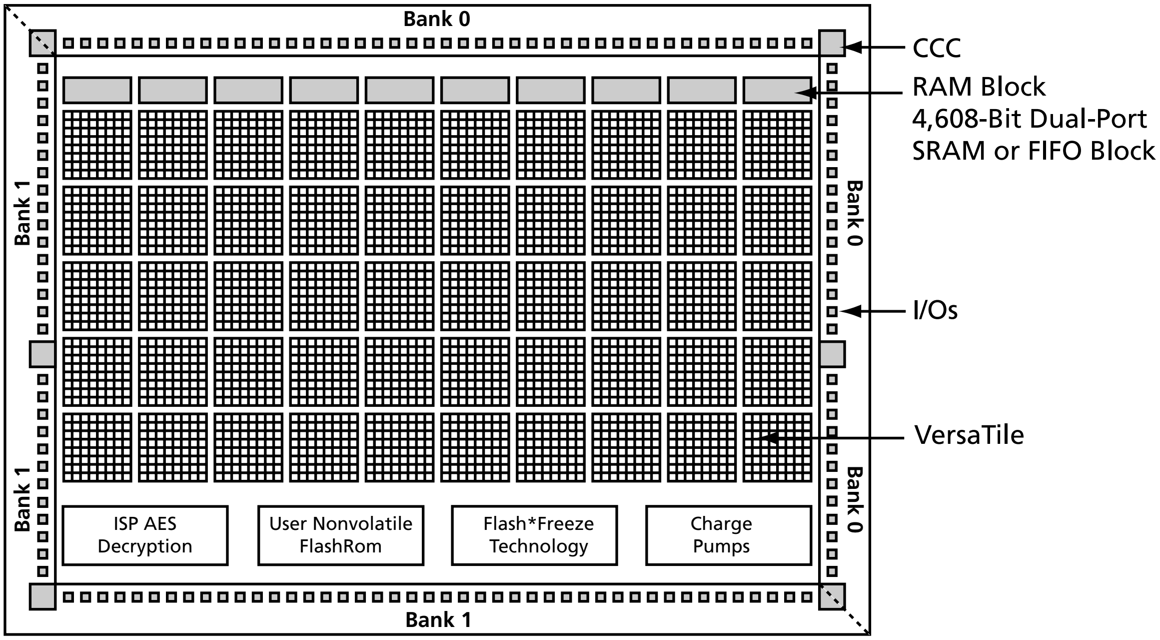


*Figure 1-3 •* **IGLOO Device Architecture Overview with Two I/O Banks (AGLN060, AGLN125)**

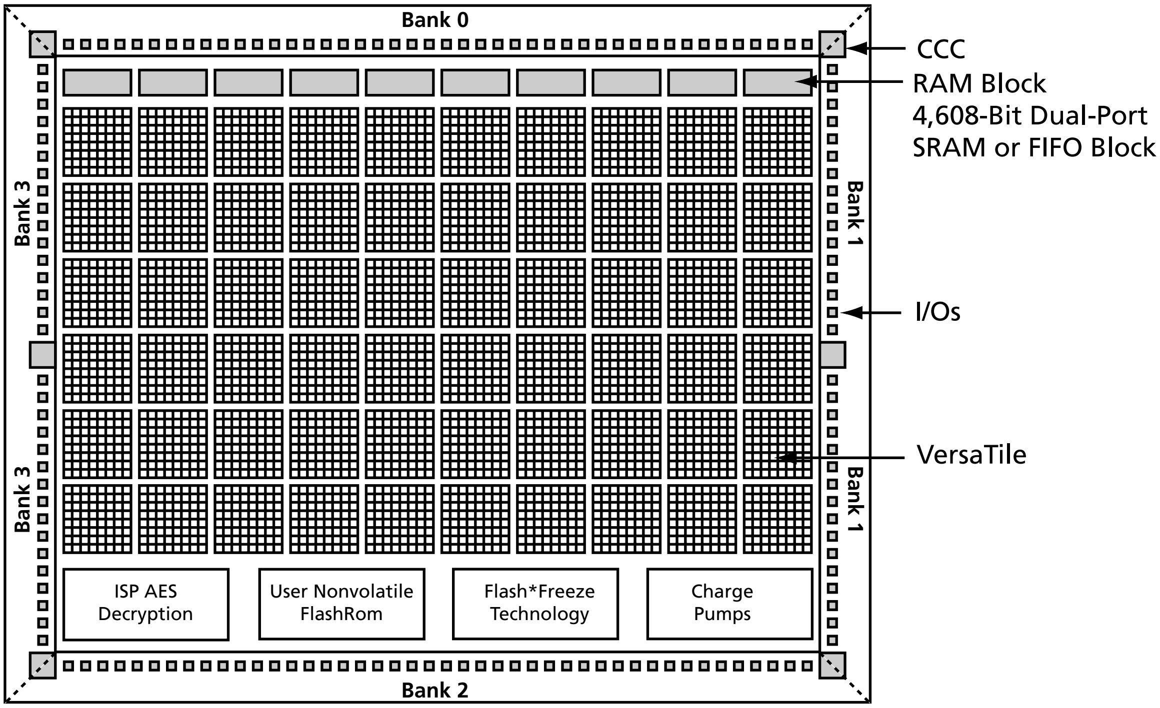


*Figure 1-4 •* **IGLOO Device Architecture Overview with Four I/O Banks (AGLN250)**

## Flash*Freeze Technology

The IGLOO nano device has an ultra-low-power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. I/Os, global I/Os, and clocks can still be driven and can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode.

Alternatively, I/Os can be set to a specific state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 2 µW in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to Figure 1-5 for an illustration of entering/exiting Flash*Freeze mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.

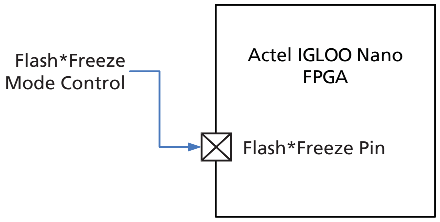


*Figure 1-5 •* **IGLOO nano Flash*Freeze Mode**

## VersaTiles

The IGLOO nano core consists of VersaTiles, which have been enhanced beyond the ProASIC$^{\text{PLUS}®}$ core tiles. The IGLOO nano VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-6 for VersaTile configurations.

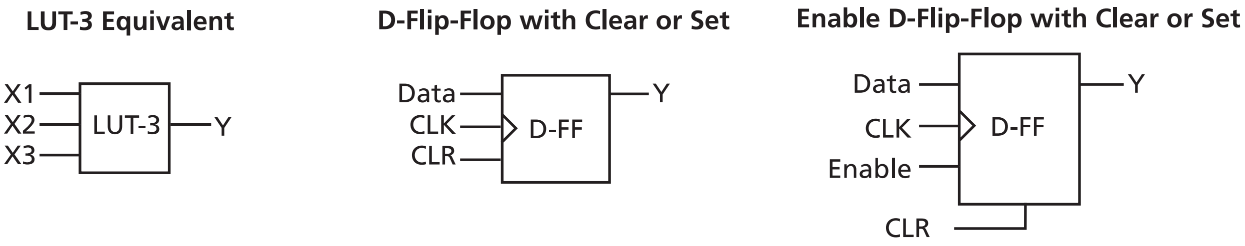


*Figure 1-6 •* **VersaTile Configurations**

## User Nonvolatile FlashROM

Actel IGLOO nano devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO nano IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the AGLN030 and smaller devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel IGLOO nano development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature enables the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

## SRAM and FIFO

IGLOO nano devices (except the AGLN030 and smaller devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in the AGLN030 and smaller devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

## PLL and CCC

Higher density IGLOO nano devices using either the two I/O bank or four I/O bank architectures provide designers with very flexible clock conditioning capabilities. AGLN060, AGLN125, and AGLN250 contain six CCCs. One CCC (center west side) has a PLL. The AGLN030 and smaller devices use different CCCs in their architecture (CCC-GL). These CCC-GLs contain a global MUX but do not have any PLLs or programmable delays.

For devices using the six CCC block architecture, these are located at the four corners and the centers of the east and west sides. All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from dedicated connections to the CCC block, which are located near the CCC.

The CCC block has these key features:

- Wide input frequency range ($f_{IN\_CCC}$) = 1.5 MHz up to 250 MHz
- Output frequency range ($f_{OUT\_CCC}$) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / $f_{OUT\_CCC}$ (for PLL only)

### Global Clocking

IGLOO nano devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

### I/Os with Advanced I/O Standards

IGLOO nano FPGAs feature a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V).

The I/Os are organized into banks with two, three, or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of various single-data-rate applications for all versions of nano devices and double-data-rate applications for the AGLN060, AGLN125, and AGLN250 devices.

IGLOO nano devices support LVTTL and LVCMOS I/O standards, are hot-swappable, and support cold-sparing and Schmitt trigger.

## Wide Range I/O Support

Actel nano devices support JEDEC-defined wide range I/O operation. IGLOO nano devices support both the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

# Part Number and Revision Date

Part Number 51700110-001-3
Revised December 2008

# List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous Version | Changes in Current Version (Advance v0.4) | Page |
|---|---|---|
| Advance v0.3 (November 2008) | The second table note in the "IGLOO nano Devices" table was revised to state, "AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs. AGLN030 and smaller devices do not support this feature." | I |
| | The I/Os per package for CS81 were revised to 60 for AGLN060, AGLN125, and AGLN250 in the "I/Os Per Package"table. | II |
| Advance v0.2 (October 2008) | The "Advanced I/Os" section was updated to include wide power supply voltage support for 1.14 V to 1.575 V. | I |
| | The AGLN030 device was added to product tables and replaces AGL030 entries that were formerly in the tables. | I to IV |
| | The "I/Os Per Package"table was updated for the CS81 package to change the number of I/Os for AGLN060, AGLN125, and AGLN250 from 66 to 64. | II |
| | The "Wide Range I/O Support" section is new. | 1-8 |
| Advance v0.1 (October 2008) | The following tables and sections were updated to add the UC81 and CS81 packages for AGL030:<br>"IGLOO nano Devices"<br>"I/Os Per Package"<br>"IGLOO nano Product Available in the Z Feature Grade"<br>"Temperature Grade Offerings" | N/A |
| | The "I/Os Per Package" table was updated to add the following information to table note 4: "For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only." | II |
| | The "IGLOO nano Product Available in the Z Feature Grade" section was updated to remove QN100 for AGLN250. | IV |
| | The device architecture figures, Figure 1-3 · IGLOO Device Architecture Overview with Two I/O Banks (AGLN060, AGLN125) through Figure 1-4 · IGLOO Device Architecture Overview with Four I/O Banks (AGLN250), were revised. Figure 1-1 · IGLOO Device Architecture Overview with Two I/O Banks and No RAM (AGLN010 and AGLN030) is new. | 1-4 through 1-5 |
| | The "PLL and CCC" section was revised to include information about CCC-GLs in AGLN020 and smaller devices. | 1-7 |
| | The "I/Os with Advanced I/O Standards" section was revised to add information about IGLOO nano devices supporting double-data-rate applications. | 1-8 |

# Datasheet Categories

### Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definition of these categories are as follows:

### Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

### Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

### Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### Unmarked (production)

This version contains information that is considered to be final.

## Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

# Actel Safety Critical, Life Support, and High-Reliability Applications Policy

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# 2 – IGLOO nano DC and Switching Characteristics

## General Specifications

The Z feature grade does not support the enhanced nano features of Schmitt trigger input, Flash*Freeze bus hold, cold-sparing, and hot-swap I/O capability. Refer to the ordering information in the *IGLOO nano Product Brief* for more information.

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

### Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

***Table 2-1 •*** **Absolute Maximum Ratings**

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| $V_{CC}$ | DC core supply voltage | –0.3 to 1.65 | V |
| $V_{JTAG}$ | JTAG DC voltage | –0.3 to 3.75 | V |
| $V_{PUMP}$ | Programming voltage | –0.3 to 3.75 | V |
| $V_{CCPLL}$ | Analog power supply (PLL) | –0.3 to 1.65 | V |
| $V_{CCI}$ | DC I/O buffer supply voltage | –0.3 to 3.75 | V |
| VI | I/O input voltage | –0.3 V to 3.6 V | V |
| $T_{STG}$ [2] | Storage temperature | –65 to +150 | °C |
| $T_J$ [2] | Junction temperature | +125 | °C |

*Notes:*

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-2, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

**Table 2-2 • Recommended Operating Conditions [1]**

| Symbol | Parameter | | Extended Commercial | Industrial | Units |
|---|---|---|---|---|---|
| $T_A$ | Ambient temperature | | –20 to +70 [2] | –40 to +85 [2] | °C |
| $T_J$ | Junction temperature | | –20 to + 85 [2] | –40 to +100 [2] | °C |
| $V_{CC}$ | 1.5 V DC core supply voltage[3] | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.2 V–1.5 V wide range core voltage[4] | | 1.14 to 1.575 | 1.14 to 1.575 | V |
| $V_{JTAG}$ | JTAG DC voltage | | 1.425 to 3.6 | 1.425 to 3.6 | V |
| $V_{PUMP}$ [5] | Programming voltage | Programming mode | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation | 0 to 3.45 | 0 to 3.45 | V |
| $V_{CCPLL}$ [6] | Analog power supply (PLL) | 1.5 V DC core supply voltage[3] | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | | 1.2 V–1.5 V wide range core supply voltage[4] | 1.14 to 1.575 | 1.14 to 1.575 | V |
| $V_{CCI}$ and VMV [7,9] | 1.2 V DC supply voltage [4] | | 1.14 to 1.26 | 1.14 to 1.26 | V |
| | 1.2 V DC wide range supply voltage [4] | | 1.14 to 1.575 | 1.14 to 1.575 | V |
| | 1.5 V DC supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | |
| | 1.8 V DC supply voltage | | 1.7 to 1.9 | 1.7 to 1.9 | V |
| | 2.5 V DC supply voltage | | 2.3 to 2.7 | 2.3 to 2.7 | V |
| | 3.3 V DC supply voltage | | 3.0 to 3.6 | 3.0 to 3.6 | V |
| | 3.3 V DC wide range supply voltage [8] | | 2.7 to 3.6 | 2.7 to 3.6 | |

*Notes:*

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *To ensure targeted reliability standards are met across ambient and junction operating temperatures, Actel recommends that the user follow best design practices using Actel's timing and power simulation tools.*
3. *For IGLOO® nano V5 devices*
4. *For IGLOO nano V2 devices only, operating at $V_{CCI} \geq V_{CC}$*
5. *$V_{PUMP}$ can be left floating during operation (not programming mode).*
6. *$V_{CCPLL}$ pins should be tied to $V_{CC}$ pins. See Pin Descriptions for further information.*
7. *VMV pins must be connected to the corresponding $V_{CCI}$ pins. See Pin Descriptions for further information.*
8. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V $V_{CCI}$ operation.*
9. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-20 on page 2-19. $V_{CCI}$ should be at the same voltage within a given I/O bank.*

**Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature[1]**

| Product Grade | Programming Cycles | Program Retention (biased/unbiased) | Maximum Storage Temperature $T_{STG}$ (°C) [2] | Maximum Operating Junction Temperature $T_J$ (°C) [2] |
|---|---|---|---|---|
| Commercial | 500 | 20 years | 110 | 100 |
| Industrial | 500 | 20 years | 110 | 100 |

*Notes:*

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

*Table 2-4 •* **Overshoot and Undershoot Limits** [1]

| $V_{CCI}$ | Average $V_{CCI}$–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2] | Maximum Overshoot/ Undershoot[2] |
|---|---|---|
| 2.7 V or less | 10% | 1.4 V |
| | 5% | 1.49 V |
| 3 V | 10% | 1.1 V |
| | 5% | 1.19 V |
| 3.3 V | 10% | 0.79 V |
| | 5% | 0.88 V |
| 3.6 V | 10% | 0.45 V |
| | 5% | 0.54 V |

*Notes:*

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*

## I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO nano device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

IGLOO nano I/Os are activated only if ALL of the following three conditions are met:

1. $V_{CC}$ and $V_{CCI}$ are above the minimum specified trip points (Figure 2-1 and Figure 2-2 on page 2-5).
2. $V_{CCI} > V_{CC} - 0.75$ V (typical)
3. Chip is in the operating mode.

**$V_{CCI}$ Trip Point:**
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.2 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.1 V
Ramping up (V2 devices): 0.75 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.65 V < trip_point_down < 0.95 V

**$V_{CC}$ Trip Point:**
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.1 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.0 V
Ramping up (V2 devices): 0.65 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.55 V < trip_point_down < 0.95 V

$V_{CC}$ and $V_{CCI}$ ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to $V_{CCI}$.
- JTAG supply, PLL power supplies, and charge pump $V_{PUMP}$ supply have no influence on I/O behavior.

## *PLL Behavior at Brownout Condition*

Actel recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until $V_{CC}$ and $V_{CCPLX}$ exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or $V_{CC}$ levels drop below the $V_{CC}$ brownout levels (0.75 V ± 0.25 V for V5 devices, and 0.75 V ± 0.2 V for V2 devices), the PLL output lock signal goes LOW and/or the output clock is lost. Refer to the "Brownout Voltage" section in the *Power-Up/-Down Behavior of Low-Power Flash Devices* chapter of the *ProASIC3* and *ProASIC3E* handbooks for information on clock and lock recovery.

## *Internal Power-Up Activation Sequence*

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

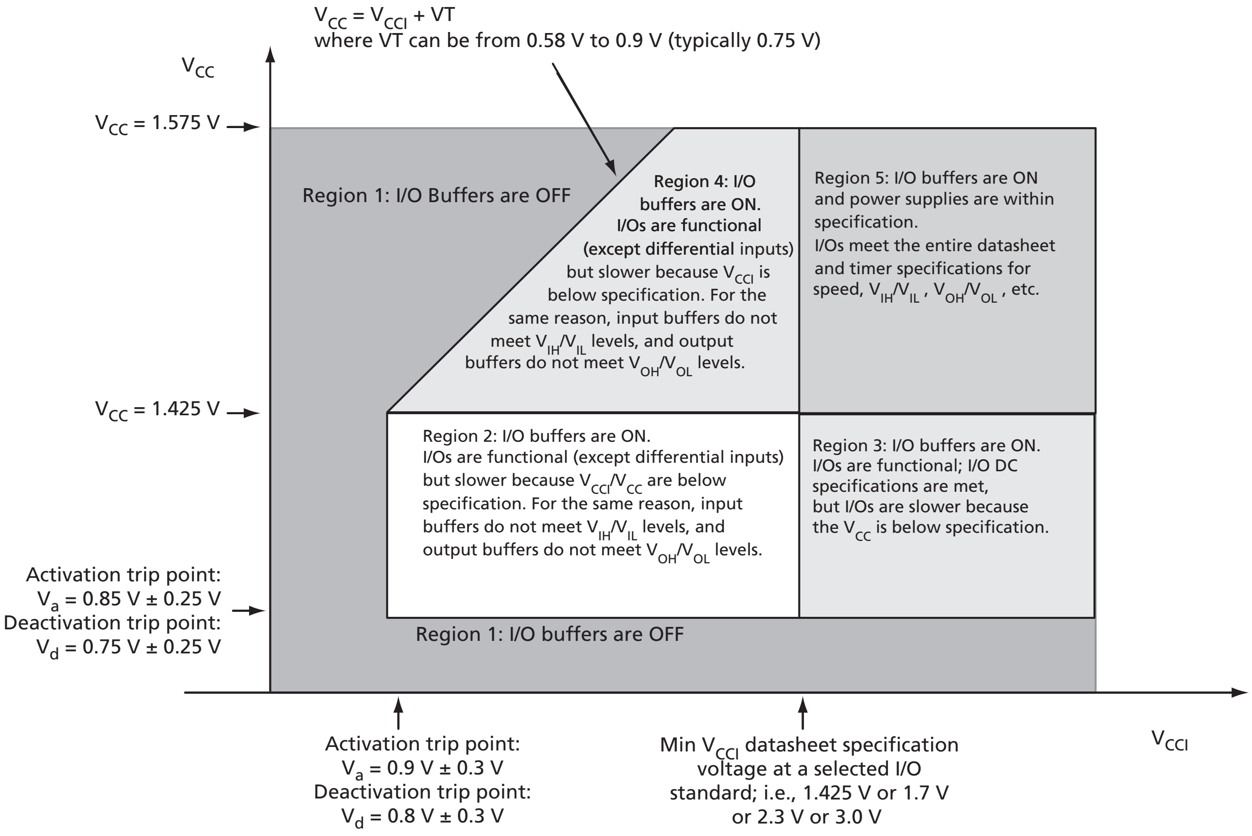


***Figure 2-1 •*** **V5 Devices – I/O State as a Function of $V_{CCI}$ and $V_{CC}$ Voltage Levels**

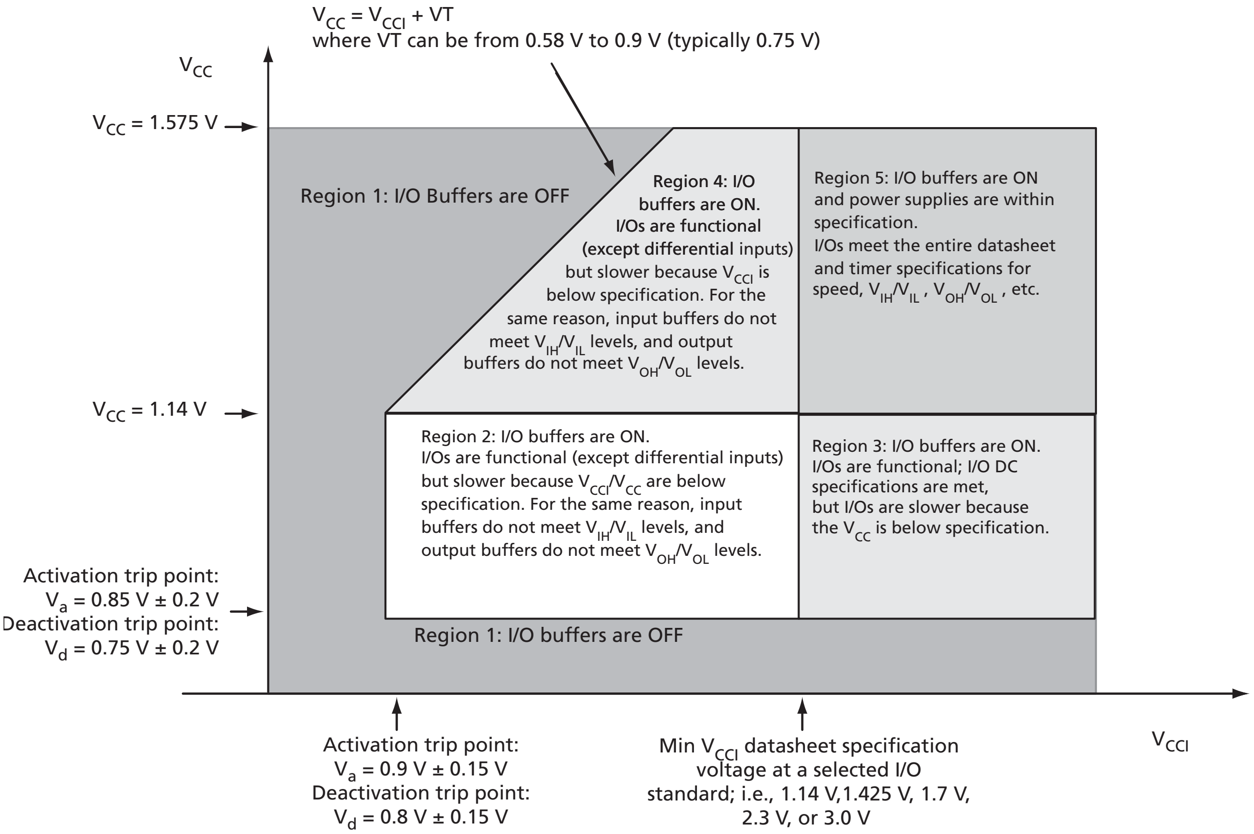


*Figure 2-2 •* **V2 Devices – I/O State as a Function of $V_{CCI}$ and $V_{CC}$ Voltage Levels**

# Thermal Characteristics

## Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 2-1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 2-1

where:

$T_A$ = Ambient temperature

$\Delta T$ = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

$\theta_{ja}$ = Junction-to-ambient of the package. $\theta_{ja}$ numbers are located in Figure 2-5.

P = Power dissipation

## Package Thermal Characteristics

The device junction-to-case thermal resistivity is $\theta_{jc}$ and the junction-to-ambient air thermal resistivity is $\theta_{ja}$. The thermal characteristics for $\theta_{ja}$ are shown for two air flow rates. The maximum operating junction temperature is 100°C. EQ 2-2 shows a sample calculation of the maximum operating power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. }(^\circ\text{C}) - \text{Max. ambient temp. }(^\circ\text{C})}{\theta_{ja}(^\circ\text{C/W})} = \frac{100^\circ\text{C} - 70^\circ\text{C}}{20.5^\circ\text{C/W}} = 1.46\text{ W}$$

EQ 2-2

*Table 2-5 •* **Package Thermal Resistivities**

| Package Type | Pin Count | $\theta_{jc}$ | $\theta_{ja}$ | | | Units |
|---|---|---|---|---|---|---|
| | | | Still Air | 200 ft./ min. | 500 ft./ min. | |
| Chip Scale Package (CSP) | 36 | TBD | TBD | TBD | TBD | C/W |
| | 81 | TBD | TBD | TBD | TBD | C/W |
| Quad Flat No Lead (QFN) | 48 | TBD | TBD | TBD | TBD | C/W |
| | 68 | TBD | TBD | TBD | TBD | C/W |
| | 100 | TBD | TBD | TBD | TBD | C/W |
| Very Thin Quad Flat Pack (VQFP) | 100 | 10.0 | 35.3 | 29.4 | 27.1 | C/W |

## Temperature and Voltage Derating Factors

*Table 2-6 •* **Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J$ = 70°C, $V_{CC}$ = 1.425 V)**
**For IGLOO nano V2 or V5 Devices, 1.5 V DC Core Supply Voltage**

| Array Voltage $V_{CC}$ (V) | Junction Temperature (°C) | | | | | | |
|---|---|---|---|---|---|---|---|
| | –40°C | –20°C | 0°C | 25°C | 70°C | 85°C | 125°C |
| 1.425 | 0.966 | 0.972 | 0.977 | 0.991 | 1.000 | 1.006 | 1.013 |
| 1.5 | 0.877 | 0.882 | 0.888 | 0.899 | 0.907 | 0.913 | 0.919 |
| 1.575 | 0.815 | 0.820 | 0.824 | 0.835 | 0.843 | 0.848 | 0.854 |

*Table 2-7 •* **Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J$ = 70°C, $V_{CC}$ = 1.14 V)
For IGLOO nano V2, 1.2 V DC Core Supply Voltage**

| Array Voltage $V_{CC}$ (V) | Junction Temperature (°C) | | | | | | |
|---|---|---|---|---|---|---|---|
| | –40°C | –20°C | 0°C | 25°C | 70°C | 85°C | 110°C |
| 1.14 | 0.968 | 0.973 | 0.978 | 0.991 | 1.000 | 1.006 | 1.012 |
| 1.2 | 0.863 | 0.869 | 0.874 | 0.885 | 0.892 | 0.898 | 0.904 |
| 1.26 | 0.793 | 0.798 | 0.802 | 0.812 | 0.820 | 0.825 | 0.830 |
| 1.3 | 0.746 | 0.750 | 0.754 | 0.764 | 0.771 | 0.776 | 0.781 |
| 1.35 | 0.690 | 0.694 | 0.698 | 0.707 | 0.714 | 0.718 | 0.723 |
| 1.425 | 0.615 | 0.618 | 0.622 | 0.630 | 0.636 | 0.640 | 0.644 |
| 1.5 | 0.558 | 0.561 | 0.565 | 0.572 | 0.577 | 0.581 | 0.585 |
| 1.575 | 0.519 | 0.522 | 0.525 | 0.532 | 0.536 | 0.540 | 0.543 |

# Calculating Power Dissipation

## Quiescent Supply Current

Quiescent supply current ($I_{DD}$) calculation depends on multiple factors, including operating voltages ($V_{CC}$, $V_{CCI}$, and $V_{JTAG}$), operating temperature, system clock frequency, and power mode usage. Actel recommends using the Power Calculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

*Table 2-8 •* **Quiescent Supply Current ($I_{DD}$) Characteristics, IGLOO nano Flash*Freeze Mode***

| | Core Voltage | AGLN010 | AGLN015 | AGLN020 | AGLN060 | AGLN125 | AGLN250 | Units |
|---|---|---|---|---|---|---|---|---|
| Typical (25°C) | 1.2 V | 1.7 | 3.3 | 3.3 | 8 | 13 | 20 | µA |
| | 1.5 V | 3 | 6 | 6 | 10 | 18 | 34 | µA |

* *$I_{DD}$ includes $V_{CC}$, $V_{PUMP}$, $V_{CCI}$, $V_{JTAG}$, and $V_{CCPLL}$ currents.*

*Table 2-9 •* **Quiescent Supply Current ($I_{DD}$) Characteristics, IGLOO nano Sleep Mode ($V_{CC}$ = 0 V)***

| | Core Voltage | AGLN010 | AGLN015 | AGLN020 | AGLN060 | AGLN125 | AGLN250 | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{CCI}/V_{JTAG}$ = 1.2 V (per bank) Typical (25°C) | 1.2 V | 1.7 | 1.7 | 1.7 | 1.7 | 1.7 | 1.7 | µA |
| $V_{CCI}/V_{JTAG}$ = 1.5 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | µA |
| $V_{CCI}/V_{JTAG}$ = 1.8 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 1.9 | 1.9 | 1.9 | 1.9 | 1.9 | 1.9 | µA |
| $V_{CCI}/V_{JTAG}$ = 2.5 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | µA |
| $V_{CCI}/V_{JTAG}$ = 3.3 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | µA |

* *$I_{DD}$ includes $V_{CC}$, $V_{PUMP}$, and $V_{CCPLL}$ currents.*

***Table 2-10 •*** **Quiescent Supply Current ($I_{DD}$) Characteristics, IGLOO nano Shutdown Mode ($V_{CC}$, $V_{CCI}$ = 0 V)***

| | Core Voltage | AGLN010 | AGLN015 | AGLN020 | AGLN060 | AGLN125 | AGLN250 | Units |
|---|---|---|---|---|---|---|---|---|
| Typical (25°C) | 1.2 V / 1.5 V | 0 | 0 | 0 | 0 | 0 | 0 | µA |

** $I_{DD}$ includes $V_{CC}$, $V_{PUMP}$, $V_{CCI}$, and $V_{CCPLL}$ currents.*

***Table 2-11 •*** **Quiescent Supply Current ($I_{DD}$), No IGLOO nano Flash*Freeze Mode**[1]

| | Core Voltage | AGLN010 | AGLN015 | AGLN020 | AGLN060 | AGLN125 | AGLN250 | Units |
|---|---|---|---|---|---|---|---|---|
| **$I_{CCA}$ Current**[2] | | | | | | | | |
| Typical (25°C) | 1.2 V | 3.7 | 5 | 5 | 10 | 13 | 18 | µA |
| | 1.5 V | 8 | 14 | 14 | 20 | 28 | 44 | µA |
| **$I_{CCI}$ or $I_{JTAG}$ Current**[3] | | | | | | | | |
| $V_{CCI}$ / $V_{JTAG}$ = 1.2 V (per bank) Typical (25°C) | 1.2 V | 1.7 | 1.7 | 1.7 | 1.7 | 1.7 | 1.7 | µA |
| $V_{CCI}$ / $V_{JTAG}$ = 1.5 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | µA |
| $V_{CCI}$ / $V_{JTAG}$ = 1.8 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 1.9 | 1.9 | 1.9 | 1.9 | 1.9 | 1.9 | µA |
| $V_{CCI}$ / $V_{JTAG}$ = 2.5 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | µA |
| $V_{CCI}$ / $V_{JTAG}$ = 3.3 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | µA |

*Notes:*

1. *To calculate total device $I_{DD}$, multiply the number of banks used by $I_{CCI}$ and add $I_{CCA}$ contribution.*
2. *Includes $V_{CC}$, $V_{CCPLL}$, and $V_{PUMP}$ currents.*
3. *Per $V_{CCI}$ or $V_{JTAG}$ bank*

## Power per I/O Pin

*Table 2-12 •* **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to IGLOO nano I/O Banks**

| | $V_{CCI}$ (V) | Dynamic Power $P_{AC9}$ (µW/MHz) [1] |
|---|---|---|
| **Single-Ended** | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 3.3 | 16.26 |
| 3.3 V LVTTL / 3.3 V LVCMOS – Schmitt Trigger | 3.3 | 18.95 |
| 2.5 V LVCMOS | 2.5 | 4.59 |
| 2.5 V LVCMOS – Schmitt Trigger | 2.5 | 6.01 |
| 1.8 V LVCMOS | 1.8 | 1.61 |
| 1.8 V LVCMOS – Schmitt Trigger | 1.8 | 1.70 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | 0.96 |
| 1.5 V LVCMOS (JESD8-11) – Schmitt Trigger | 1.5 | 0.90 |
| 1.2 V LVCMOS [2] | 1.2 | 0.55 |
| 1.2 V LVCMOS [2] – Schmitt Trigger | 1.2 | 0.47 |

*Notes:*

1. *$P_{AC9}$ is the total dynamic power measured on $V_{CCI}$.*
2. *Applicable to IGLOO nano V2 devices operating at $V_{CCI} \geq V_{CC}$.*

*Table 2-13 •* **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to IGLOO nano I/O Banks**

| | $C_{LOAD}$ (pF) | $V_{CCI}$ (V) | Dynamic Power $P_{AC10}$ (µW/MHz)[2] |
|---|---|---|---|
| **Single-Ended** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 5 | 3.3 | 107.98 |
| 2.5 V LVCMOS | 5 | 2.5 | 61.24 |
| 1.8 V LVCMOS | 5 | 1.8 | 31.28 |
| 1.5 V LVCMOS (JESD8-11) | 5 | 1.5 | 21.50 |
| 1.2 V LVCMOS[3] | 5 | 1.2 | 21.05 |

*Notes:*

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *$P_{AC10}$ is the total dynamic power measured on $V_{CCI}$.*
3. *Applicable for IGLOO nano V2 devices operating at $V_{CCI} \geq V_{CC}$.*

## Power Consumption of Various Internal Resources

*Table 2-14 •* **Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices For IGLOO nano V2 or V5 Devices, 1.5 V Core Supply Voltage**

| Parameter | Definition | Device Specific Dynamic Power (µW/MHz) | | | | | |
|---|---|---|---|---|---|---|---|
| | | AGLN250 | AGLN125 | AGLN060 | AGLN020 | AGLN015 | AGLN010 |
| $P_{AC1}$ | Clock contribution of a Global Rib | 11.03 | 11.03 | 9.3 | 9.3 | 9.3 | 9.3 |
| $P_{AC2}$ | Clock contribution of a Global Spine | 1.58 | 0.81 | 0.81 | 0.41 | 0.41 | 0.41 |
| $P_{AC3}$ | Clock contribution of a VersaTile row | 0.81 | | | | | |
| $P_{AC4}$ | Clock contribution of a VersaTile used as a sequential module | 0.11 | | | | | |
| $P_{AC5}$ | First contribution of a VersaTile used as a sequential module | 0.057 | | | | | |
| $P_{AC6}$ | Second contribution of a VersaTile used as a sequential module | 0.207 | | | | | |
| $P_{AC7}$ | Contribution of a VersaTile used as a combinatorial module | 0.17 | | | | | |
| $P_{AC8}$ | Average contribution of a routing net | 0.7 | | | | | |
| $P_{AC9}$ | Contribution of an I/O input pin (standard-dependent) | See Table 2-12 on page 2-9. | | | | | |
| $P_{AC10}$ | Contribution of an I/O output pin (standard-dependent) | See Table 2-13. | | | | | |
| $P_{AC11}$ | Average contribution of a RAM block during a read operation | 25.00 | | | N/A | | |
| $P_{AC12}$ | Average contribution of a RAM block during a write operation | 30.00 | | | N/A | | |
| $P_{AC13}$ | Dynamic contribution for PLL | 2.70 | | | N/A | | |

*Table 2-15 •* **Different Components Contributing to the Static Power Consumption in IGLOO nano Devices For IGLOO nano V2 or V5 Devices, 1.5 V Core Supply Voltage**

| Parameter | Definition | Device -Specific Static Power (mW) | | | | | |
|---|---|---|---|---|---|---|---|
| | | AGLN250 | AGLN125 | AGLN060 | AGLN020 | AGLN015 | AGLN010 |
| $P_{DC1}$ | Array static power in Active mode | See Table 2-11 on page 2-8 | | | | | |
| $P_{DC2}$ | Array static power in Static (Idle) mode | See Table 2-11 on page 2-8 | | | | | |
| $P_{DC3}$ | Array static power in Flash*Freeze mode | See Table 2-8 on page 2-7 | | | | | |
| $P_{DC4}$ [2] | Static PLL contribution | 1.84 | | | N/A | | |
| $P_{DC5}$ | Bank quiescent power ($V_{CCI}$-dependent) | See Table 2-11 on page 2-8 | | | | | |

*Notes:*

1. *For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or the SmartPower tool in Actel Libero® Integrated Design Environment (IDE).*
2. *Minimum contribution of the PLL when running at lowest frequency.*

*Table 2-16 •* **Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices For IGLOO nano V2 Devices, 1.2 V Core Supply Voltage**

| Parameter | Definition | Device-Specific Dynamic Power (µW/MHz) | | | | | |
|---|---|---|---|---|---|---|---|
| | | AGLN250 | AGLN125 | AGLN060 | AGLN020 | AGLN015 | AGLN010 |
| $P_{AC1}$ | Clock contribution of a Global Rib | 7.07 | 7.07 | 5.96 | 5.96 | 5.96 | 5.96 |
| $P_{AC2}$ | Clock contribution of a Global Spine | 1.01 | 0.52 | 0.52 | 0.26 | 0.26 | 0.26 |
| $P_{AC3}$ | Clock contribution of a VersaTile row | 0.52 | | | | | |
| $P_{AC4}$ | Clock contribution of a VersaTile used as a sequential module | 0.07 | | | | | |
| $P_{AC5}$ | First contribution of a VersaTile used as a sequential module | 0.045 | | | | | |
| $P_{AC6}$ | Second contribution of a VersaTile used as a sequential module | 0.186 | | | | | |
| $P_{AC7}$ | Contribution of a VersaTile used as a combinatorial module | 0.11 | | | | | |
| $P_{AC8}$ | Average contribution of a routing net | 0.45 | | | | | |
| $P_{AC9}$ | Contribution of an I/O input pin (standard-dependent) | See Table 2-12 on page 2-9 | | | | | |
| $P_{AC10}$ | Contribution of an I/O output pin (standard-dependent) | See Table 2-13 on page 2-9 | | | | | |
| $P_{AC11}$ | Average contribution of a RAM block during a read operation | 25.00 | | | N/A | | |
| $P_{AC12}$ | Average contribution of a RAM block during a write operation | 30.00 | | | N/A | | |
| $P_{AC13}$ | Dynamic contribution for PLL | 2.10 | | | N/A | | |

*Table 2-17 •* **Different Components Contributing to the Static Power Consumption in IGLOO nano Devices For IGLOO nano V2 Devices, 1.2 V Core Supply Voltage**

| Parameter | Definition | Device-Specific Static Power (mW) | | | | | |
|---|---|---|---|---|---|---|---|
| | | AGLN250 | AGLN125 | AGLN060 | AGLN020 | AGLN015 | AGLN010 |
| $P_{DC1}$ | Array static power in Active mode | See Table 2-11 on page 2-8 | | | | | |
| $P_{DC2}$ | Array static power in Static (Idle) mode | See Table 2-11 on page 2-8 | | | | | |
| $P_{DC3}$ | Array static power in Flash*Freeze mode | See Table 2-8 on page 2-7 | | | | | |
| $P_{DC4}$ [2] | Static PLL contribution | 0.90 | | | N/A | | |
| $P_{DC5}$ | Bank quiescent power ($V_{CCI}$-dependent) | See Table 2-11 on page 2-8 | | | | | |

*Notes:*

1. *For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or the SmartPower tool in Actel Libero IDE.*
2. *Minimum contribution of the PLL when running at lowest frequency.*

## Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Actel Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-18 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-19 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-19 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

### *Methodology*

#### Total Power Consumption—$P_{TOTAL}$

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

$P_{STAT}$ is the total static power consumption.

$P_{DYN}$ is the total dynamic power consumption.

#### Total Static Power Consumption—$P_{STAT}$

$$P_{STAT} = (P_{DC1} \text{ or } P_{DC2} \text{ or } P_{DC3}) + N_{BANKS} * P_{DC5}$$

$N_{BANKS}$ is the number of I/O banks powered in the design.

#### Total Dynamic Power Consumption—$P_{DYN}$

$$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

#### Global Clock Contribution—$P_{CLOCK}$

$$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$$

$N_{SPINE}$ is the number of global spines used in the user design—guidelines are provided in Table 2-18 on page 2-14.

$N_{ROW}$ is the number of VersaTile rows used in the design—guidelines are provided in Table 2-18 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$P_{AC1}$, $P_{AC2}$, $P_{AC3}$, and $P_{AC4}$ are device-dependent.

#### Sequential Cells Contribution—$P_{S\text{-}CELL}$

$$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-18 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-18 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### Routing Net Contribution—$P_{NET}$

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-18 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### I/O Input Buffer Contribution—$P_{INPUTS}$

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 2-18 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 2-18 on page 2-14.

$\beta_1$ is the I/O buffer enable rate—guidelines are provided in Table 2-19 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### RAM Contribution—$P_{MEMORY}$

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

$N_{BLOCKS}$ is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

$\beta_2$ is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

$\beta_3$ is the RAM enable rate for write operations—guidelines are provided in Table 2-19 on page 2-14.

### PLL Contribution—$P_{PLL}$

$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$

$F_{CLKOUT}$ is the output clock frequency.[1]

---

[1] *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

## Guidelines

### Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

### Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

*Table 2-18 •* **Toggle Rate Guidelines Recommended for Power Calculation**

| Component | Definition | Guideline |
|---|---|---|
| $\alpha_1$ | Toggle rate of VersaTile outputs | 10% |
| $\alpha_2$ | I/O buffer toggle rate | 10% |

*Table 2-19 •* **Enable Rate Guidelines Recommended for Power Calculation**

| Component | Definition | Guideline |
|---|---|---|
| $\beta_1$ | I/O output buffer enable rate | 100% |
| $\beta_2$ | RAM enable rate for read operations | 12.5% |
| $\beta_3$ | RAM enable rate for write operations | 12.5% |

# User I/O Characteristics

## Timing Model

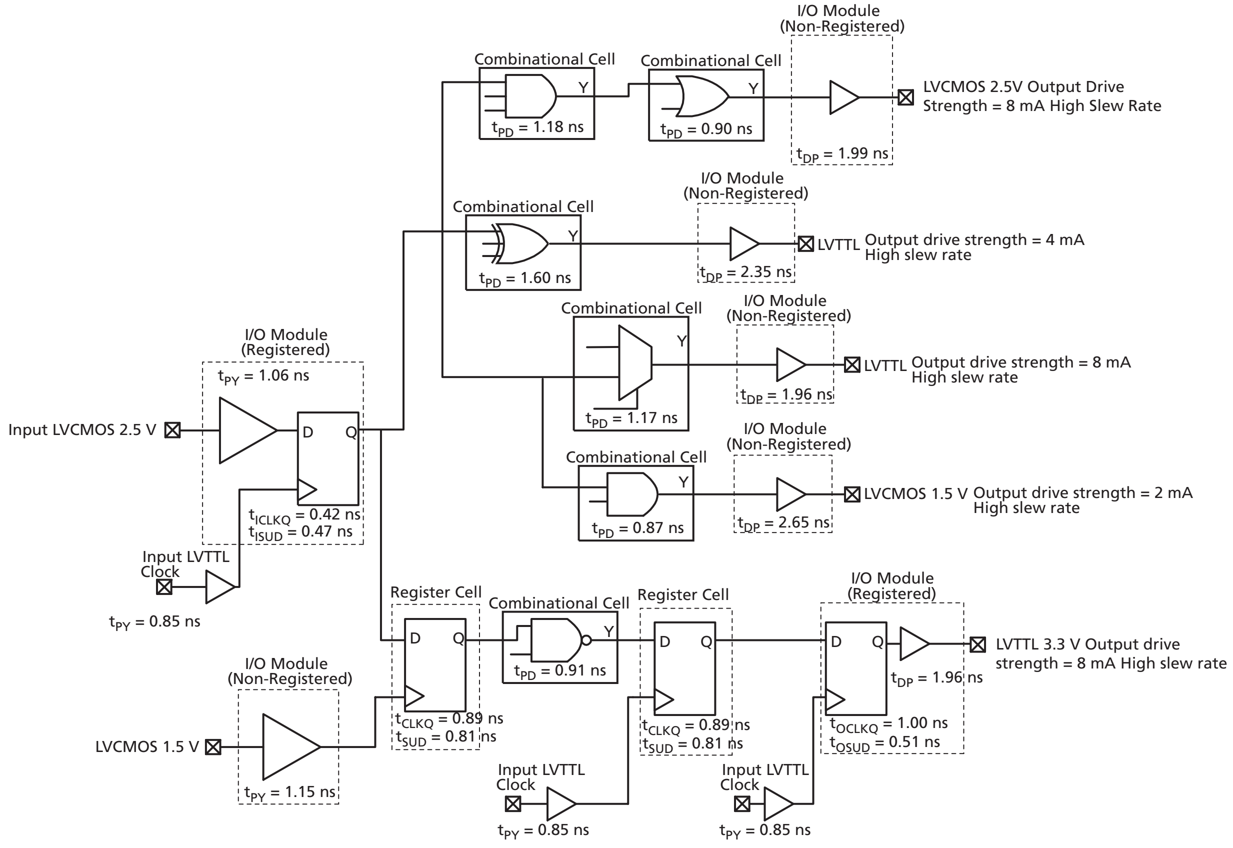


*Figure 2-3* • **Timing Model**
**Operating Conditions: STD Speed, Commercial Temperature Range ($T_J$ = 70°C), Worst-Case $V_{CC}$ = 1.425 V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices**

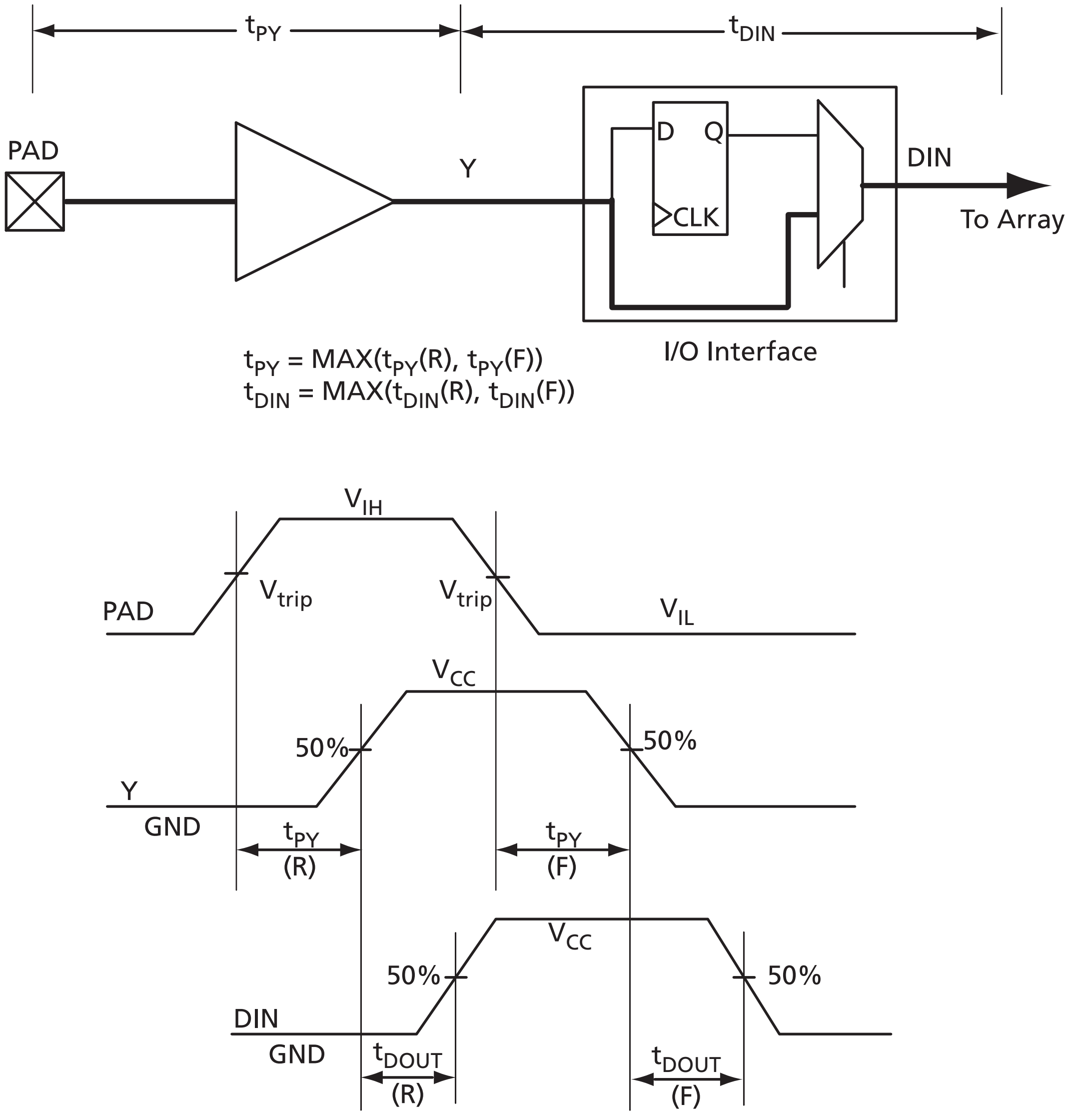


*Figure 2-4 •* **Input Buffer Timing Model and Delays (example)**

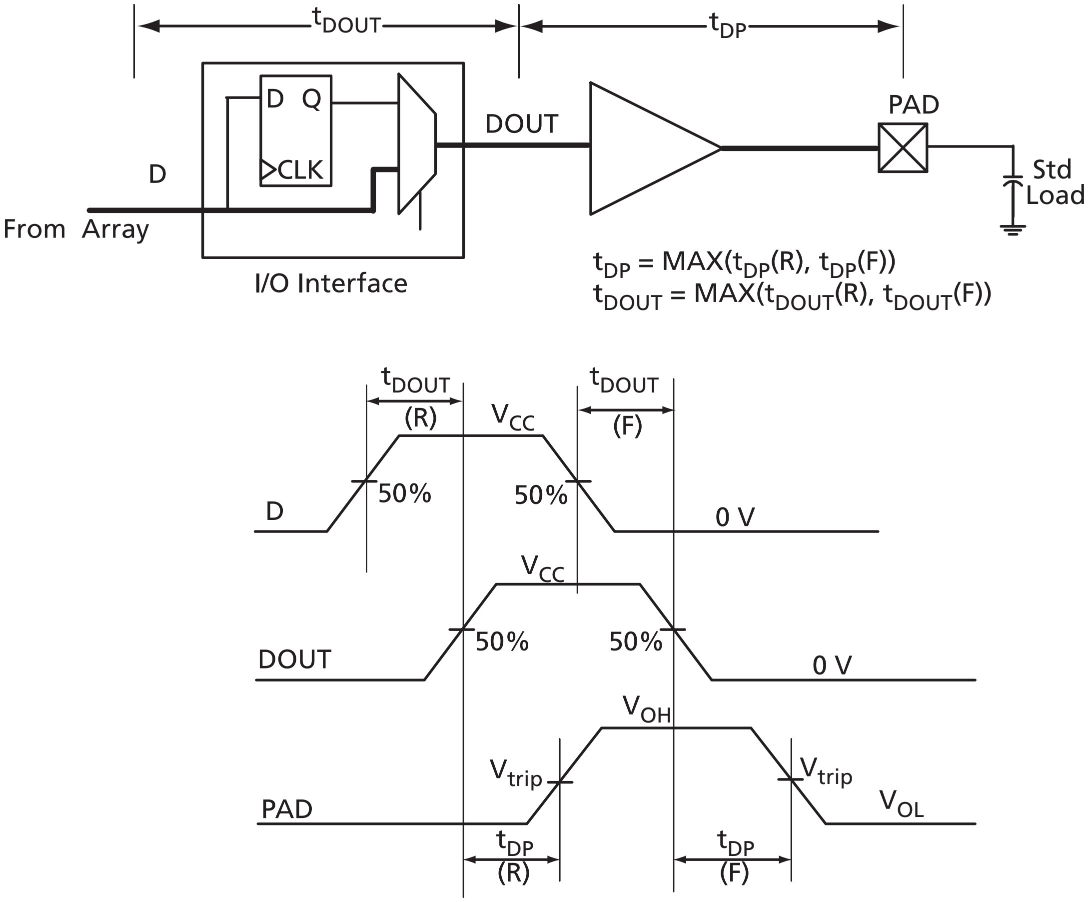


*Figure 2-5 •* **Output Buffer Model and Delays (example)**

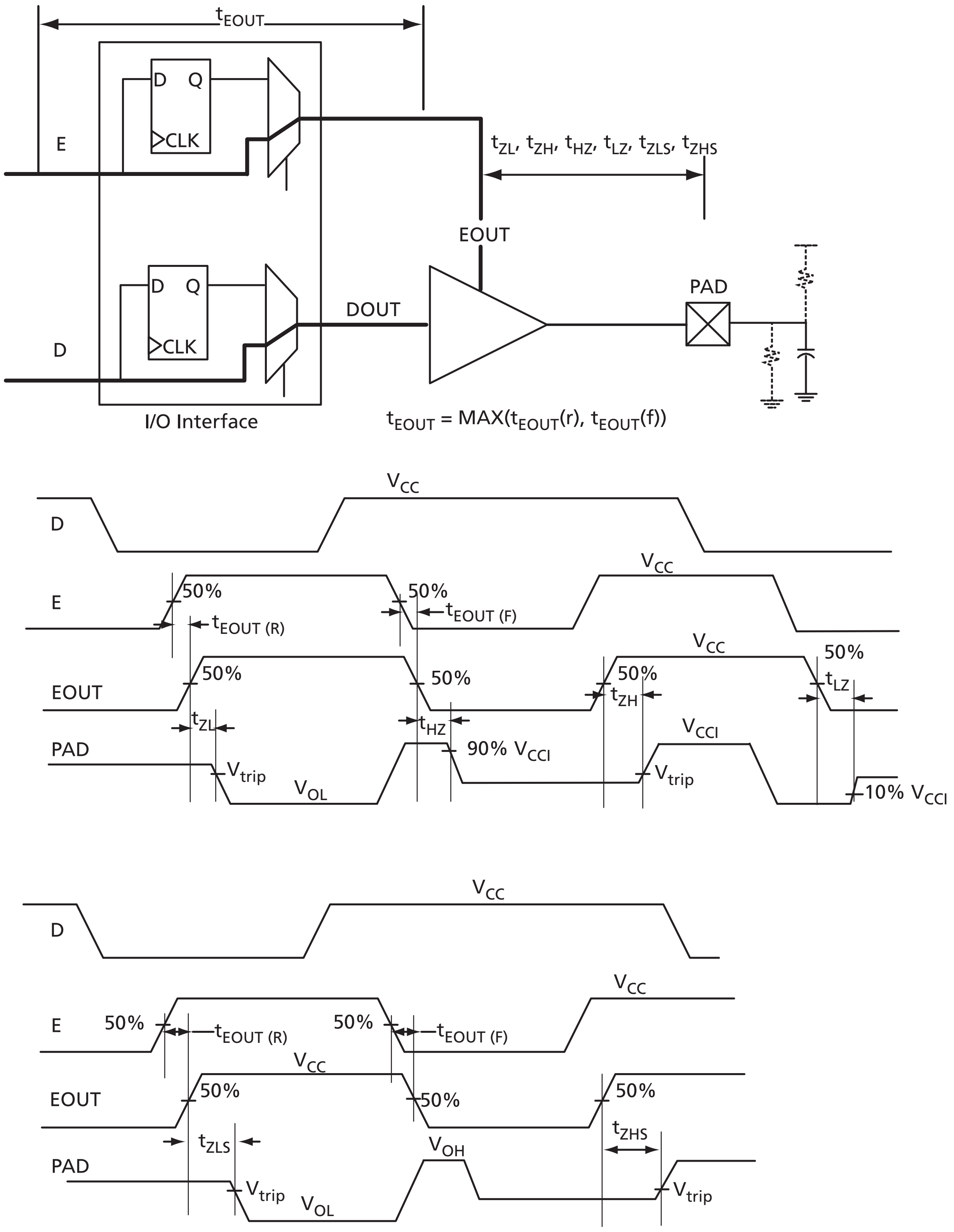


***Figure 2-6 •*** **Tristate Output Buffer Timing Model and Delays (example)**

## Overview of I/O Performance

### Summary of I/O DC Input and Output Levels – Default I/O Software Settings

*Table 2-20* • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings**

| I/O Standard | Drive Strength | Slew Rate | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ [1] | $I_{OH}$ [1] |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min, V | Max, V | Min, V | Max, V | Max, V | Min, V | mA | mA |
| 3.3 V LVTTL / 3.3 V LVCMOS | 8 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 |
| 3.3 V Wide Range | Any [2] | High | –0.3 | 0.8 | 2 | 3.6 | 0.2 | $V_{CCI}$ – 0.2 | 100 µA | 100 µA |
| 2.5 V LVCMOS | 8 mA | High | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 |
| 1.8 V LVCMOS | 4 mA | High | –0.3 | 0.35 * $V_{CCI}$ | 0.65 * $V_{CCI}$ | 3.6 | 0.45 | $V_{CCI}$ – 0.45 | 4 | 4 |
| 1.5 V LVCMOS | 2 mA | High | –0.3 | 0.35 * $V_{CCI}$ | 0.65 * $V_{CCI}$ | 3.6 | 0.25 * $V_{CCI}$ | 0.75 * $V_{CCI}$ | 2 | 2 |
| 1.2 V LVCMOS [3] | 1 mA | High | –0.3 | 0.35 * $V_{CCI}$ | 0.65 * $V_{CCI}$ | 3.6 | 0.25 * $V_{CCI}$ | 0.75 * $V_{CCI}$ | 1 | 1 |
| 1.2 V LVCMOS Wide Range [3] | Any [4] | High | –0.3 | 0.3 * $V_{CCI}$ | 0.7 * $V_{CCI}$ | 3.6 | 0.1 | $V_{CCI}$ – 0.1 | 100 µA | 100 µA |

*Notes:*

1. *Currents are measured at 85°C junction temperature.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification.*
3. *Applicable to IGLOO nano V2 devices operating at $V_{CCI} \geq V_{CC}$.*
4. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range, as specified in the JESD8-12 specification.*

*Table 2-21* • **Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions**

| DC I/O Standards | Commercial [1] | | Industrial [2] | |
|---|---|---|---|---|
| | $I_{IL}$ [3] | $I_{IH}$ [4] | $I_{IL}$ [3] | $I_{IH}$ [4] |
| | µA | µA | µA | µA |
| 3.3 V LVTTL / 3.3 V LVCMOS | 10 | 10 | 15 | 15 |
| 3.3 V LVCOMS Wide Range | 10 | 10 | 15 | 15 |
| 2.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.8 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.2 V LVCMOS [5] | 10 | 10 | 15 | 15 |
| 1.2 V LVCMOS Wide Range [5] | 10 | 10 | 15 | 15 |

*Notes:*

1. *Commercial range ($-20°C < T_A < 70°C$)*
2. *Industrial range ($-40°C < T_A < 85°C$)*
3. *$I_{IH}$ is the input leakage current per I/O pin over recommended operating conditions, where $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.*
4. *$I_{IL}$ is the input leakage current per I/O pin over recommended operating conditions, where $-0.3\ V < V_{IN} < V_{IL}$.*
5. *Applicable to IGLOO nano V2 devices operating at $V_{CCI} \geq V_{CC}$.*

## Summary of I/O Timing Characteristics – Default I/O Software Settings

*Table 2-22 •* **Summary of AC Measuring Points**

| Standard | Measuring Trip Point ($V_{trip}$) |
|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 1.4 V |
| 3.3 V LVCMOS Wide Range | 1.4 V |
| 2.5 V LVCMOS | 1.2 V |
| 1.8 V LVCMOS | 0.90 V |
| 1.5 V LVCMOS | 0.75 V |
| 1.2 V LVCMOS | 0.60 V |
| 1.2 V LVCMOS Wide Range | 0.60 V |

*Table 2-23 •* **I/O AC Parameter Definitions**

| Parameter | Parameter Definition |
|---|---|
| $t_{DP}$ | Data to Pad delay through the Output Buffer |
| $t_{PY}$ | Pad to Data delay through the Input Buffer |
| $t_{DOUT}$ | Data to Output Buffer delay through the I/O interface |
| $t_{EOUT}$ | Enable to Output Buffer Tristate Control delay through the I/O interface |
| $t_{DIN}$ | Input Buffer to Data delay through the I/O interface |
| $t_{HZ}$ | Enable to Pad delay through the Output Buffer—HIGH to Z |
| $t_{ZH}$ | Enable to Pad delay through the Output Buffer—Z to HIGH |
| $t_{LZ}$ | Enable to Pad delay through the Output Buffer—LOW to Z |
| $t_{ZL}$ | Enable to Pad delay through the Output Buffer—Z to LOW |
| $t_{ZHS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH |
| $t_{ZLS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW |

### Applies to IGLOO nano at 1.5 V Core Operating Conditions

***Table 2-24 •*** **Summary of I/O Timing Characteristics—Software Default Settings**
**STD Speed Grade, Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V,**
**Worst-Case $V_{CCI}$ = 3.0 V**

| I/O Standard | Drive Strength (mA) | Slew Rate | Capacitive Load (pF) | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 8 mA | High | 5 pF | 0.97 | 1.96 | 0.19 | 0.85 | 1.14 | 0.66 | 1.73 | 1.32 | 2.04 | 2.38 | ns |
| 3.3 V LVCMOS Wide Range | Any [1] | High | 5 pF | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD |
| 2.5 V LVCMOS | 8 mA | High | 5 pF | 0.97 | 1.99 | 0.19 | 1.06 | 1.22 | 0.66 | 1.76 | 1.42 | 2.04 | 2.25 | ns |
| 1.8 V LVCMOS | 4 mA | High | 5 pF | 0.97 | 2.30 | 0.19 | 0.99 | 1.43 | 0.66 | 2.01 | 1.64 | 2.08 | 2.15 | ns |
| 1.5 V LVCMOS | 2 mA | High | 5 pF | 0.97 | 2.65 | 0.19 | 1.15 | 1.62 | 0.66 | 2.31 | 1.85 | 2.13 | 2.11 | ns |

*Notes:*

1. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### Applies to IGLOO nano at 1.2 V Core Operating Conditions

***Table 2-25 •*** **Summary of I/O Timing Characteristics—Software Default Settings**
**STD Speed Grade, Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V,**
**Worst-Case $V_{CCI}$ = 3.0 V**

| I/O Standard | Drive Strength (mA) | Slew Rate | Capacitive Load (pF) | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY)}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 8 mA | High | 5 pF | 1.55 | 2.81 | 0.26 | 0.99 | 1.14 | 1.10 | 2.53 | 2.01 | 2.48 | 3.10 | ns |
| 3.3 V LVCMOS Wide Range | Any [1] | High | 5 pF | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | ns |
| 2.5 V LVCMOS | 8 mA | High | 5 pF | 1.55 | 2.82 | 0.26 | 1.20 | 1.22 | 1.10 | 2.53 | 2.15 | 2.46 | 2.93 | ns |
| 1.8 V LVCMOS | 4 mA | High | 5 pF | 1.55 | 3.11 | 0.26 | 1.12 | 1.43 | 1.10 | 2.76 | 2.46 | 2.49 | 2.75 | ns |
| 1.5 V LVCMOS | 2 mA | High | 5 pF | 1.55 | 3.50 | 0.26 | 1.26 | 1.62 | 1.10 | 3.09 | 2.76 | 2.53 | 2.67 | ns |
| 1.2 V LVCMOS | 1 mA | High | 5 pF | 1.55 | 4.47 | 0.26 | 1.56 | 1.66 | 1.10 | 3.56 | 3.18 | 3.00 | 3.25 | ns |
| 1.2 V LVCMOS Wide Range | 100 µA | High | 5 pF | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | ns |

*Notes:*

1. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Detailed I/O DC Characteristics

***Table 2-26 •*** **Input Capacitance**

| Symbol | Definition | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN} = 0$, f = 1.0 MHz |  | 8 | pF |
| $C_{INCLK}$ | Input capacitance on the clock pin | $V_{IN} = 0$, f = 1.0 MHz |  | 8 | pF |

***Table 2-27 •*** **I/O Output Buffer Maximum Resistances** [1]

| Standard | Drive Strength | $R_{PULL-DOWN}$ $(\Omega)^2$ | $R_{PULL-UP}$ $(\Omega)^3$ |
|---|---|---|---|
| 3.3 V LVTTL / 3.3V LVCMOS | 2 mA | 100 | 300 |
|  | 4 mA | 100 | 300 |
|  | 6 mA | 50 | 150 |
|  | 8 mA | 50 | 150 |
| 3.3 V LVCMOS Wide Range | 100 µA | TBD | TBD |
| 2.5 V LVCMOS | 2 mA | 100 | 200 |
|  | 4 mA | 100 | 200 |
|  | 6 mA | 50 | 100 |
|  | 8 mA | 50 | 100 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
|  | 4 mA | 100 | 112 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| 1.2 V LVCMOS [4] | 2 mA | TBD | TBD |
| 1.2 V LVCMOS Wide Range [4] | 100 µA | TBD | TBD |

*Notes:*

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on $V_{CCI}$, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/download/ibis/default.aspx.*
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$
4. *Applicable to IGLOO nano V2 devices operating at $V_{CCI} \geq V_{CC}$.*

*Table 2-28 •* **I/O Weak Pull-Up/Pull-Down Resistances**
**Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

| $V_{CCI}$ | $R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω) | | $R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω) | |
|---|---|---|---|---|
| | **Min.** | **Max.** | **Min.** | **Max.** |
| 3.3 V | 10 k | 45 k | 10 k | 45 k |
| 2.5 V | 11 k | 55 k | 12 k | 74 k |
| 1.8 V | 18 k | 70 k | 17 k | 110 k |
| 1.5 V | 19 k | 90 k | 19 k | 140 k |
| 1.2 V | 25 k | 110 k | 25 k | 150 k |

*Notes:*

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (V_{OLspec}) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$

*Table 2-29 •* **I/O Short Currents $I_{OSH}/I_{OSL}$**

| | **Drive Strength** | **$I_{OSL}$ (mA)*** | **$I_{OSH}$ (mA)*** |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| 3.3 V LVCMOS Wide Range | 100 µA | TBD | TBD |
| 2.5 V LVCMOS | 2 mA | 16 | 18 |
| | 4 mA | 16 | 18 |
| | 6 mA | 32 | 37 |
| | 8 mA | 32 | 37 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| 1.2 V LVCMOS | 1 mA | TBD | TBD |
| 1.2 V LVCMOS Wide Range | 100 µA | TBD | TBD |

* $T_J = 100°C$

The length of time an I/O can withstand $I_{OSH}/I_{OSL}$ events depends on the junction temperature. The reliability data below is based on a 3.3 V, 8 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

**Table 2-30 • Duration of Short Circuit Event before Failure**

| Temperature | Time before Failure |
|---|---|
| –40°C | > 20 years |
| –20°C | > 20 years |
| 0°C | > 20 years |
| 25°C | > 20 years |
| 70°C | 5 years |
| 85°C | 2 years |
| 100°C | 6 months |
| 110°C | 3 months |

**Table 2-31 • Schmitt Trigger Input Hysteresis**
**Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers**

| Input Buffer Configuration | Hysteresis Value (typ.) |
|---|---|
| 3.3 V LVTTL / LVCMOS (Schmitt trigger mode) | 240 mV |
| 2.5 V LVCMOS (Schmitt trigger mode) | 140 mV |
| 1.8 V LVCMOS (Schmitt trigger mode) | 80 mV |
| 1.5 V LVCMOS (Schmitt trigger mode) | 60 mV |
| 1.2 V LVCMOS (Schmitt trigger mode) | 40 mV |

**Table 2-32 • I/O Input Rise Time, Fall Time, and Related I/O Reliability**

| Input Buffer | Input Rise/Fall Time (min.) | Input Rise/Fall Time (max.) | Reliability |
|---|---|---|---|
| LVTTL/LVCMOS (Schmitt trigger disabled) | No requirement | 10 ns * | 20 years (100°C) |
| LVTTL/LVCMOS (Schmitt trigger enabled) | No requirement | No requirement, but input noise voltage cannot exceed Schmitt hysteresis. | 20 years (100°C) |

* *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

## Single-Ended I/O Characteristics

### 3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

***Table 2-33 •*** **Minimum and Maximum DC Input and Output Levels**

| 3.3 V LVTTL / 3.3 V LVCMOS | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ [1] | $I_{IH}$ [2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Drive Strength** | **Min., V** | **Max., V** | **Min., V** | **Max., V** | **Max., V** | **Min., V** | **mA** | **mA** | **Max., mA[3]** | **Max., mA[3]** | **µA[4]** | **µA[4]** |
| 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 25 | 27 | 10 | 10 |
| 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 25 | 27 | 10 | 10 |
| 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 51 | 54 | 10 | 10 |
| 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 51 | 54 | 10 | 10 |

*Notes:*

1. *$I_{IL}$ is the input leakage current per I/O pin over recommended operating conditions where $-0.3 < V_{IN} < V_{IL}$.*
2. *$I_{IH}$ is the input leakage current per I/O pin over recommended operating conditions where $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

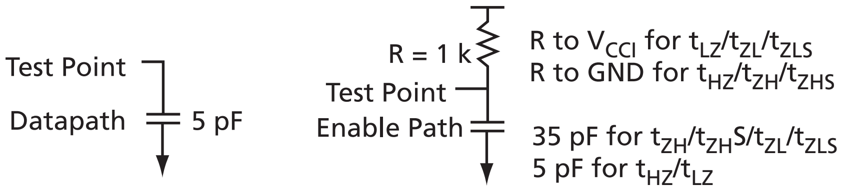


***Figure 2-7 •*** **AC Loading**

***Table 2-34 •*** **3.3 V LVTTL/LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 3.3 | 1.4 | 5 |

* *Measuring point = $V_{trip}$. See Table 2-22 on page 2-20 for a complete table of trip points.*

### Timing Characteristics

#### *Applies to 1.5 V DC Core Voltage*

***Table 2-35 •*** **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V, Worst-Case $V_{CCI}$ = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 3.94 | 0.19 | 0.85 | 1.14 | 0.66 | 3.39 | 2.95 | 1.82 | 1.87 | ns |
| 4 mA | STD | 0.97 | 3.94 | 0.19 | 0.85 | 1.14 | 0.66 | 3.39 | 2.95 | 1.82 | 1.87 | ns |
| 6 mA | STD | 0.97 | 3.20 | 0.19 | 0.85 | 1.14 | 0.66 | 2.88 | 2.65 | 2.04 | 2.27 | ns |
| 8 mA | STD | 0.97 | 3.20 | 0.19 | 0.85 | 1.14 | 0.66 | 2.88 | 2.65 | 2.04 | 2.27 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-36 •*** **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V, Worst-Case $V_{CCI}$ = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 2.35 | 0.19 | 0.85 | 1.14 | 0.66 | 1.88 | 1.43 | 1.81 | 1.98 | ns |
| 4 mA | STD | 0.97 | 2.35 | 0.19 | 0.85 | 1.14 | 0.66 | 1.88 | 1.43 | 1.81 | 1.98 | ns |
| 6 mA | STD | 0.97 | 1.96 | 0.19 | 0.85 | 1.14 | 0.66 | 1.73 | 1.32 | 2.04 | 2.38 | ns |
| 8 mA | STD | 0.97 | 1.96 | 0.19 | 0.85 | 1.14 | 0.66 | 1.73 | 1.32 | 2.04 | 2.38 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### *Applies to 1.2 V DC Core Voltage*

*Table 2-37 •* **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V, Worst-Case $V_{CCI}$ = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 5.23 | 0.26 | 0.99 | 1.14 | 1.10 | 4.56 | 3.93 | 2.25 | 2.56 | ns |
| 4 mA | STD | 1.55 | 5.23 | 0.26 | 0.99 | 1.14 | 1.10 | 4.56 | 3.93 | 2.25 | 2.56 | ns |
| 6 mA | STD | 1.55 | 4.21 | 0.26 | 0.99 | 1.14 | 1.10 | 3.81 | 3.42 | 2.48 | 2.97 | ns |
| 8 mA | STD | 1.55 | 4.21 | 0.26 | 0.99 | 1.14 | 1.10 | 3.81 | 3.42 | 2.48 | 2.97 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-38 •* **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V, Worst-Case $V_{CCI}$ = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 3.49 | 0.26 | 0.99 | 1.14 | 1.10 | 2.91 | 2.33 | 2.24 | 2.68 | ns |
| 4 mA | STD | 1.55 | 3.49 | 0.26 | 0.99 | 1.14 | 1.10 | 2.91 | 2.33 | 2.24 | 2.68 | ns |
| 6 mA | STD | 1.55 | 2.81 | 0.26 | 0.99 | 1.14 | 1.10 | 2.53 | 2.01 | 2.48 | 3.10 | ns |
| 8 mA | STD | 1.55 | 2.81 | 0.26 | 0.99 | 1.14 | 1.10 | 2.53 | 2.01 | 2.48 | 3.10 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## 3.3 V LVCOMOS Wide Range

*Table 2-39 •* **Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range**

| **3.3 V LVCMOS Wide Range** | **$V_{IL}$** | | **$V_{IH}$** | | **$V_{OL}$** | **$V_{OH}$** | **$I_{OL}$** | **$I_{OH}$** | **$I_{IL}$ [1]** | **$I_{IH}$ [2]** |
|---|---|---|---|---|---|---|---|---|---|---|
| **Drive Strength** | **Min., V** | **Max., V** | **Min., V** | **Max., V** | **Max., V** | **Min., V** | **µA** | **µA** | **µA [3]** | **µA [3]** |
| All [4] | –0.3 | 0.8 | 2 | 3.6 | 0.2 | $V_{DD}$ – 0.2 | 100 | 100 | 10 | 10 |

*Notes:*

1. *$I_{IL}$ is the input leakage current per I/O pin over recommended operating conditions where $-0.3 < V_{IN} < V_{IL}$.*
2. *$I_{IH}$ is the input leakage current per I/O pin over recommended operating conditions where $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at 85°C junction temperature.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V Wide Range, as specified in the JEDEC JESD8-B specification.*

## *2.5 V LVCMOS*

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 5 V–tolerant input buffer and push-pull output buffer.

***Table 2-40 •*** **Minimum and Maximum DC Input and Output Levels**

| 2.5 V LVCMOS | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ [1] | $I_{IH}$ [2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Drive Strength** | **Min., V** | **Max., V** | **Min., V** | **Max., V** | **Max., V** | **Min., V** | **mA** | **mA** | **Max., mA[3]** | **Max., mA[3]** | **µA[4]** | **µA[4]** |
| 2 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 2 | 2 | 16 | 18 | 10 | 10 |
| 4 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 16 | 18 | 10 | 10 |
| 6 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 6 | 6 | 32 | 37 | 10 | 10 |
| 8 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 32 | 37 | 10 | 10 |

*Notes:*

1. *$I_{IL}$ is the input leakage current per I/O pin over recommended operating conditions where $-0.3 < V_{IN} < V_{IL}$.*
2. *$I_{IH}$ is the input leakage current per I/O pin over recommended operating conditions where $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

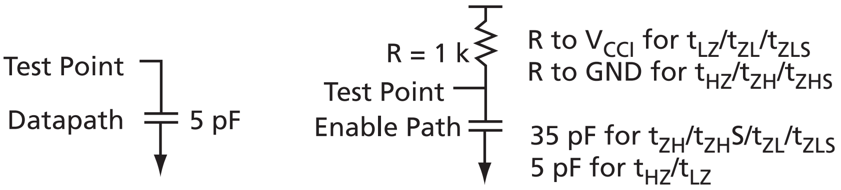


***Figure 2-8 •*** **AC Loading**

***Table 2-41 •*** **2.5 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 2.5 | 1.2 | 5 |

* *Measuring point = $V_{trip}$. See Table 2-22 on page 2-20 for a complete table of trip points.*

### Timing Characteristics

#### *Applies to 1.5 V DC Core Voltage*

*Table 2-42 •* **2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V, Worst-Case $V_{CCI}$ = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 4.44 | 0.19 | 1.06 | 1.22 | 0.66 | 3.87 | 3.47 | 1.80 | 1.70 | ns |
| 4 mA | STD | 0.97 | 4.44 | 0.19 | 1.06 | 1.22 | 0.66 | 3.87 | 3.47 | 1.80 | 1.70 | ns |
| 8 mA | STD | 0.97 | 3.61 | 0.19 | 1.06 | 1.22 | 0.66 | 3.27 | 3.11 | 2.05 | 2.17 | ns |
| 8 mA | STD | 0.97 | 3.61 | 0.19 | 1.06 | 1.22 | 0.66 | 3.27 | 3.11 | 2.05 | 2.17 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-43 •* **2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V, Worst-Case $V_{CCI}$ = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 2.41 | 0.19 | 1.06 | 1.22 | 0.66 | 1.93 | 1.57 | 1.79 | 1.77 | ns |
| 4 mA | STD | 0.97 | 2.41 | 0.19 | 1.06 | 1.22 | 0.66 | 1.93 | 1.57 | 1.79 | 1.77 | ns |
| 6 mA | STD | 0.97 | 1.99 | 0.19 | 1.06 | 1.22 | 0.66 | 1.76 | 1.42 | 2.04 | 2.25 | ns |
| 8 mA | STD | 0.97 | 1.99 | 0.19 | 1.06 | 1.22 | 0.66 | 1.76 | 1.42 | 2.04 | 2.25 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### *Applies to 1.2 V DC Core Voltage*

*Table 2-44 •* **2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V, Worst-Case $V_{CCI}$ = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 5.75 | 0.26 | 1.20 | 1.22 | 1.10 | 5.05 | 4.57 | 2.21 | 2.35 | ns |
| 4 mA | STD | 1.55 | 5.75 | 0.26 | 1.20 | 1.22 | 1.10 | 5.05 | 4.57 | 2.21 | 2.35 | ns |
| 6 mA | STD | 1.55 | 4.63 | 0.26 | 1.20 | 1.22 | 1.10 | 4.21 | 3.94 | 2.47 | 2.83 | ns |
| 8 mA | STD | 1.55 | 4.63 | 0.26 | 1.20 | 1.22 | 1.10 | 4.21 | 3.94 | 2.47 | 2.83 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-45 •* **2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V, Worst-Case $V_{CCI}$ = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 3.52 | 0.26 | 1.20 | 1.22 | 1.10 | 2.94 | 2.60 | 2.21 | 2.44 | ns |
| 4 mA | STD | 1.55 | 3.52 | 0.26 | 1.20 | 1.22 | 1.10 | 2.94 | 2.60 | 2.21 | 2.44 | ns |
| 6 mA | STD | 1.55 | 2.82 | 0.26 | 1.20 | 1.22 | 1.10 | 2.53 | 2.15 | 2.46 | 2.93 | ns |
| 8 mA | STD | 1.55 | 2.82 | 0.26 | 1.20 | 1.22 | 1.10 | 2.53 | 2.15 | 2.46 | 2.93 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## 1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

*Table 2-46* • **Minimum and Maximum DC Input and Output Levels**

| 1.8 V LVCMOS | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ [1] | $I_{IH}$ [2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA[3] | Max., mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * $V_{CCI}$ | 0.65 * $V_{CCI}$ | 3.6 | 0.45 | $V_{CCI}$ – 0.45 | 2 | 2 | 9 | 11 | 10 | 10 |
| 4 mA | –0.3 | 0.35 * $V_{CCI}$ | 0.65 * $V_{CCI}$ | 3.6 | 0.45 | $V_{CCI}$ – 0.45 | 4 | 4 | 17 | 22 | 10 | 10 |

*Notes:*

1. *$I_{IL}$ is the input leakage current per I/O pin over recommended operating conditions where $-0.3 < V_{IN} < V_{IL}$.*
2. *$I_{IH}$ is the input leakage current per I/O pin over recommended operating conditions where $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

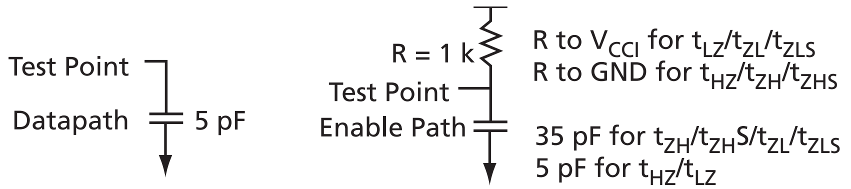


*Figure 2-9* • **AC Loading**

*Table 2-47* • **1.8 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 1.8 | 0.9 | 5 |

* *Measuring point = $V_{trip}$. See Table 2-22 on page 2-20 for a complete table of trip points.*

### Timing Characteristics

*Applies to 1.5 V DC Core Voltage*

*Table 2-48 •* **1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V, Worst-Case $V_{CCI}$ = 1.7 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 5.89 | 0.19 | 0.99 | 1.43 | 0.66 | 5.20 | 4.48 | 1.78 | 1.30 | ns |
| 4 mA | STD | 0.97 | 4.82 | 0.19 | 0.99 | 1.43 | 0.66 | 4.39 | 4.04 | 2.08 | 2.07 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-49 •* **1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V, Worst-Case $V_{CCI}$ = 1.7 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 2.82 | 0.19 | 0.99 | 1.43 | 0.66 | 2.25 | 1.86 | 1.78 | 1.35 | ns |
| 4 mA | STD | 0.97 | 2.30 | 0.19 | 0.99 | 1.43 | 0.66 | 2.01 | 1.64 | 2.08 | 2.15 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Applies to 1.2 V DC Core Voltage*

*Table 2-50 •* **1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V, Worst-Case $V_{CCI}$ = 1.7 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 7.30 | 0.26 | 1.12 | 1.43 | 1.10 | 6.45 | 5.82 | 2.18 | 1.87 | ns |
| 4 mA | STD | 1.55 | 5.88 | 0.26 | 1.12 | 1.43 | 1.10 | 5.35 | 4.98 | 2.49 | 2.67 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-51 •* **1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V, Worst-Case $V_{CCI}$ = 1.7 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 4.24 | 0.26 | 1.12 | 1.43 | 1.10 | 3.28 | 3.11 | 2.18 | 1.92 | ns |
| 4 mA | STD | 1.55 | 3.11 | 0.26 | 1.12 | 1.43 | 1.10 | 2.76 | 2.46 | 2.49 | 2.75 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

*Table 2-52 •* **Minimum and Maximum DC Input and Output Levels**

| 1.5 V LVCMOS | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$[1] | $I_{IH}$[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Drive Strength** | **Min., V** | **Max., V** | **Min., V** | **Max., V** | **Max., V** | **Min., V** | **mA** | **mA** | **Max., mA[3]** | **Max., mA[3]** | **µA[4]** | **µA[4]** |
| 2 mA | –0.3 | 0.35 * $V_{CCI}$ | 0.65 * $V_{CCI}$ | 3.6 | 0.25 * $V_{CCI}$ | 0.75 * $V_{CCI}$ | 2 | 2 | 13 | 16 | 10 | 10 |

*Notes:*

1. *$I_{IL}$ is the input leakage current per I/O pin over recommended operating conditions where $–0.3 < V_{IN} < V_{IL}$.*
2. *$I_{IH}$ is the input leakage current per I/O pin over recommended operating conditions where $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

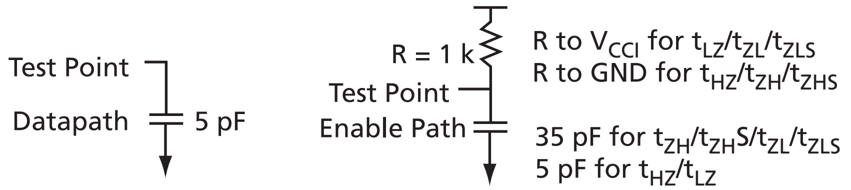


*Figure 2-10 •* **AC Loading**

*Table 2-53 •* **1.5 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 1.5 | 0.75 | 5 |

* *Measuring point = $V_{trip.}$ See Table 2-22 on page 2-20 for a complete table of trip points.*

### Timing Characteristics

#### *Applies to 1.5 V DC Core Voltage*

*Table 2-54* • **1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V, Worst-Case $V_{CCI}$ = 1.4 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 6.07 | 0.19 | 1.15 | 1.62 | 0.66 | 5.57 | 4.89 | 2.13 | 2.02 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-55* • **1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V, Worst-Case $V_{CCI}$ = 1.4 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 2.65 | 0.19 | 1.15 | 1.62 | 0.66 | 2.31 | 1.85 | 2.13 | 2.11 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

#### *Applies to 1.2 V DC Core Voltage*

*Table 2-56* • **1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V, Worst-Case $V_{CCI}$ = 1.4 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 7.23 | 0.26 | 1.26 | 1.62 | 1.10 | 6.61 | 5.94 | 2.53 | 2.58 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-57* • **1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V, Worst-Case $V_{CCI}$ = 1.4 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 3.50 | 0.26 | 1.26 | 1.62 | 1.10 | 3.09 | 2.76 | 2.53 | 2.67 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## 1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

**Table 2-58 • Minimum and Maximum DC Input and Output Levels**

| 1.2 V LVCMOS | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$[1] | $I_{IH}$[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA[3] | Max., mA[3] | µA[4] | µA[4] |
| 1 mA | –0.3 | 0.35 * $V_{CCI}$ | 0.65 * $V_{CCI}$ | 3.6 | 0.25 * $V_{CCI}$ | 0.75 * $V_{CCI}$ | 1 | 1 | TBD | TBD | 10 | 10 |

*Notes:*

1. *$I_{IL}$ is the input leakage current per I/O pin over recommended operating conditions where $-0.3 < V_{IN} < V_{IL}$.*
2. *$I_{IH}$ is the input leakage current per I/O pin over recommended operating conditions where $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

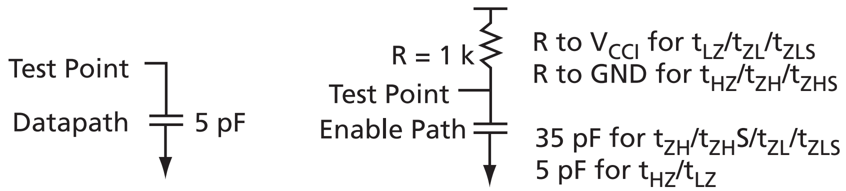


***Figure 2-11*** **• AC Loading**

**Table 2-59 • 1.2 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 1.2 | 0.6 | 5 |

* *Measuring point = $V_{trip}$. See Table 2-22 on page 2-20 for a complete table of trip points.*

### Timing Characteristics

#### *Applies to 1.2 V DC Core Voltage*

***Table 2-60*** **• 1.2 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V, Worst-Case $V_{CCI}$ = 1.14 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 mA | STD | 1.55 | 10.33 | 0.26 | 1.56 | 1.66 | 1.10 | 8.52 | 7.30 | 3.00 | 3.12 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-61*** **• 1.2 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V, Worst-Case $V_{CCI}$ = 1.14 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 mA | STD | 1.55 | 4.47 | 0.26 | 1.56 | 1.66 | 1.10 | 3.56 | 3.18 | 3.00 | 3.25 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## I/O Register Specifications

### Fully Registered I/O Buffers with Asynchronous Preset

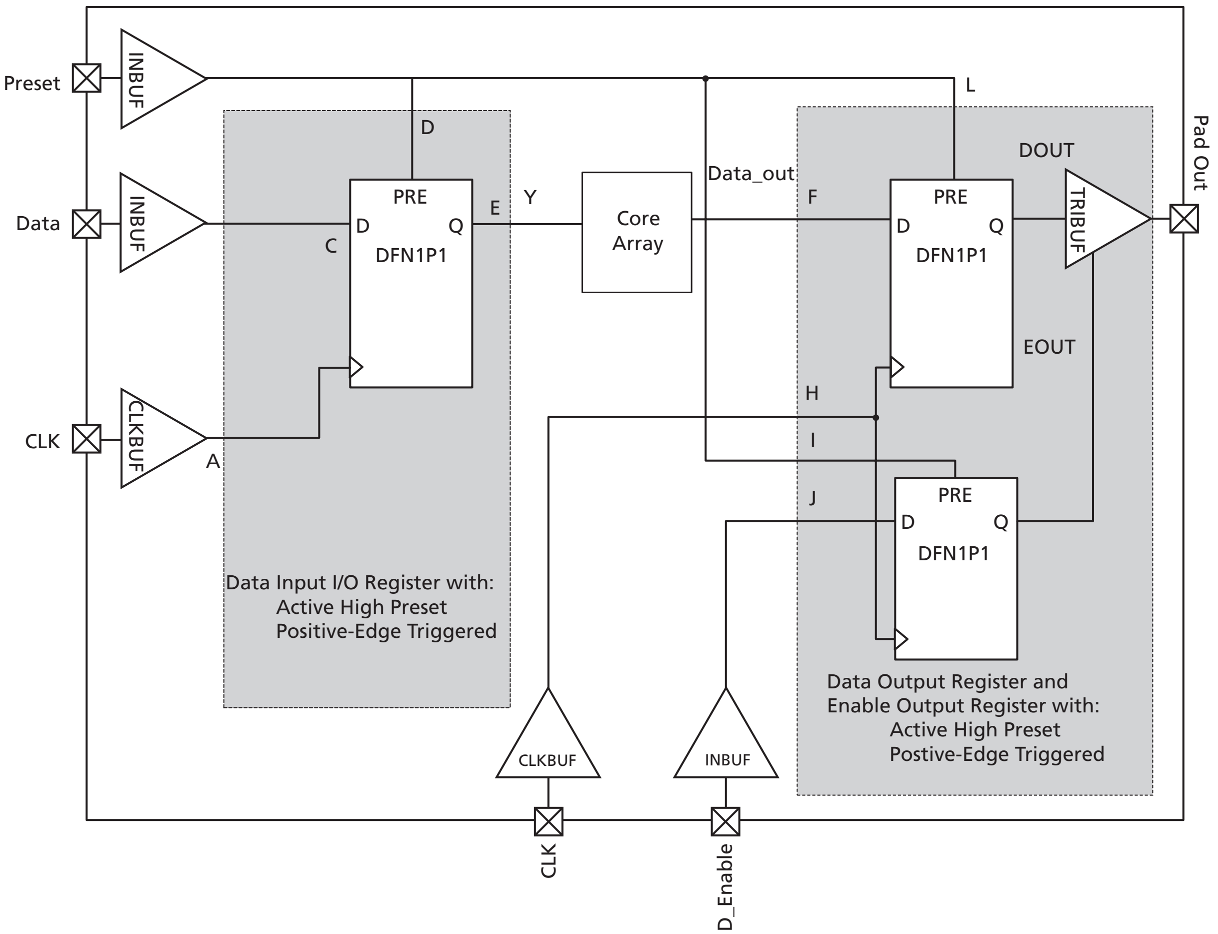


**Figure 2-12 • Timing Model of Registered I/O Buffers with Asynchronous Preset**

***Table 2-62 •*** **Parameter Definition and Measuring Nodes**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | H, DOUT |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | F, H |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | F, H |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | L, DOUT |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | L, H |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | L, H |
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | H, EOUT |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | J, H |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | J, H |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | I, EOUT |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | I, H |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | I, H |
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | A, E |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | C, A |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | C, A |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | D, E |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | D, A |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | D, A |

** See Figure 2-12 on page 2-37 for more information.*

## Fully Registered I/O Buffers with Asynchronous Clear

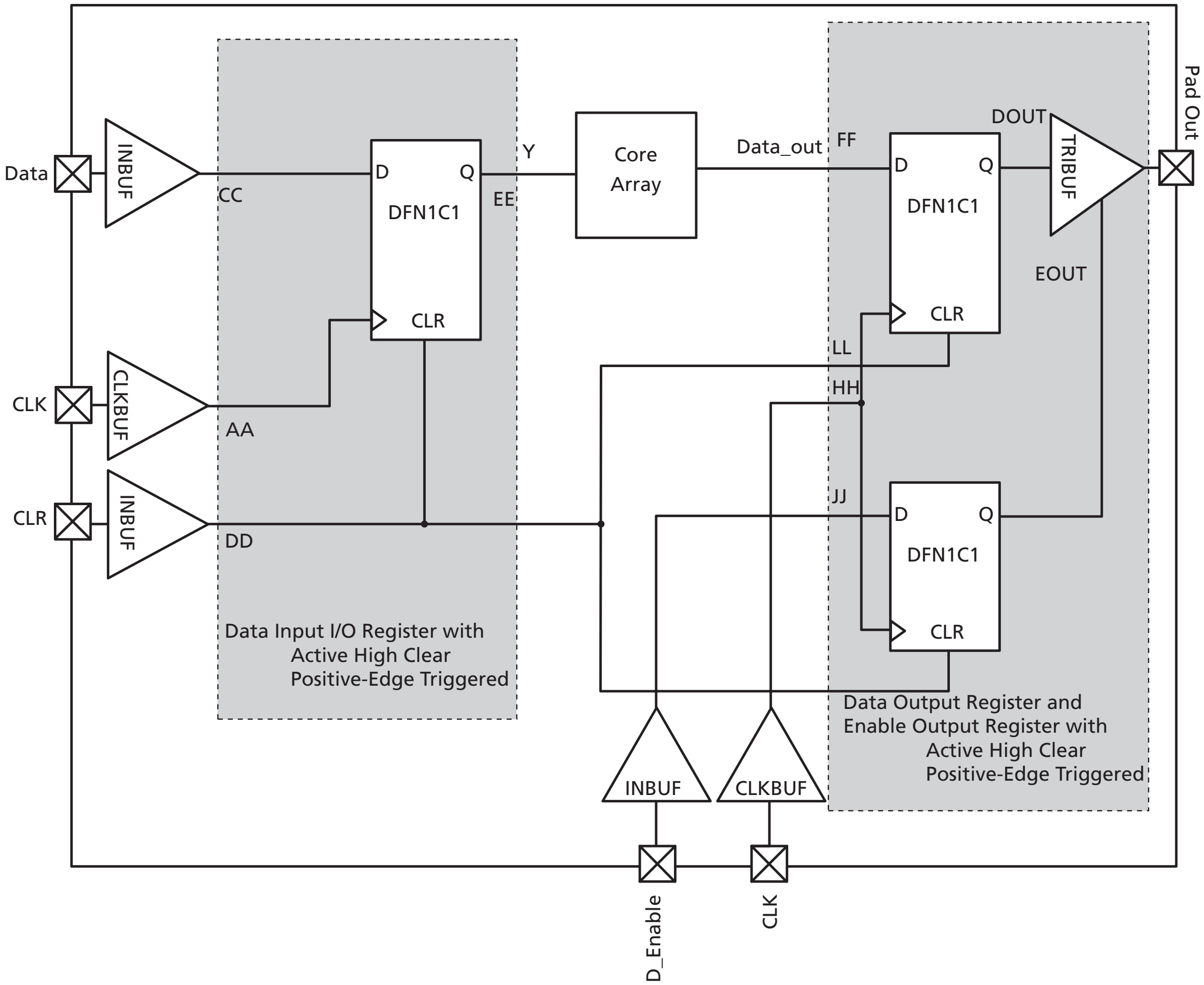


*Figure 2-13* • **Timing Model of the Registered I/O Buffers with Asynchronous Clear**

*Table 2-63 •* **Parameter Definition and Measuring Nodes**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | HH, DOUT |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | FF, HH |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | FF, HH |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | HH, EOUT |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | JJ, HH |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | JJ, HH |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | AA, EE |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | CC, AA |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | CC, AA |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

** See Figure 2-13 on page 2-39 for more information.*

## Input Register

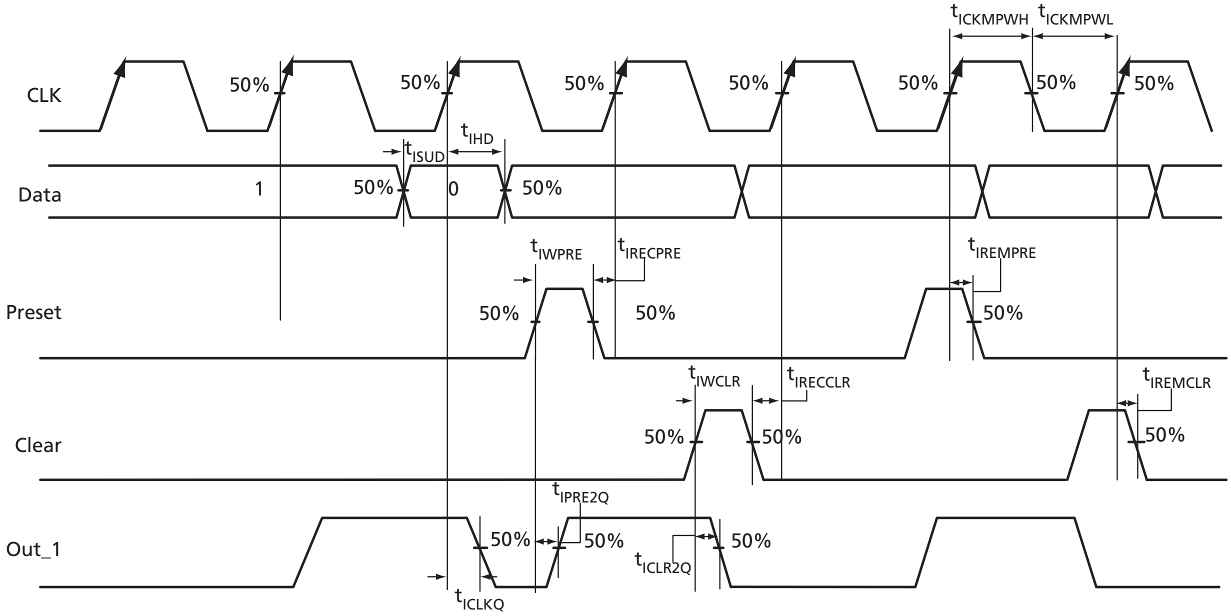


*Figure 2-14* • **Input Register Timing Diagram**

### Timing Characteristics

#### *1.5 V DC Core Voltage*

*Table 2-64* • **Input Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.42 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.47 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 0.79 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 0.79 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width HIGH for the Input Data Register | 0.31 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width LOW for the Input Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### *1.2 V DC Core Voltage*

**Table 2-65 • Input Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.68 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.97 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 1.19 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 1.19 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width HIGH for the Input Data Register | 0.31 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width LOW for the Input Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## Output Register

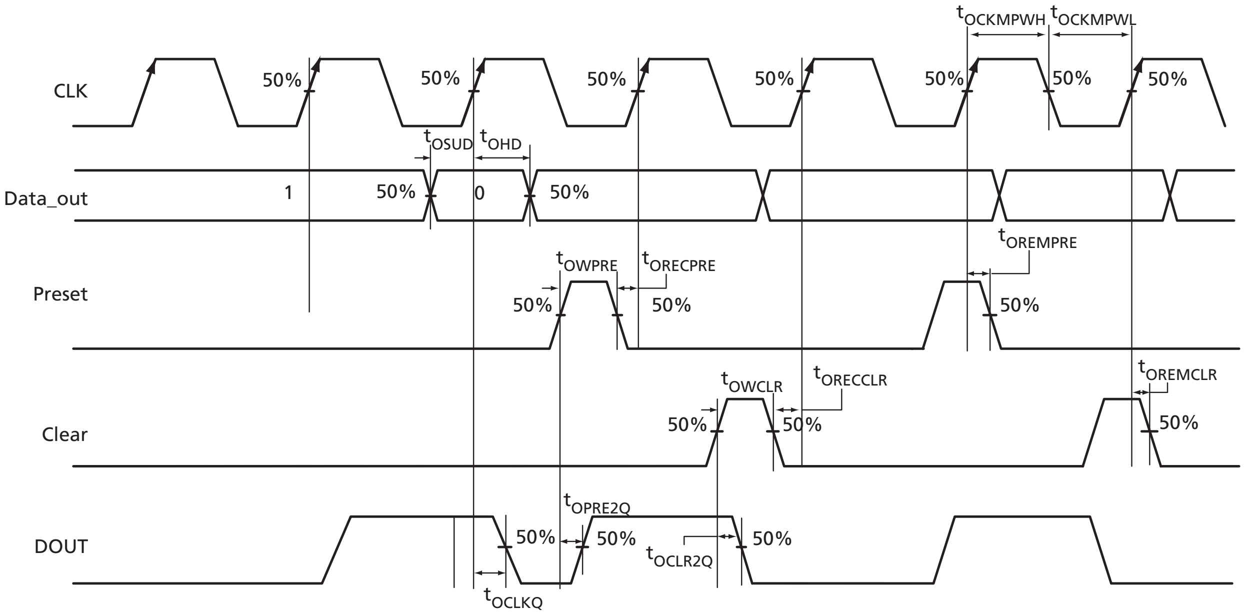


**Figure 2-15 • Output Register Timing Diagram**

### Timing Characteristics

#### 1.5 V DC Core Voltage

**Table 2-66 • Output Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | 1.00 | ns |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | 0.51 | ns |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | 0.00 | ns |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | 1.34 | ns |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | 1.34 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output Data Register | 0.31 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-67 • Output Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | 1.52 | ns |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | 1.15 | ns |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | 0.00 | ns |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | 1.96 | ns |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | 1.96 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output Data Register | 0.31 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## Output Enable Register

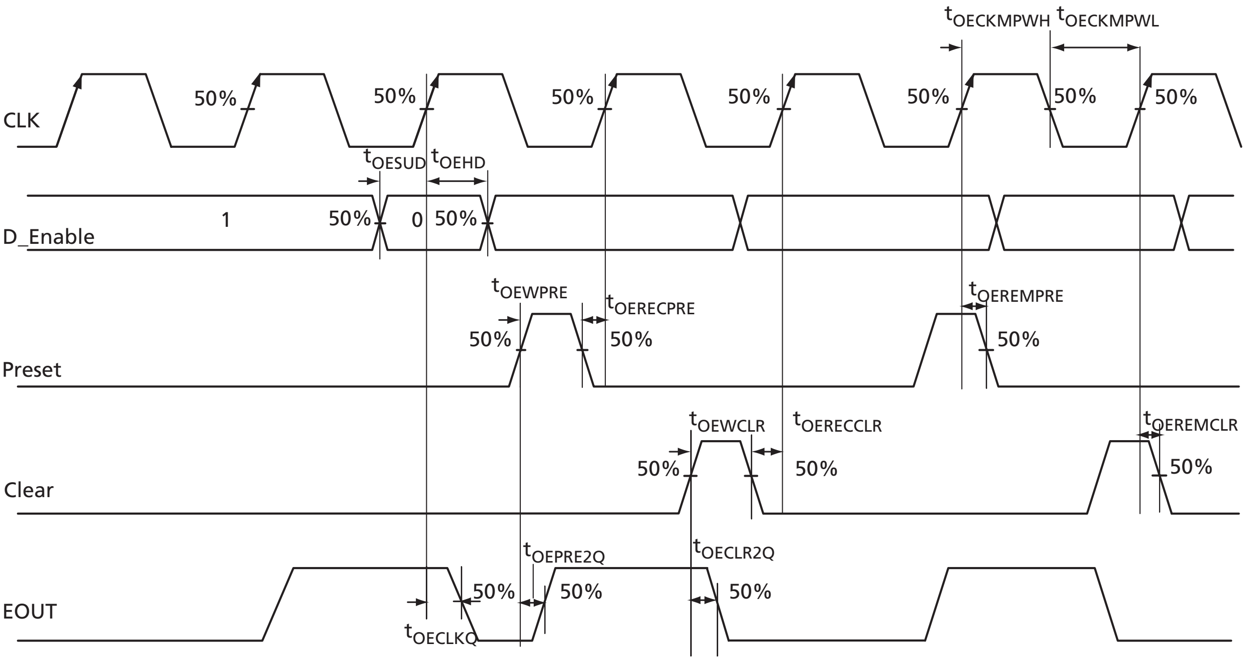


***Figure 2-16* • Output Enable Register Timing Diagram**

### Timing Characteristics

#### *1.5 V DC Core Voltage*

***Table 2-68* • Output Enable Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | 0.75 | ns |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | 0.51 | ns |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 1.13 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 1.13 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OEWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output Enable Register | 0.31 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width LOW for the Output Enable Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### *1.2 V DC Core Voltage*

*Table 2-69 •* **Output Enable Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | 1.10 | ns |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | 1.15 | ns |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 1.65 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 1.65 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OEWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output Enable Register | 0.31 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width LOW for the Output Enable Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## DDR Module Specifications

### Input DDR Module

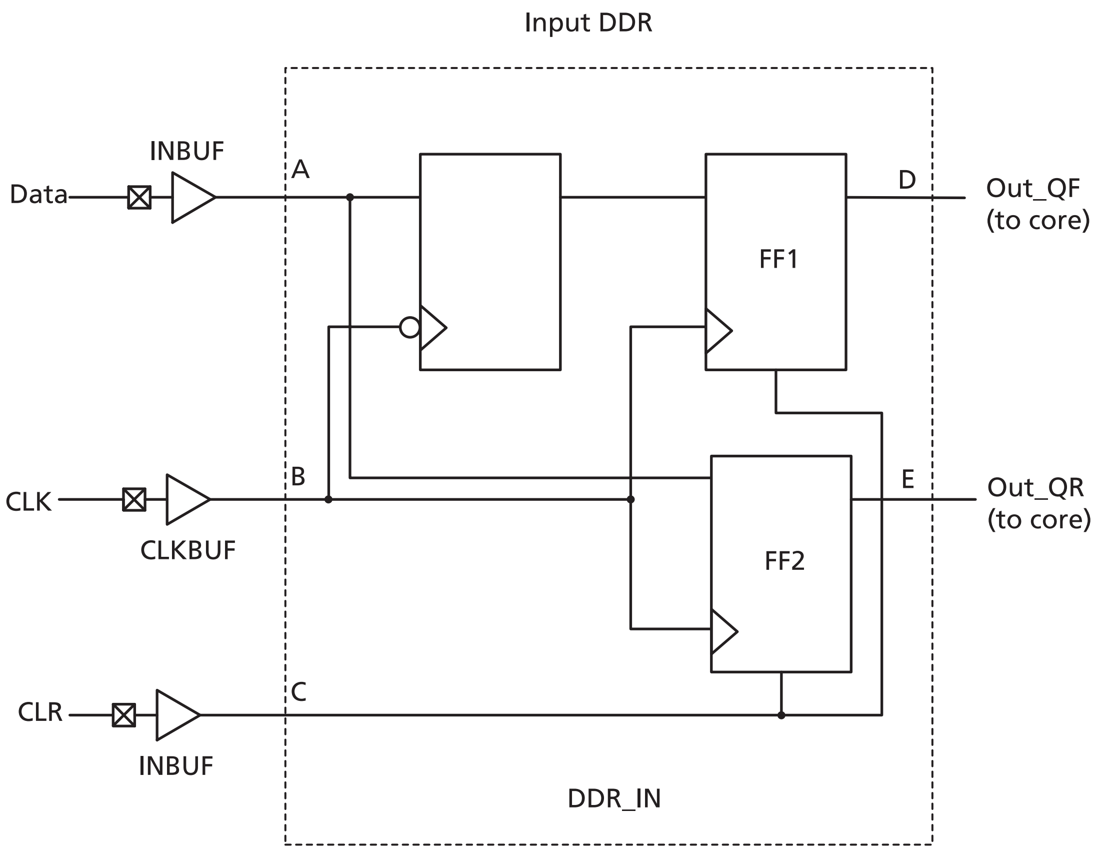


*Figure 2-17* • **Input DDR Timing Model**

*Table 2-70* • **Parameter Definitions**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR input | A, B |
| $t_{DDRIHD}$ | Data Hold Time of DDR input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |

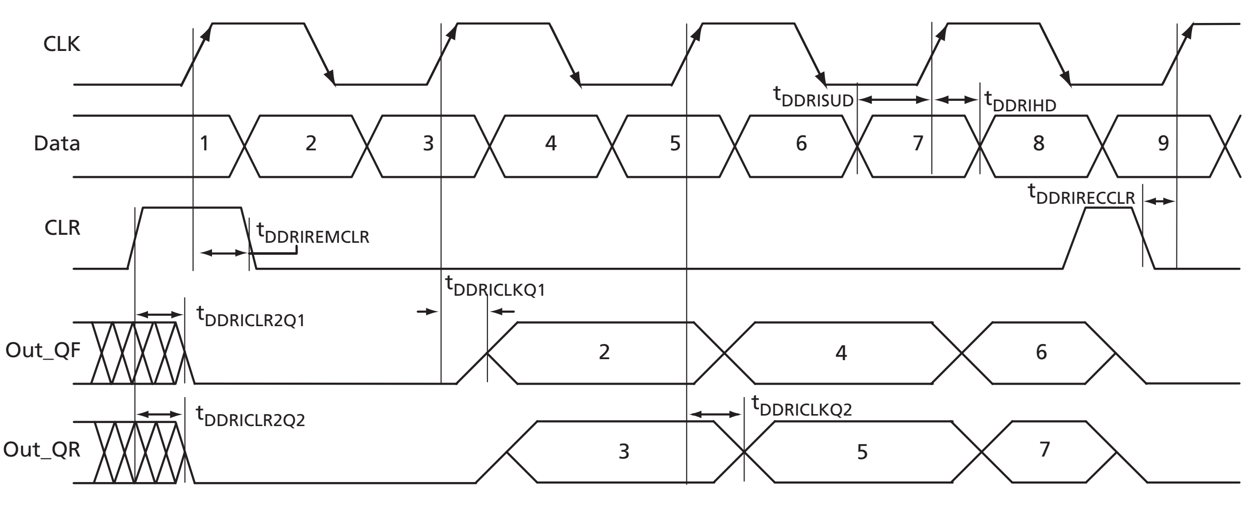


*Figure 2-18* • **Input DDR Timing Diagram**

## Timing Characteristics

### *1.5 V DC Core Voltage*

***Table 2-71*** • **Input DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.25 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR for Input DDR | 0.48 | ns |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF for Input DDR | 0.65 | ns |
| $t_{DDRISUD1}$ | Data Setup for Input DDR (negedge) | 0.50 | ns |
| $t_{DDRISUD2}$ | Data Setup for Input DDR (posedge) | 0.40 | ns |
| $t_{DDRIHD1}$ | Data Hold for Input DDR (negedge) | 0.00 | ns |
| $t_{DDRIHD2}$ | Data Hold for Input DDR (posedge) | 0.00 | ns |
| $t_{DDRICLR2Q1}$ | Asynchronous Clear-to-Out Out_QR for Input DDR | 0.82 | ns |
| $t_{DDRICLR2Q2}$ | Asynchronous Clear-to-Out Out_QF for Input DDR | 0.98 | ns |
| $t_{DDRIREMCLR}$ | Asynchronous Clear Removal Time for Input DDR | 0.00 | ns |
| $t_{DDRIRECCLR}$ | Asynchronous Clear Recovery Time for Input DDR | 0.23 | ns |
| $t_{DDRIWCLR}$ | Asynchronous Clear Minimum Pulse Width for Input DDR | 0.19 | ns |
| $t_{DDRICKMPWH}$ | Clock Minimum Pulse Width HIGH for Input DDR | 0.31 | ns |
| $t_{DDRICKMPWL}$ | Clock Minimum Pulse Width LOW for Input DDR | 0.28 | ns |
| $F_{DDRIMAX}$ | Maximum Frequency for Input DDR | TBD | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

### *1.2 V DC Core Voltage*

***Table 2-72 •*** **Input DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR for Input DDR | 0.76 | ns |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF for Input DDR | 0.94 | ns |
| $t_{DDRISUD1}$ | Data Setup for Input DDR (negedge) | 0.93 | ns |
| $t_{DDRISUD2}$ | Data Setup for Input DDR (posedge) | 0.84 | ns |
| $t_{DDRIHD1}$ | Data Hold for Input DDR (negedge) | 0.00 | ns |
| $t_{DDRIHD2}$ | Data Hold for Input DDR (posedge) | 0.00 | ns |
| $t_{DDRICLR2Q1}$ | Asynchronous Clear-to-Out Out_QR for Input DDR | 1.23 | ns |
| $t_{DDRICLR2Q2}$ | Asynchronous Clear-to-Out Out_QF for Input DDR | 1.42 | ns |
| $t_{DDRIREMCLR}$ | Asynchronous Clear Removal Time for Input DDR | 0.00 | ns |
| $t_{DDRIRECCLR}$ | Asynchronous Clear Recovery Time for Input DDR | 0.24 | ns |
| $t_{DDRIWCLR}$ | Asynchronous Clear Minimum Pulse Width for Input DDR | 0.19 | ns |
| $t_{DDRICKMPWH}$ | Clock Minimum Pulse Width HIGH for Input DDR | 0.31 | ns |
| $t_{DDRICKMPWL}$ | Clock Minimum Pulse Width LOW for Input DDR | 0.28 | ns |
| $F_{DDRIMAX}$ | Maximum Frequency for Input DDR | TBD | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## Output DDR Module

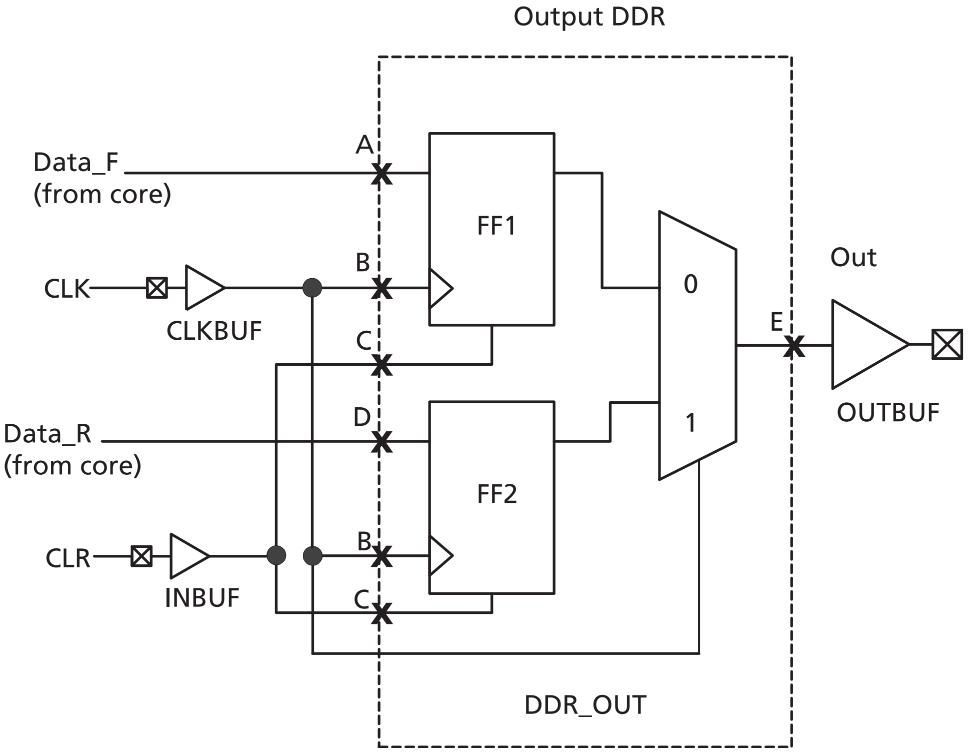


*Figure 2-19* • **Output DDR Timing Model**

*Table 2-73* • **Parameter Definitions**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out | B, E |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out | C, E |
| $t_{DDROREMCLR}$ | Clear Removal | C, B |
| $t_{DDRORECCLR}$ | Clear Recovery | C, B |
| $t_{DDROSUD1}$ | Data Setup Data_F | A, B |
| $t_{DDROSUD2}$ | Data Setup Data_R | D, B |
| $t_{DDROHD1}$ | Data Hold Data_F | A, B |
| $t_{DDROHD2}$ | Data Hold Data_R | D, B |

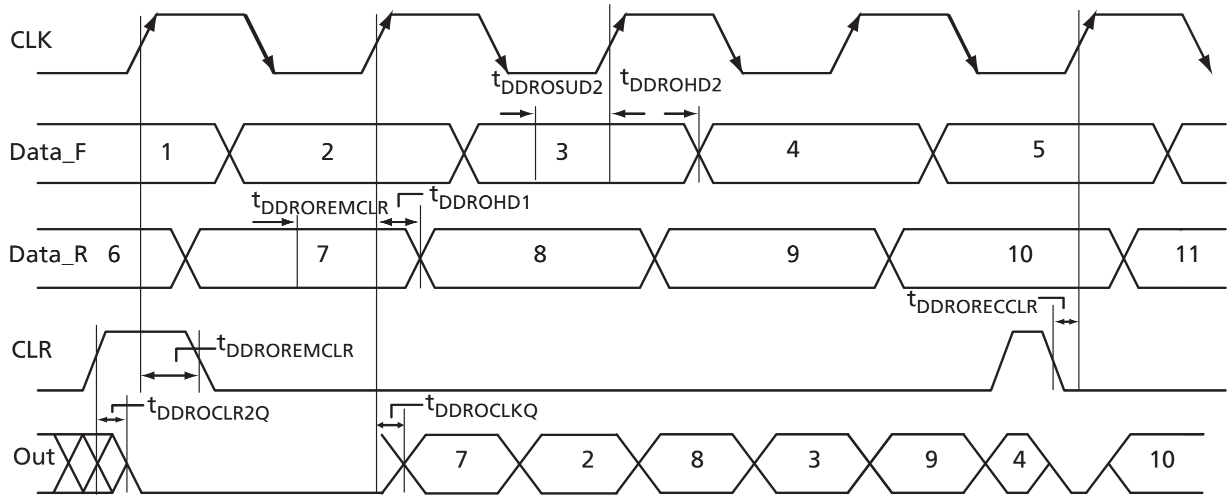


***Figure 2-20* • Output DDR Timing Diagram**

## Timing Characteristics

### *1.5 V DC Core Voltage*

***Table 2-74* • Output DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 1.07 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 0.67 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 0.67 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 1.38 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.23 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.19 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output DDR | 0.31 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output DDR | 0.28 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | TBD | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### *1.2 V DC Core Voltage*

***Table 2-75 •*** **Output DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 1.60 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 1.09 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 1.16 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 1.99 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.24 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.19 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output DDR | 0.31 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output DDR | 0.28 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | TBD | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

# VersaTile Characteristics

## VersaTile Specifications as a Combinatorial Module

The IGLOO nano library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/ E Macro Library Guide*.

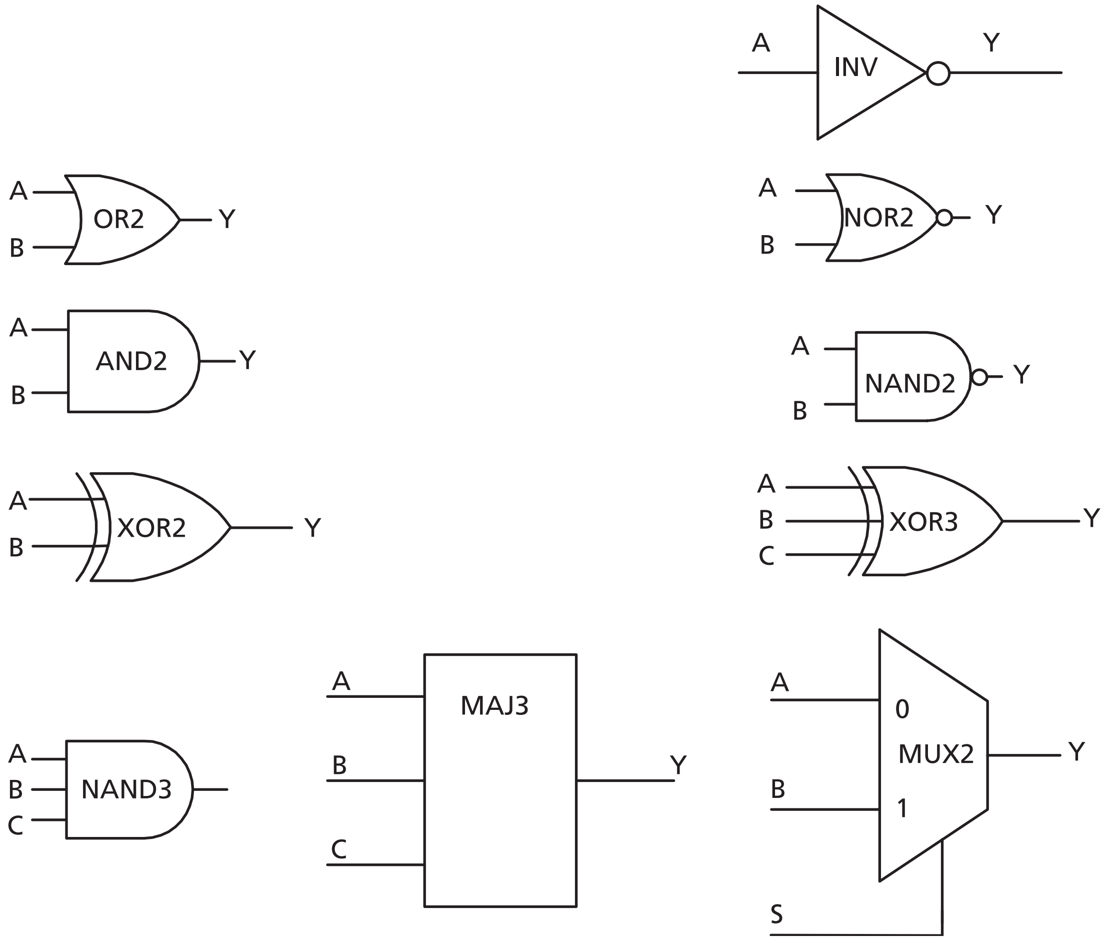


*Figure 2-21* • **Sample of Combinatorial Cells**

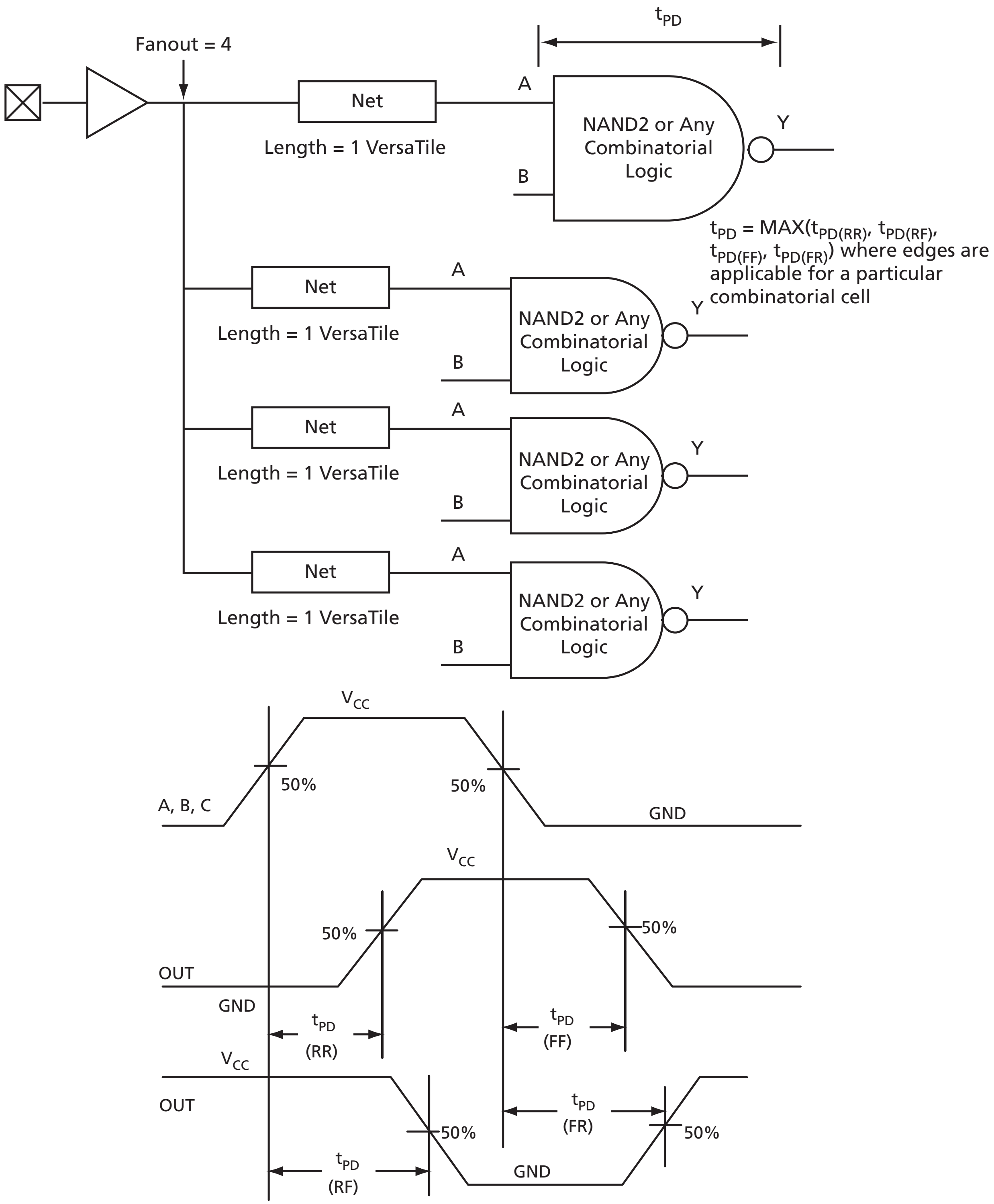


*Figure 2-22* • **Timing Model and Waveforms**

## *Timing Characteristics*

### 1.5 V DC Core Voltage

***Table 2-76 •*** **Combinatorial Cell Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V**

| Combinatorial Cell | Equation | Parameter | Std. | Units |
|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 0.76 | ns |
| AND2 | $Y = A \cdot B$ | $t_{PD}$ | 0.87 | ns |
| NAND2 | $Y = !(A \cdot B)$ | $t_{PD}$ | 0.91 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 0.90 | ns |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 0.94 | ns |
| XOR2 | $Y = A \oplus B$ | $t_{PD}$ | 1.39 | ns |
| MAJ3 | Y = MAJ(A, B, C) | $t_{PD}$ | 1.44 | ns |
| XOR3 | $Y = A \oplus B \oplus C$ | $t_{PD}$ | 1.60 | ns |
| MUX2 | Y = A !S + B S | $t_{PD}$ | 1.17 | ns |
| AND3 | $Y = A \cdot B \cdot C$ | $t_{PD}$ | 1.18 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

***Table 2-77 •*** **Combinatorial Cell Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V**

| Combinatorial Cell | Equation | Parameter | Std. | Units |
|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 1.33 | ns |
| AND2 | $Y = A \cdot B$ | $t_{PD}$ | 1.48 | ns |
| NAND2 | $Y = !(A \cdot B)$ | $t_{PD}$ | 1.58 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 1.53 | ns |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 1.63 | ns |
| XOR2 | $Y = A \oplus B$ | $t_{PD}$ | 2.34 | ns |
| MAJ3 | Y = MAJ(A, B, C) | $t_{PD}$ | 2.59 | ns |
| XOR3 | $Y = A \oplus B \oplus C$ | $t_{PD}$ | 2.74 | ns |
| MUX2 | Y = A !S + B S | $t_{PD}$ | 2.03 | ns |
| AND3 | $Y = A \cdot B \cdot C$ | $t_{PD}$ | 2.11 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## VersaTile Specifications as a Sequential Module

The IGLOO nano library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

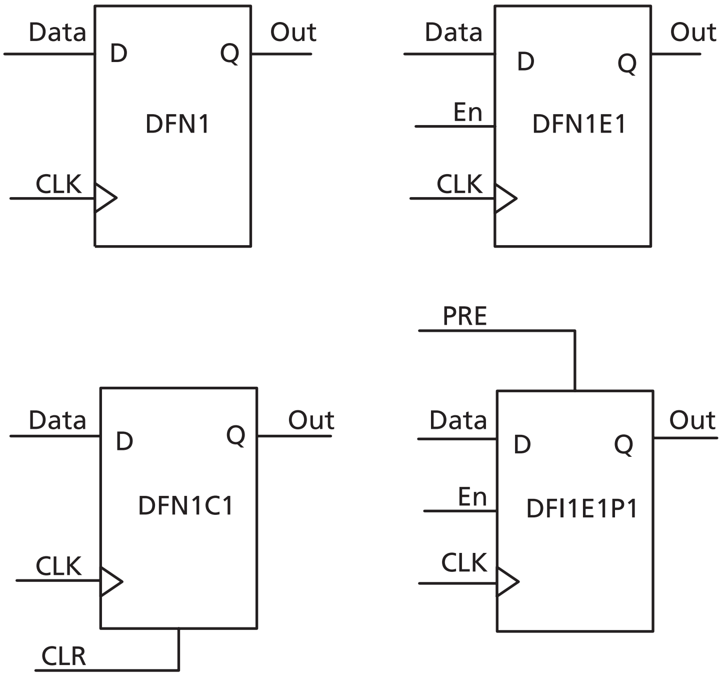


***Figure 2-23*** **• Sample of Sequential Cells**

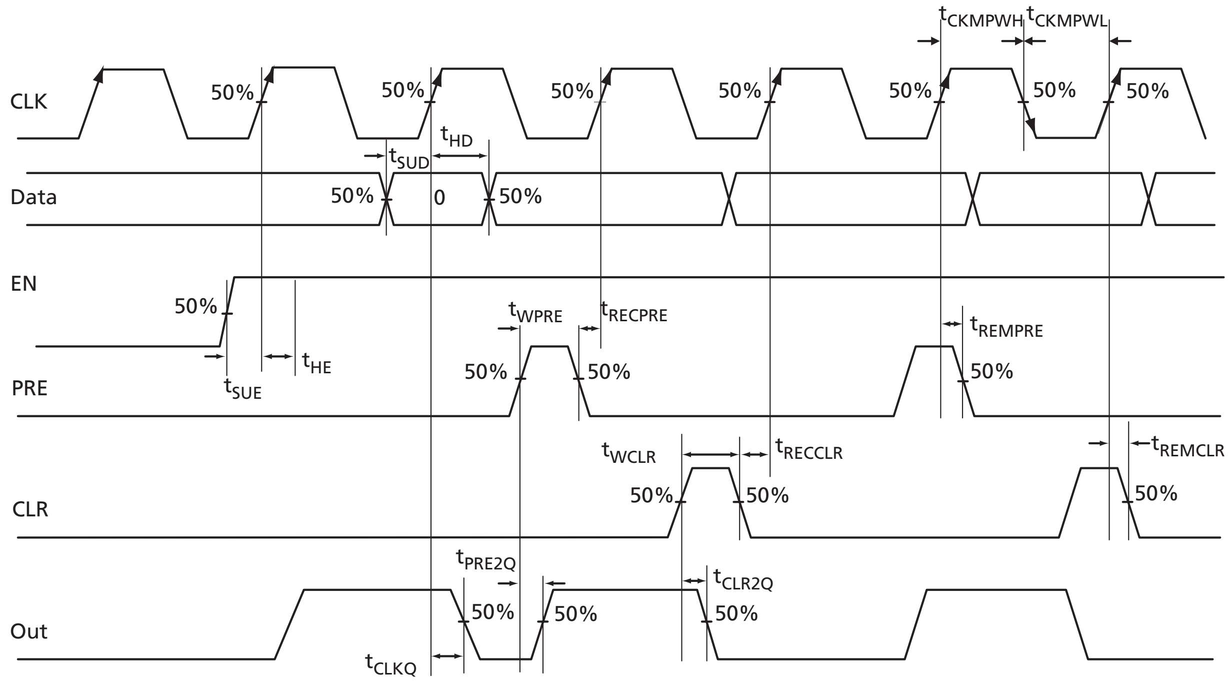


*Figure 2-24* • **Timing Model and Waveforms**

## Timing Characteristics

### 1.5 V DC Core Voltage

***Table 2-78* • Register Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 0.89 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 0.81 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 0.73 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.60 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.62 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.24 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.23 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.30 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.30 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width HIGH for the Core Register | 0.56 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width LOW for the Core Register | 0.56 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

***Table 2-79 •*** **Register Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 1.61 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 1.17 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 1.29 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.87 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.89 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.24 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.24 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.46 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.46 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width HIGH for the Core Register | 0.95 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width LOW for the Core Register | 0.95 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

# Global Resource Characteristics

## AGLN125 Clock Tree Topology

Clock delays are device-specific. Figure 2-25 is an example of a global tree used for clock routing. The global tree presented in Figure 2-25 is driven by a CCC located on the west side of the AGLN125 device. It is used to drive all D-flip-flops in the device.

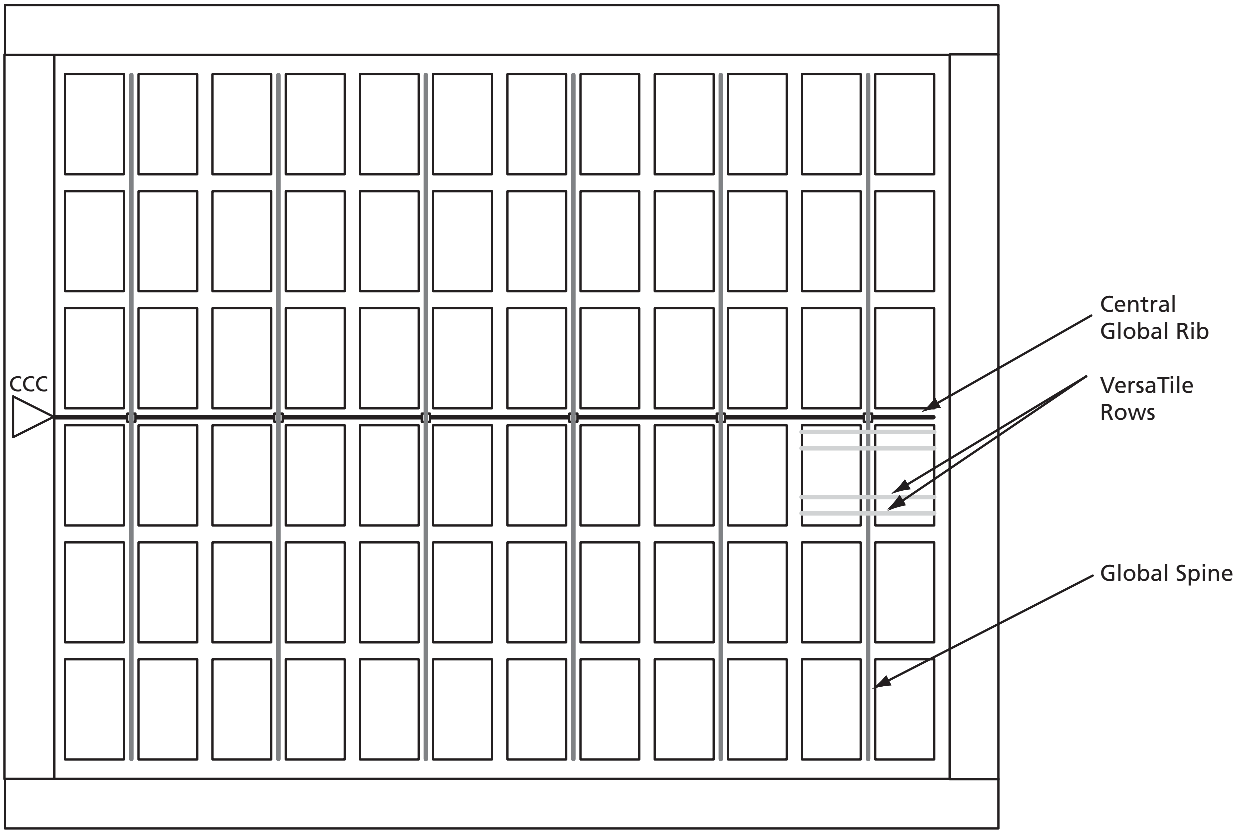


*Figure 2-25* • **Example of Global Tree Use in an AGLN125 Device for Clock Routing**

## Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-66. Table 2-80 to Table 2-88 on page 2-64 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

### Timing Characteristics

#### *1.5 V DC Core Voltage*

*Table 2-80 •* **AGLN010 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input LOW Delay for Global Clock | 1.08 | 1.36 | ns |
| $t_{RCKH}$ | Input HIGH Delay for Global Clock | 1.09 | 1.44 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.35 | ns |
| $F_{RMAX}$ | Maximum Frequency for Global Clock | | | MHz |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-81 •* **AGLN015 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input LOW Delay for Global Clock | 1.15 | 1.49 | ns |
| $t_{RCKH}$ | Input HIGH Delay for Global Clock | 1.16 | 1.59 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.42 | ns |
| $F_{RMAX}$ | Maximum Frequency for Global Clock | | | MHz |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-82 •* **AGLN020 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.425 V**

| **Parameter** | **Description** | **Std.** | | **Units** |
|---|---|---|---|---|
| | | **Min.**[1] | **Max.**[2] | |
| $t_{RCKL}$ | Input LOW Delay for Global Clock | 1.15 | 1.49 | ns |
| $t_{RCKH}$ | Input HIGH Delay for Global Clock | 1.16 | 1.59 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.42 | ns |
| $F_{RMAX}$ | Maximum Frequency for Global Clock | | | MHz |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-83 •* **AGLN060 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.425 V**

| **Parameter** | **Description** | **Std.** | | **Units** |
|---|---|---|---|---|
| | | **Min.**[1] | **Max.**[2] | |
| $t_{RCKL}$ | Input LOW Delay for Global Clock | 1.32 | 1.67 | ns |
| $t_{RCKH}$ | Input HIGH Delay for Global Clock | 1.34 | 1.76 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.42 | ns |
| $F_{RMAX}$ | Maximum Frequency for Global Clock | | | MHz |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-84 •*** **AGLN125 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input LOW Delay for Global Clock | 1.36 | 1.71 | ns |
| $t_{RCKH}$ | Input HIGH Delay for Global Clock | 1.39 | 1.82 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.43 | ns |
| $F_{RMAX}$ | Maximum Frequency for Global Clock | | | MHz |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-85 •*** **AGLN250 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input LOW Delay for Global Clock | 1.39 | 1.73 | ns |
| $t_{RCKH}$ | Input HIGH Delay for Global Clock | 1.41 | 1.84 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.43 | ns |
| $F_{RMAX}$ | Maximum Frequency for Global Clock | | | MHz |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### *1.2 V DC Core Voltage*

***Table 2-86 •*** **AGLN010 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. |  | Units |
|---|---|---|---|---|
|  |  | Min.[1] | Max.[2] |  |
| $t_{RCKL}$ | Input LOW Delay for Global Clock | TBD | TBD | ns |
| $t_{RCKH}$ | Input HIGH Delay for Global Clock | TBD | TBD | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock |  |  | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock |  |  | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock |  | TBD | ns |
| $F_{RMAX}$ | Maximum Frequency for Global Clock |  |  | MHz |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-87 •*** **AGLN015 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. |  | Units |
|---|---|---|---|---|
|  |  | Min.[1] | Max.[2] |  |
| $t_{RCKL}$ | Input LOW Delay for Global Clock | TBD | TBD | ns |
| $t_{RCKH}$ | Input HIGH Delay for Global Clock | TBD | TBD | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock |  |  | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock |  |  | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock |  | TBD | ns |
| $F_{RMAX}$ | Maximum Frequency for Global Clock |  |  | MHz |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

**Table 2-88 • AGLN020 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input LOW Delay for Global Clock | TBD | TBD | ns |
| $t_{RCKH}$ | Input HIGH Delay for Global Clock | TBD | TBD | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | TBD | ns |
| $F_{RMAX}$ | Maximum Frequency for Global Clock | | | MHz |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

**Table 2-89 • AGLN060 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input LOW Delay for Global Clock | 2.02 | 2.49 | ns |
| $t_{RCKH}$ | Input HIGH Delay for Global Clock | 2.09 | 2.72 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.63 | ns |
| $F_{RMAX}$ | Maximum Frequency for Global Clock | | | MHz |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-90 •*** **AGLN125 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input LOW Delay for Global Clock | 2.08 | 2.54 | ns |
| $t_{RCKH}$ | Input HIGH Delay for Global Clock | 2.15 | 2.77 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.62 | ns |
| $F_{RMAX}$ | Maximum Frequency for Global Clock | | | MHz |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-91 •*** **AGLN250 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input LOW Delay for Global Clock | 2.11 | 2.57 | ns |
| $t_{RCKH}$ | Input HIGH Delay for Global Clock | 2.19 | 2.81 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.62 | ns |
| $F_{RMAX}$ | Maximum Frequency for Global Clock | | | MHz |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

# Clock Conditioning Circuits

## CCC Electrical Specifications

### Timing Characteristics

*Table 2-92 •* **IGLOO nano CCC/PLL Specification**
**For IGLOO nano V2 or V5 devices, 1.5 V DC Core Supply Voltage**

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Clock Conditioning Circuitry Input Frequency $f_{IN\_CCC}$ | 1.5 | | 250 | MHz |
| Clock Conditioning Circuitry Output Frequency $f_{OUT\_CCC}$ | 0.75 | | 250 | MHz |
| Delay Increments in Programmable Delay Blocks [1, 2] | | 360 | | ps |
| Number of Programmable Values in Each Programmable Delay Block | | | 32 | |
| Serial Clock (SCLK) for Dynamic PLL [5] | | | 100 | |
| Input Cycle-to-Cycle Jitter (peak magnitude) | | | 1 | ns |
| CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$ | Max Peak-to-Peak Period Jitter | | | |
| | 1 Global Network Used | External FB Used | 3 Global Networks Used | |
| 0.75 MHz to 24 MHz | 0.50% | 0.75% | 0.70% | |
| 24 MHz to 100 MHz | 1.00% | 1.50% | 1.20% | |
| 100 MHz to 250 MHz | 2.50% | 3.75% | 2.75% | |
| Acquisition Time | | | | |
| LockControl = 0 | | | 300 | µs |
| LockControl = 1 | | | 6.0 | ms |
| Tracking Jitter | | | | |
| LockControl = 0 | | | 2.5 | ns |
| LockControl = 1 | | | 1.5 | ns |
| Output Duty Cycle | 48.5 | | 51.5 | % |
| Delay Range in Block: Programmable Delay 1 [1, 2] | 1.25 | | 15.65 | ns |
| Delay Range in Block: Programmable Delay 2 [1, 2] | 0.025 | | 15.65 | ns |
| Delay Range in Block: Fixed Delay [1, 2] | | 3.5 | | ns |

*Notes:*

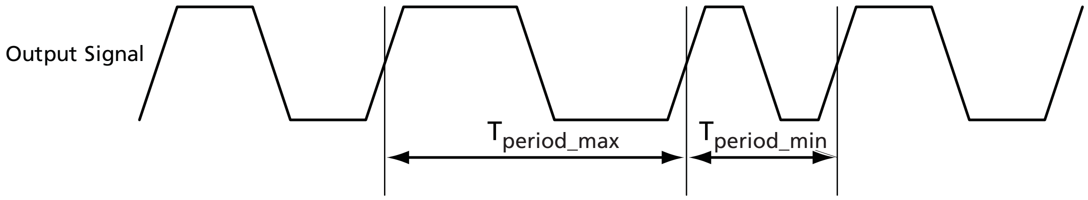
1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for deratings.*
2. *$T_J = 25°C$, $V_{CC} = 1.5$ V*
3. *The AGLN010, AGLN015, and AGLN020 devices do not support PLL.*
4. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
5. *Maximum value obtained for a STD speed grade device in Worst-Case Commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for derating values.*

***Table 2-93 •*** **IGLOO nano CCC/PLL Specification**
**For IGLOO nano V2 Devices, 1.2 V DC Core Supply Voltage**

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Clock Conditioning Circuitry Input Frequency $f_{IN\_CCC}$ | 1.5 | | 160 | MHz |
| Clock Conditioning Circuitry Output Frequency $f_{OUT\_CCC}$ | 0.75 | | 160 | MHz |
| Delay Increments in Programmable Delay Blocks [1, 2] | | 580 | | ps |
| Number of Programmable Values in Each Programmable Delay Block | | | 32 | |
| Serial Clock (SCLK) for Dynamic PLL [5] | | | 60 | MHz |
| Input Cycle-to-Cycle Jitter (peak magnitude) | | | 0.25 | ns |
| CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$ | Max Peak-to-Peak Period Jitter | | | |
| | 1 Global Network Used | External FB Used | 3 Global Networks Used | |
| 0.75 MHz to 24 MHz | 0.50% | 0.75% | 0.70% | |
| 24 MHz to 100 MHz | 1.00% | 1.50% | 1.20% | |
| 100 MHz to 160 MHz | 2.50% | 3.75% | 2.75% | |
| Acquisition Time | | | | |
| LockControl = 0 | | | 300 | µs |
| LockControl = 1 | | | 6.0 | ms |
| Tracking Jitter | | | | |
| LockControl = 0 | | | 4 | ns |
| LockControl = 1 | | | 3 | ns |
| Output Duty Cycle | 48.5 | | 51.5 | % |
| Delay Range in Block: Programmable Delay 1 [1, 2] | 2.3 | | 20.86 | ns |
| Delay Range in Block: Programmable Delay 2 [1, 2,] | 0.025 | | 20.86 | ns |
| Delay Range in Block: Fixed Delay [1, 2] | | 5.7 | | ns |

*Notes:*

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for deratings.*
2. $T_J = 25°C$, $V_{CC} = 1.2$ V
3. *The AGLN010, AGLN015, and AGLN020 devices do not support PLLs.*
4. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.*
5. *Maximum value obtained for a STD speed grade device in Worst-Case Commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for derating values.*



*Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.*

***Figure 2-26*** **• Peak-to-Peak Jitter Definition**

# Embedded SRAM and FIFO Characteristics

## SRAM

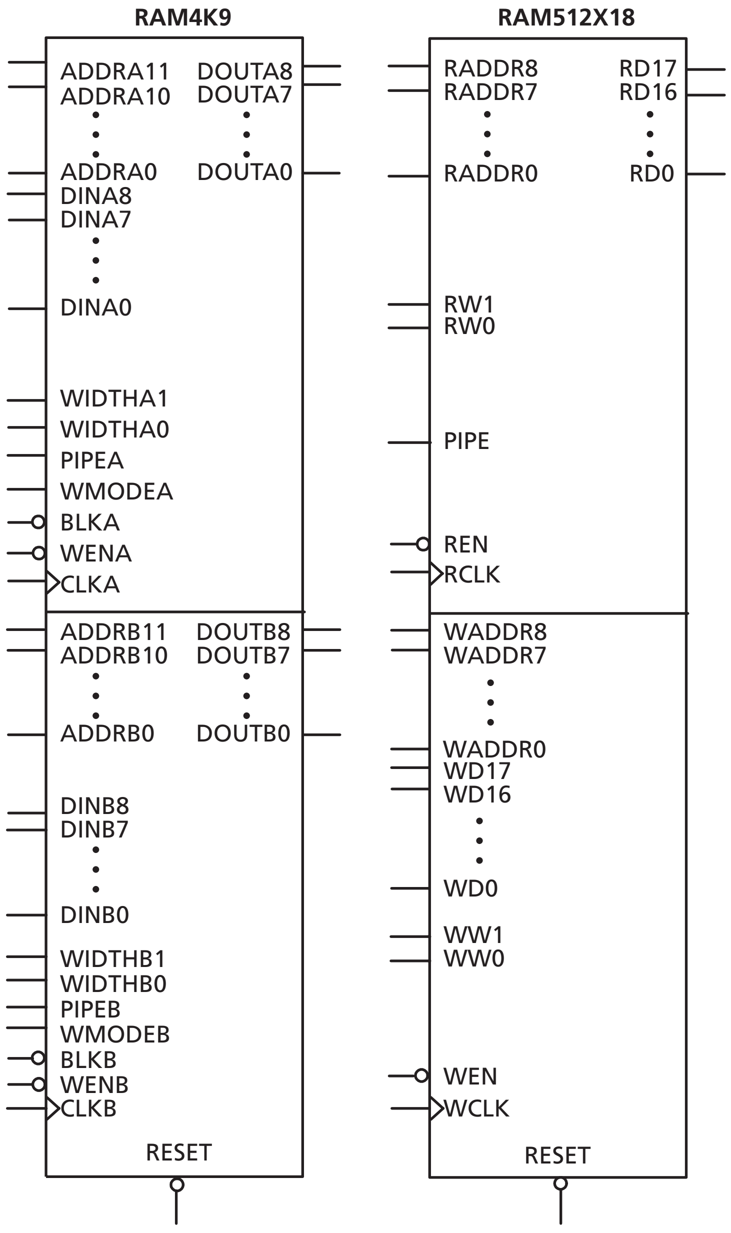


*Figure 2-27* • **RAM Models**

## Timing Waveforms

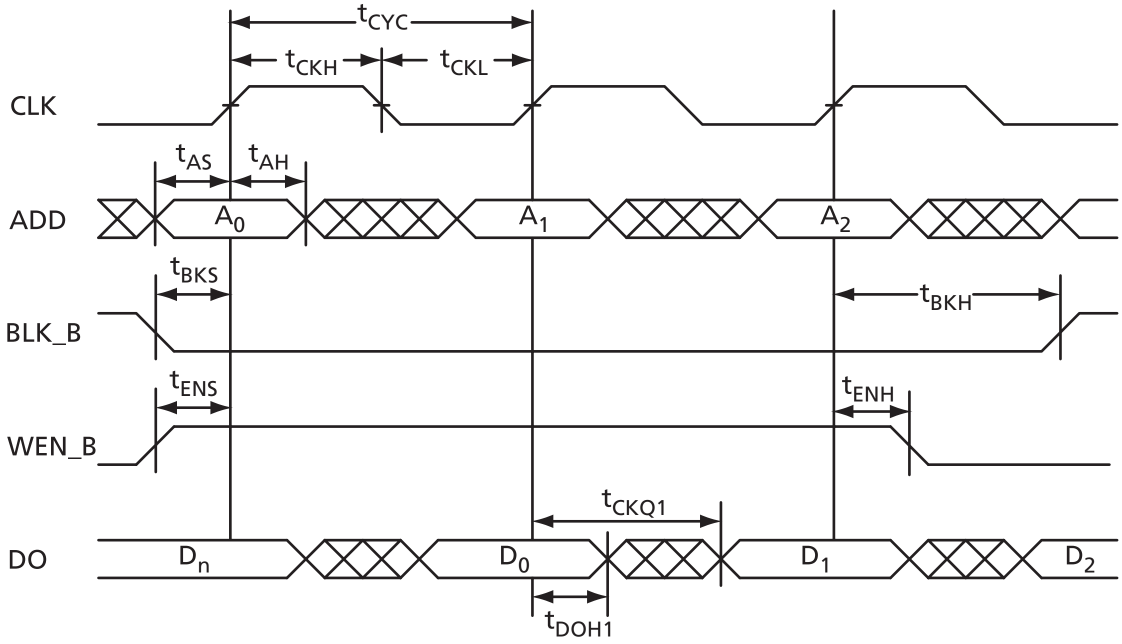


*Figure 2-28* • **RAM Read for Pass-Through Output**

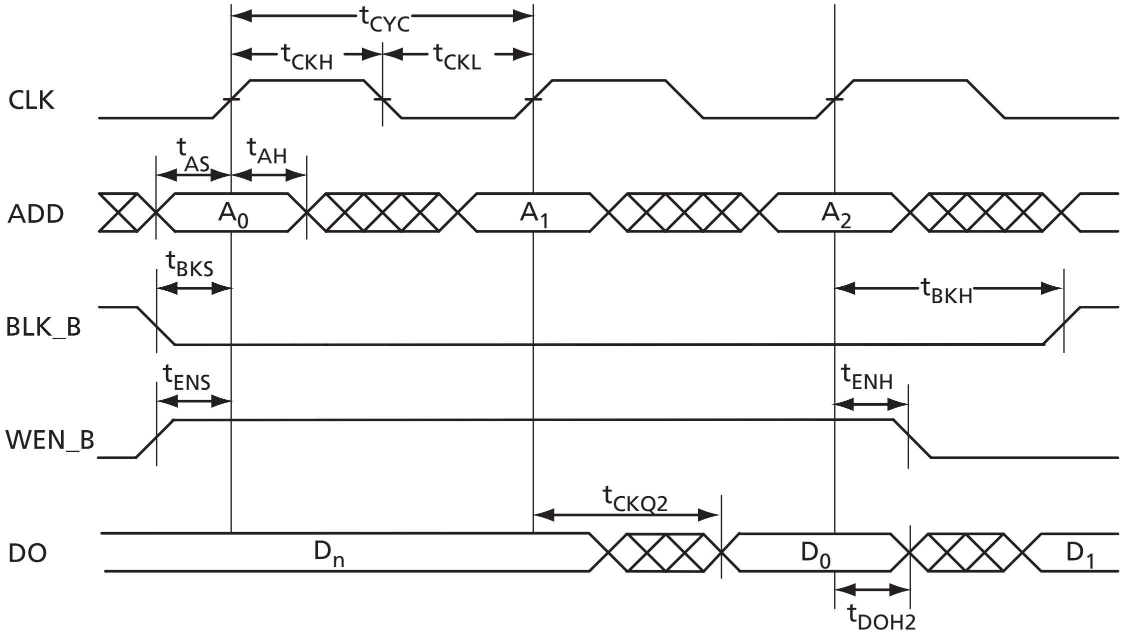


*Figure 2-29* • **RAM Read for Pipelined Output**

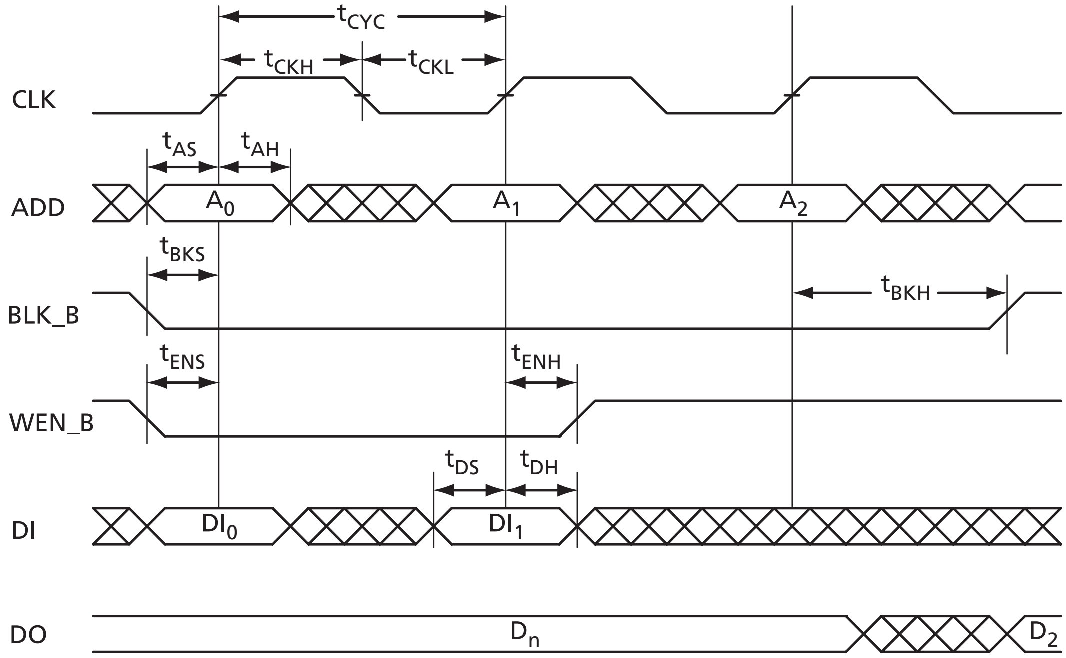


*Figure 2-30* • **RAM Write, Output Retained (WMODE = 0)**

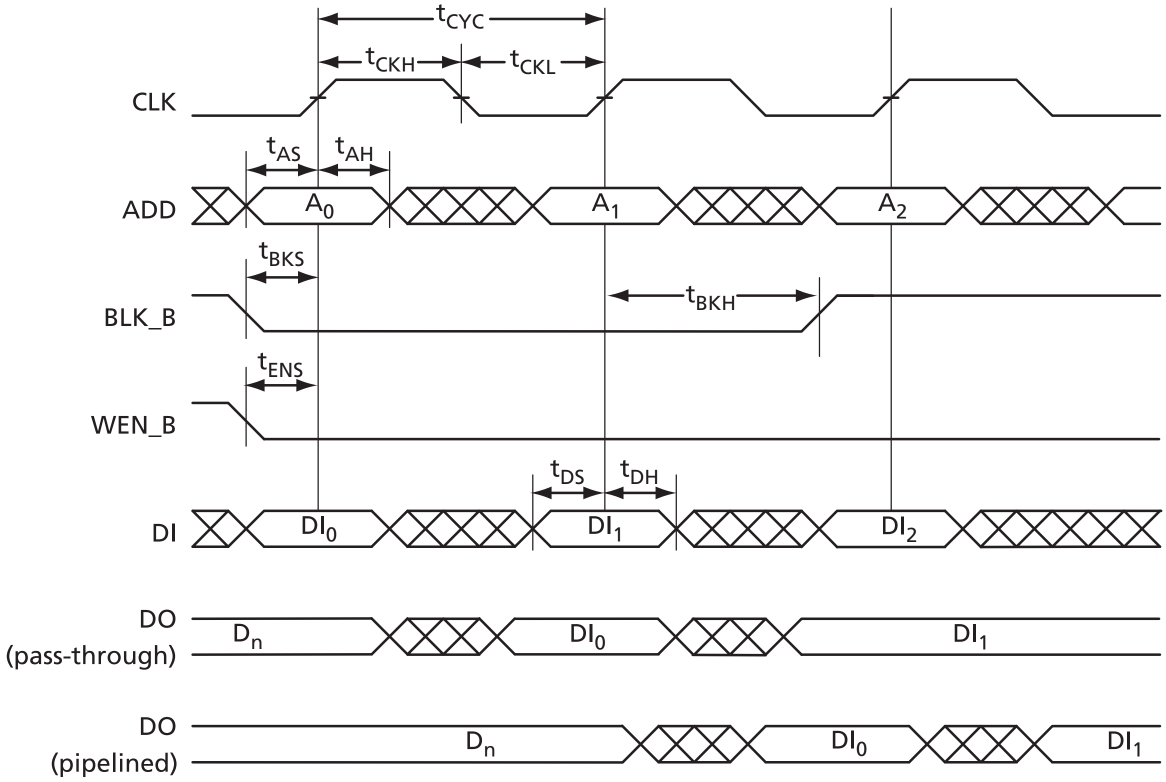


*Figure 2-31* • **RAM Write, Output as Write Data (WMODE = 1)**

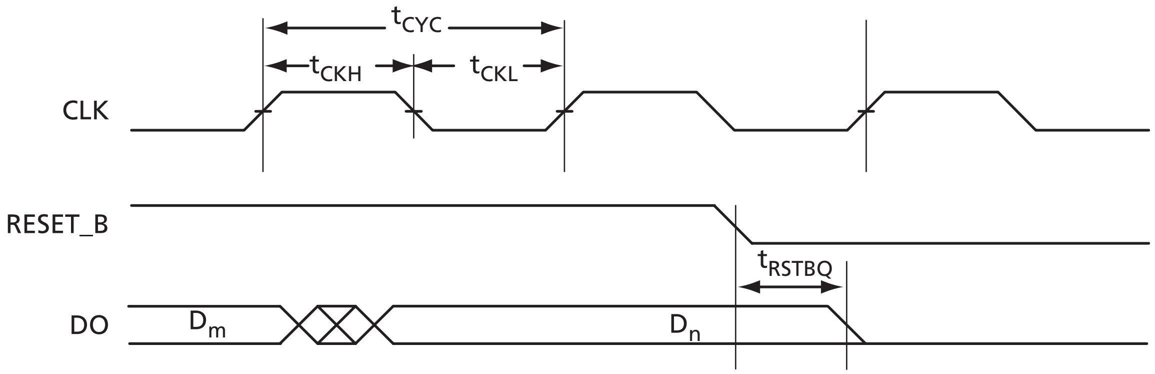


*Figure 2-32* • **RAM Reset**

## *Timing Characteristics*

### 1.5 V DC Core Voltage

*Table 2-94 •* **RAM4K9**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.83 | ns |
| $t_{AH}$ | Address hold time | 0.16 | ns |
| $t_{ENS}$ | REN_B, WEN_B setup time | 0.81 | ns |
| $t_{ENH}$ | REN_B, WEN_B hold time | 0.16 | ns |
| $t_{BKS}$ | BLK_B setup time | 1.65 | ns |
| $t_{BKH}$ | BLK_B hold time | 0.16 | ns |
| $t_{DS}$ | Input data (DI) setup time | 0.71 | ns |
| $t_{DH}$ | Input data (DI) hold time | 0.36 | ns |
| $t_{CKQ1}$ | Clock HIGH to new data valid on DO (output retained, WMODE = 0) | 3.53 | ns |
|  | Clock HIGH to new data valid on DO (flow-through, WMODE = 1) | 3.06 | ns |
| $t_{CKQ2}$ | Clock HIGH to new data valid on DO (pipelined) | 1.81 | ns |
| $t_{C2CWWL}$ | Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge | 0.23 | ns |
| $t_{C2CRWH}$ | Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge | 0.35 | ns |
| $t_{C2CWRH}$ | Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge | 0.41 | ns |
| $t_{RSTBQ}$ | RESET_B LOW to data out LOW on DO (flow-through) | 2.06 | ns |
|  | RESET_B LOW to data out LOW on DO (pipelined) | 2.06 | ns |
| $t_{REMRSTB}$ | RESET_B removal | 0.61 | ns |
| $t_{RECRSTB}$ | RESET_B recovery | 3.21 | ns |
| $t_{MPWRSTB}$ | RESET_B minimum pulse width | 0.68 | ns |
| $t_{CYC}$ | Clock cycle time | 6.24 | ns |
| $F_{MAX}$ | Maximum frequency | 160 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-95 • RAM512X18**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.83 | ns |
| $t_{AH}$ | Address hold time | 0.16 | ns |
| $t_{ENS}$ | REN_B, WEN_B setup time | 0.73 | ns |
| $t_{ENH}$ | REN_B, WEN_B hold time | 0.08 | ns |
| $t_{DS}$ | Input data (DI) setup time | 0.71 | ns |
| $t_{DH}$ | Input data (DI) hold time | 0.36 | ns |
| $t_{CKQ1}$ | Clock HIGH to new data valid on DO (output retained, WMODE = 0) | 4.21 | ns |
| $t_{CKQ2}$ | Clock HIGH to new data valid on DO (pipelined) | 1.71 | ns |
| $t_{C2CRWH}$ | Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge | 0.35 | ns |
| $t_{C2CWRH}$ | Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge | 0.42 | ns |
| $t_{RSTBQ}$ | RESET_B LOW to data out LOW on DO (flow-through) | 2.06 | ns |
| | RESET_B LOW to data out LOW on DO (pipelined) | 2.06 | ns |
| $t_{REMRSTB}$ | RESET_B removal | 0.61 | ns |
| $t_{RECRSTB}$ | RESET_B recovery | 3.21 | ns |
| $t_{MPWRSTB}$ | RESET_B minimum pulse width | 0.68 | ns |
| $t_{CYC}$ | Clock cycle time | 6.24 | ns |
| $F_{MAX}$ | Maximum frequency | 160 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## 1.2 V DC Core Voltage

*Table 2-96 •* **RAM4K9**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address setup time | 1.53 | ns |
| $t_{AH}$ | Address hold time | 0.29 | ns |
| $t_{ENS}$ | REN_B, WEN_B setup time | 1.50 | ns |
| $t_{ENH}$ | REN_B, WEN_B hold time | 0.29 | ns |
| $t_{BKS}$ | BLK_B setup time | 3.05 | ns |
| $t_{BKH}$ | BLK_B hold time | 0.29 | ns |
| $t_{DS}$ | Input data (DI) setup time | 1.33 | ns |
| $t_{DH}$ | Input data (DI) hold time | 0.66 | ns |
| $t_{CKQ1}$ | Clock HIGH to new data valid on DO (output retained, WMODE = 0) | 6.61 | ns |
|  | Clock HIGH to new data valid on DO (flow-through, WMODE = 1) | 5.72 | ns |
| $t_{CKQ2}$ | Clock HIGH to new data valid on DO (pipelined) | 3.38 | ns |
| $t_{C2CWWL}$ | Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge | 0.30 | ns |
| $t_{C2CRWH}$ | Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge | 0.89 | ns |
| $t_{C2CWRH}$ | Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge | 1.01 | ns |
| $t_{RSTBQ}$ | RESET_B LOW to data out LOW on DO (flow-through) | 3.86 | ns |
|  | RESET_B LOW to data out LOW on DO (pipelined) | 3.86 | ns |
| $t_{REMRSTB}$ | RESET_B removal | 1.12 | ns |
| $t_{RECRSTB}$ | RESET_B recovery | 5.93 | ns |
| $t_{MPWRSTB}$ | RESET_B minimum pulse width | 1.18 | ns |
| $t_{CYC}$ | Clock cycle time | 10.90 | ns |
| $F_{MAX}$ | Maximum frequency | 92 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

**Table 2-97 • RAM512X18**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address setup time | 1.53 | ns |
| $t_{AH}$ | Address hold time | 0.29 | ns |
| $t_{ENS}$ | REN_B, WEN_B setup time | 1.36 | ns |
| $t_{ENH}$ | REN_B, WEN_B hold time | 0.15 | ns |
| $t_{DS}$ | Input data (DI) setup time | 1.33 | ns |
| $t_{DH}$ | Input data (DI) hold time | 0.66 | ns |
| $t_{CKQ1}$ | Clock HIGH to new data valid on DO (output retained, WMODE = 0) | 7.88 | ns |
| $t_{CKQ2}$ | Clock HIGH to new data valid on DO (pipelined) | 3.20 | ns |
| $t_{C2CRWH}$ | Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge | 0.87 | ns |
| $t_{C2CWRH}$ | Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge | 1.04 | ns |
| $t_{RSTBQ}$ | RESET_B LOW to data out LOW on DO (flow through) | 3.86 | ns |
| | RESET_B LOW to data out LOW on DO (pipelined) | 3.86 | ns |
| $t_{REMRSTB}$ | RESET_B removal | 1.12 | ns |
| $t_{RECRSTB}$ | RESET_B recovery | 5.93 | ns |
| $t_{MPWRSTB}$ | RESET_B minimum pulse width | 1.18 | ns |
| $t_{CYC}$ | Clock cycle time | 10.90 | ns |
| $F_{MAX}$ | Maximum frequency | 92 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## FIFO

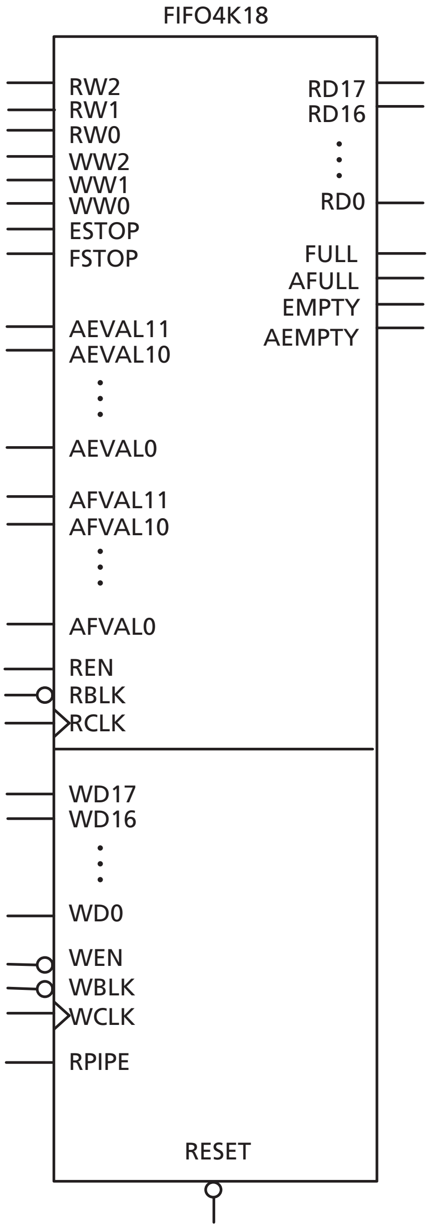


*Figure 2-33* • **FIFO Model**

## Timing Waveforms

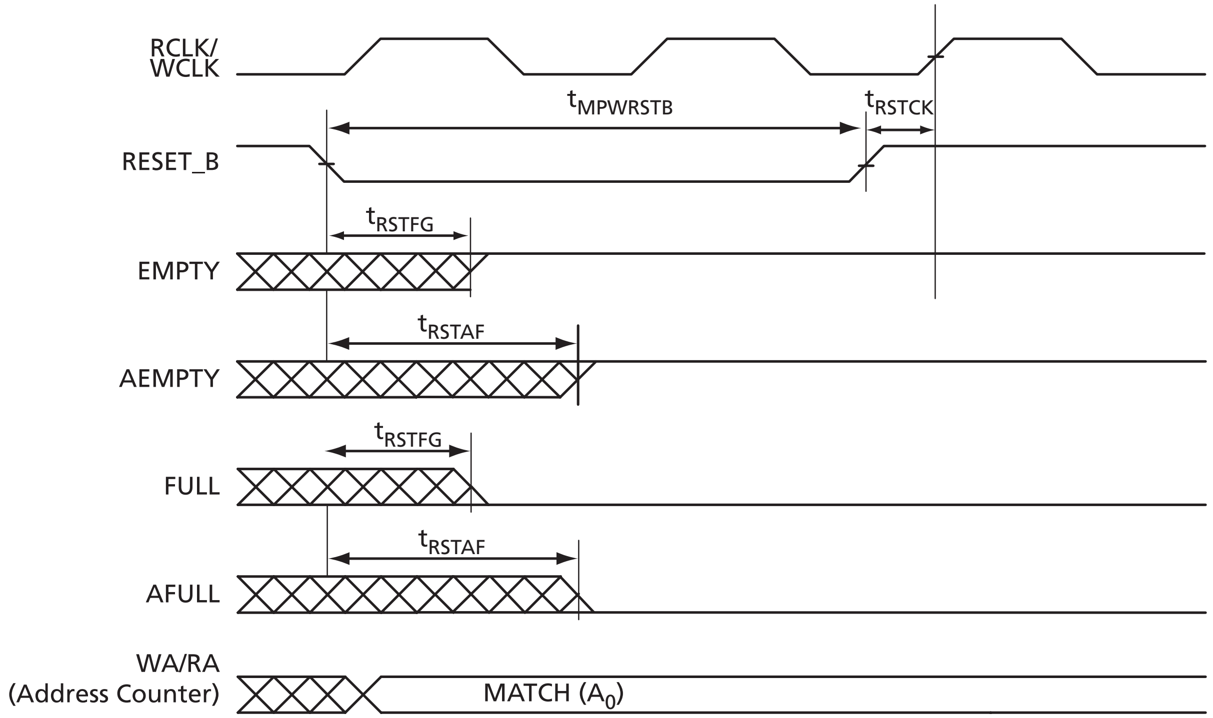


*Figure 2-34* • **FIFO Reset**

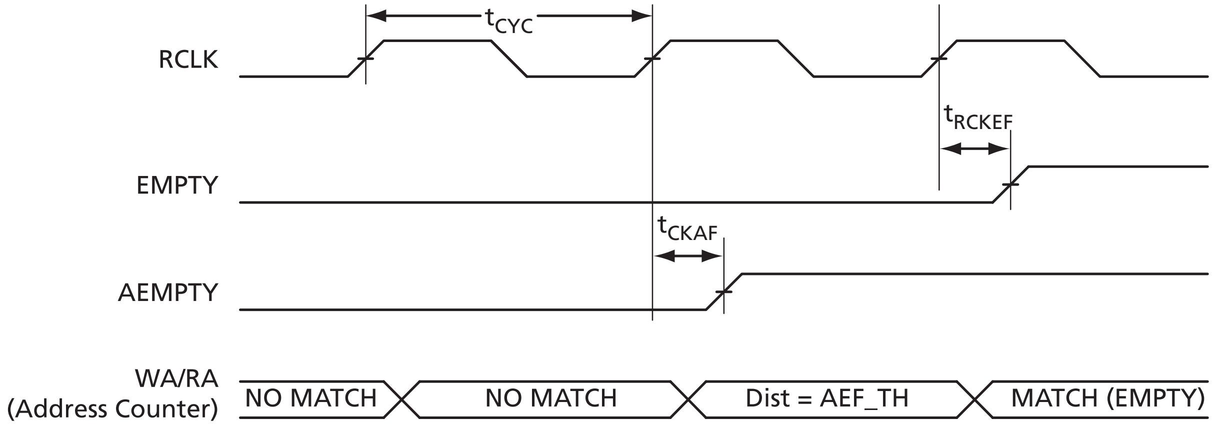


*Figure 2-35* • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

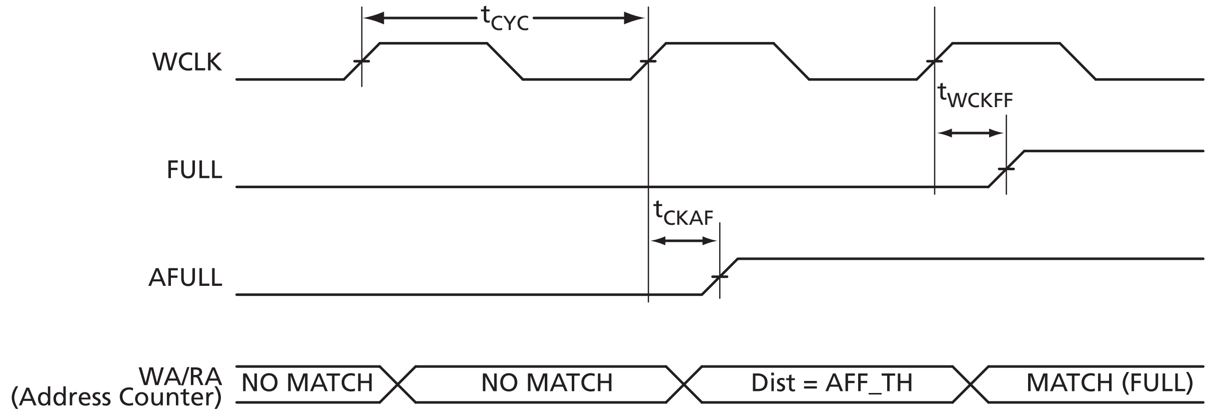


*Figure 2-36* • **FIFO FULL Flag and AFULL Flag Assertion**

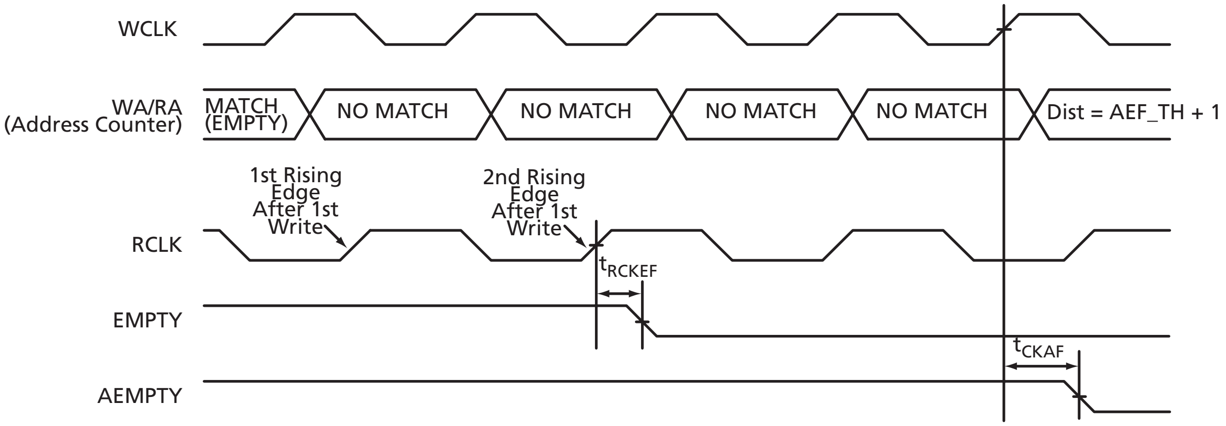


*Figure 2-37* • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

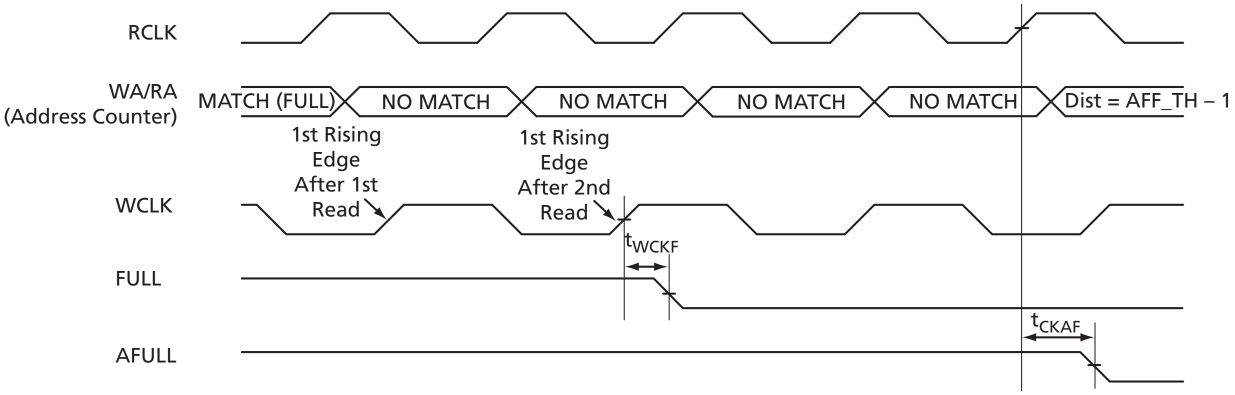


*Figure 2-38* • **FIFO FULL Flag and AFULL Flag Deassertion**

## Timing Characteristics

### 1.5 V DC Core Voltage

***Table 2-98 •*** **FIFO**
**Worst Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ENS}$ | REN_B, WEN_B Setup Time | 1.99 | ns |
| $t_{ENH}$ | REN_B, WEN_B Hold Time | 0.16 | ns |
| $t_{BKS}$ | BLK_B Setup Time | 0.30 | ns |
| $t_{BKH}$ | BLK_B Hold Time | 0.00 | ns |
| $t_{DS}$ | Input Data (DI) Setup Time | 0.76 | ns |
| $t_{DH}$ | Input Data (DI) Hold Time | 0.25 | ns |
| $t_{CKQ1}$ | Clock HIGH to New Data Valid on DO (flow-through) | 3.33 | ns |
| $t_{CKQ2}$ | Clock HIGH to New Data Valid on DO (pipelined) | 1.80 | ns |
| $t_{RCKEF}$ | RCLK HIGH to Empty Flag Valid | 3.53 | ns |
| $t_{WCKFF}$ | WCLK HIGH to Full Flag Valid | 3.35 | ns |
| $t_{CKAF}$ | Clock HIGH to Almost Empty/Full Flag Valid | 12.85 | ns |
| $t_{RSTFG}$ | RESET_B LOW to Empty/Full Flag Valid | 3.48 | ns |
| $t_{RSTAF}$ | RESET_B LOW to Almost Empty/Full Flag Valid | 12.72 | ns |
| $t_{RSTBQ}$ | RESET_B LOW to Data Out LOW on DO (flow-through) | 2.02 | ns |
|  | RESET_B LOW to Data Out LOW on DO (pipelined) | 2.02 | ns |
| $t_{REMRSTB}$ | RESET_B Removal | 0.61 | ns |
| $t_{RECRSTB}$ | RESET_B Recovery | 3.21 | ns |
| $t_{MPWRSTB}$ | RESET_B Minimum Pulse Width | 0.68 | ns |
| $t_{CYC}$ | Clock Cycle Time | 6.24 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 160 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

*Table 2-99 •* **FIFO**
**Worst Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ENS}$ | REN_B, WEN_B Setup Time | 4.13 | ns |
| $t_{ENH}$ | REN_B, WEN_B Hold Time | 0.31 | ns |
| $t_{BKS}$ | BLK_B Setup Time | 0.30 | ns |
| $t_{BKH}$ | BLK_B Hold Time | 0.00 | ns |
| $t_{DS}$ | Input Data (DI) Setup Time | 1.56 | ns |
| $t_{DH}$ | Input Data (DI) Hold Time | 0.49 | ns |
| $t_{CKQ1}$ | Clock HIGH to New Data Valid on DO (flow-through) | 6.80 | ns |
| $t_{CKQ2}$ | Clock HIGH to New Data Valid on DO (pipelined) | 3.62 | ns |
| $t_{RCKEF}$ | RCLK HIGH to Empty Flag Valid | 7.23 | ns |
| $t_{WCKFF}$ | WCLK HIGH to Full Flag Valid | 6.85 | ns |
| $t_{CKAF}$ | Clock HIGH to Almost Empty/Full Flag Valid | 26.61 | ns |
| $t_{RSTFG}$ | RESET_B LOW to Empty/Full Flag Valid | 7.12 | ns |
| $t_{RSTAF}$ | RESET_B LOW to Almost Empty/Full Flag Valid | 26.33 | ns |
| $t_{RSTBQ}$ | RESET_B LOW to Data Out LOW on DO (flow-through) | 4.09 | ns |
|  | RESET_B LOW to Data Out LOW on DO (pipelined) | 4.09 | ns |
| $t_{REMRSTB}$ | RESET_B Removal | 1.23 | ns |
| $t_{RECRSTB}$ | RESET_B Recovery | 6.58 | ns |
| $t_{MPWRSTB}$ | RESET_B Minimum Pulse Width | 1.18 | ns |
| $t_{CYC}$ | Clock Cycle Time | 10.90 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 92 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

# Embedded FlashROM Characteristics

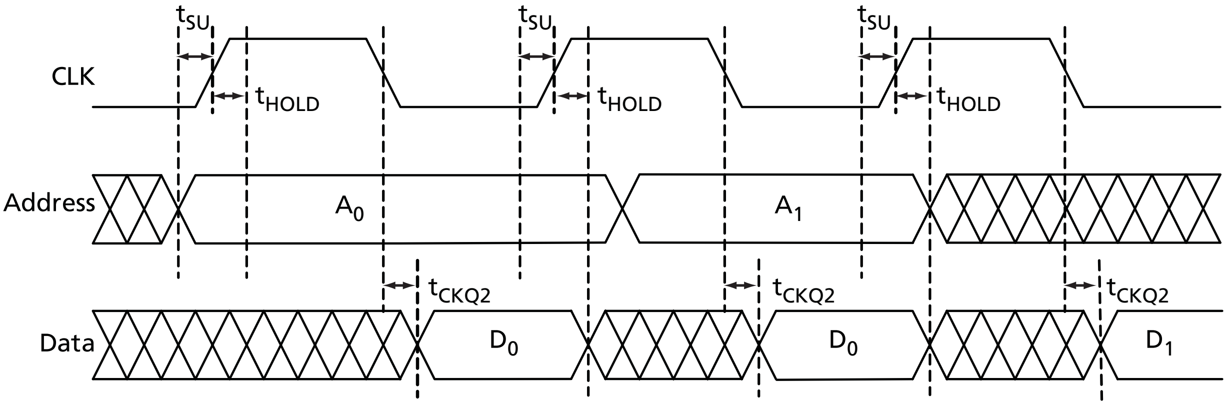


*Figure 2-39* • **Timing Diagram**

## *Timing Characteristics*

### 1.5 V DC Core Voltage

*Table 2-100* • **Embedded FlashROM Access Time**
**Worst Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{SU}$ | Address Setup Time | 0.57 | ns |
| $t_{HOLD}$ | Address Hold Time | 0.00 | ns |
| $t_{CK2Q}$ | Clock to Out | 20.90 | ns |
| $F_{MAX}$ | Maximum Clock Frequency | 15 | MHz |

### 1.2 V DC Core Voltage

*Table 2-101* • **Embedded FlashROM Access Time**
**Worst Commercial-Case Conditions: $T_J$ = 70°C, $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{SU}$ | Address Setup Time | 0.59 | ns |
| $t_{HOLD}$ | Address Hold Time | 0.00 | ns |
| $t_{CK2Q}$ | Clock to Out | 35.74 | ns |
| $F_{MAX}$ | Maximum Clock Frequency | 10 | MHz |

# JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

## *Timing Characteristics*

### 1.5 V DC Core Voltage

***Table 2-102* • JTAG 1532**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DISU}$ | Test Data Input Setup Time | 1.00 | ns |
| $t_{DIHD}$ | Test Data Input Hold Time | 2.00 | ns |
| $t_{TMSSU}$ | Test Mode Select Setup Time | 1.00 | ns |
| $t_{TMDHD}$ | Test Mode Select Hold Time | 2.00 | ns |
| $t_{TCK2Q}$ | Clock to Q (data out) | 8.00 | ns |
| $t_{RSTB2Q}$ | Reset to Q (data out) | 25.00 | ns |
| $F_{TCKMAX}$ | TCK Maximum Frequency | 15 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 0.58 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.00 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

***Table 2-103* • JTAG 1532**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case $V_{CC}$ = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DISU}$ | Test Data Input Setup Time | 1.50 | ns |
| $t_{DIHD}$ | Test Data Input Hold Time | 3.00 | ns |
| $t_{TMSSU}$ | Test Mode Select Setup Time | 1.50 | ns |
| $t_{TMDHD}$ | Test Mode Select Hold Time | 3.00 | ns |
| $t_{TCK2Q}$ | Clock to Q (data out) | 11.00 | ns |
| $t_{RSTB2Q}$ | Reset to Q (data out) | 30.00 | ns |
| $F_{TCKMAX}$ | TCK Maximum Frequency | 9.00 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 1.18 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.00 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Part Number and Revision Date

Part Number 51700110-002-1
Revised November 2008

## List of Changes

The following table lists critical changes that were made in the current version of the chapter.

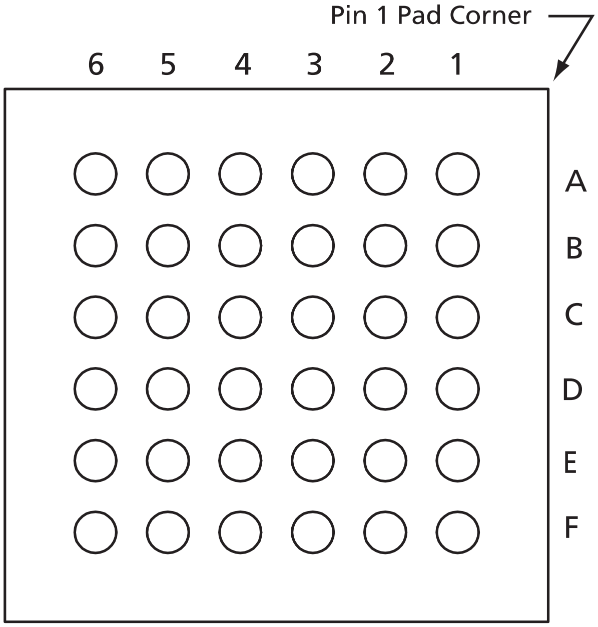
| Previous Version | Changes in Current Version (Advance v0.2) | Page |
|---|---|---|
| Advance v0.1 (October 2008) | The table notes and references were revised in Table 2-2 · Recommended Operating Conditions[1]. VMV was included with $V_{CCI}$ and a table note was added stating, "VMV pins must be connected to the corresponding $V_{CCI}$ pins. See *Pin Descriptions* for further information." Please review carefully. | 2-2 |
| | $V_{JTAG}$ was added to the list in the table note for Table 2-8 · Quiescent Supply Current ($I_{DD}$) Characteristics, IGLOO nano Flash*Freeze Mode*. Values were added for AGLN010, AGLN015, and AGLN030 for 1.5 V. | 2-7 |
| | $V_{CCI}$ was removed from the list in the table note for Table 2-9 · Quiescent Supply Current ($I_{DD}$) Characteristics, IGLOO nano Sleep Mode (VCC = 0 V)*. | 2-7 |
| | Values for $I_{CCA}$ current were updated for AGLN010, AGLN015, and AGLN030 in Table 2-11 · Quiescent Supply Current ($I_{DD}$), No IGLOO nano Flash*Freeze Mode1. | 2-8 |
| | Values for PAC1 and PAC2 were added to Table 2-14 · Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices and Table 2-16 · Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices. | 2-10,<br>2-11 |
| | Table notes regarding wide range support were added to Table 2-20 · Summary of Maximum and Minimum DC Input and Output Levels. | 2-19 |
| | 1.2 V LVCMOS wide range values were added to Table 2-21 · Summary of Maximum and Minimum DC Input Levels and Table 2-22 · Summary of AC Measuring Points. | 2-19,<br>2-20 |
| | The following table note was added to Table 2-24 · Summary of I/O Timing Characteristics—Software Default Settings and Table 2-25 · Summary of I/O Timing Characteristics—Software Default Settings: "All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification." | 2-21 |
| | 3.3 V LVCMOS Wide Range and 1.2 V Wide Range were added to Table 2-27 · I/O Output Buffer Maximum Resistances[1] andTable 2-29 · I/O Short Currents IOSH/IOSL. | 2-22,<br>2-23 |

## Actel Safety Critical, Life Support, and High-Reliability Applications Policy

The Actel products described in this advance status datasheet may not have completed Actel's qualification process. Actel may amend or enhance products during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any Actel product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult Actel's Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of Actel's products is available on the Actel website at http://www.actel.com/documents/ORT_Report.pdf. Actel also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local Actel sales office for additional reliability information.

# 3 – Package Pin Assignments

## 36-Pin UC



*Note: This is the bottom view of the package.*

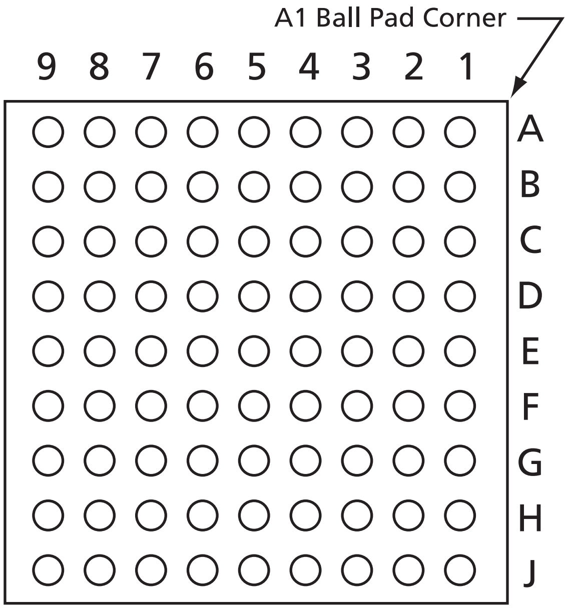
***Figure 3-1 •***

### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

| 36-Pin UC | |
|---|---|
| **Pin Number** | **AGLN010 Function** |
| A1 | IO21RSB1 |
| A2 | IO18RSB1 |
| A3 | IO13RSB1 |
| A4 | GDC0/IO00RSB0 |
| A5 | IO06RSB0 |
| A6 | GDA0/IO04RSB0 |
| B1 | GEC0/IO37RSB1 |
| B2 | IO20RSB1 |
| B3 | IO15RSB1 |
| B4 | IO09RSB0 |
| B5 | IO08RSB0 |
| B6 | IO07RSB0 |
| C1 | IO22RSB1 |
| C2 | GEA0/IO34RSB1 |
| C3 | GND |
| C4 | GND |
| C5 | $V_{CCI}$B0 |
| C6 | IO02RSB0 |
| D1 | IO33RSB1 |
| D2 | $V_{CCI}$B1 |
| D3 | $V_{CC}$ |
| D4 | $V_{CC}$ |
| D5 | IO10RSB0 |
| D6 | IO11RSB0 |
| E1 | IO32RSB1 |
| E2 | FF/IO31RSB1 |
| E3 | TCK |
| E4 | $V_{PUMP}$ |
| E5 | TRST |
| E6 | $V_{JTAG}$ |
| F1 | IO29RSB1 |
| F2 | IO25RSB1 |
| F3 | IO23RSB1 |
| F4 | TDI |
| F5 | TMS |
| F6 | TDO |

# 81-Pin UC



Note: *This is the bottom view of the package.*

***Figure 3-2 •***

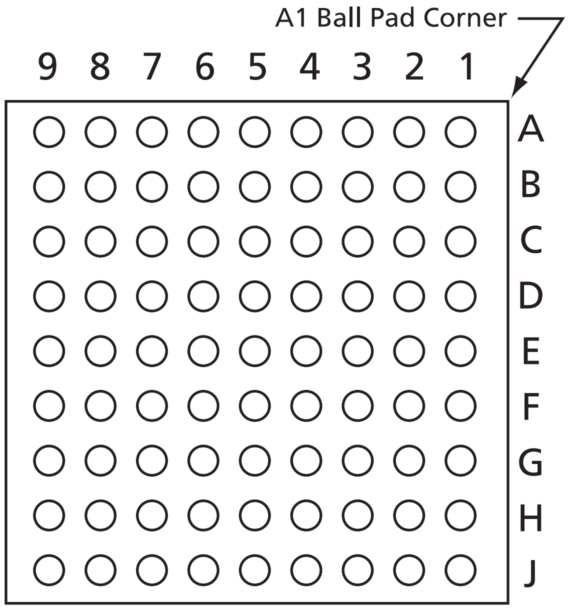
## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

## *Pin Assignments*

Pin assignments for the 81-Pin UC package will be published in a future version of this document.

# 81-Pin CS



*Note: This is the bottom view of the package.*

***Figure 3-3 •***

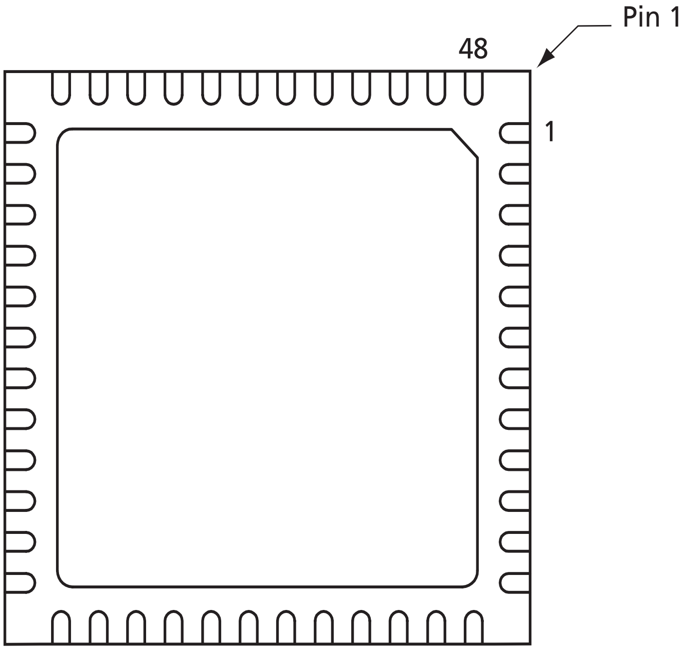
### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

### *Pin Assignments*

Pin assignments for the 81-Pin CS package will be published in a future version of this document.

## 48-Pin QFN



*Notes:*

1. *This is the bottom view of the package.*
2. *The die attach paddle of the package is tied to ground (GND).*

***Figure 3-4 •***

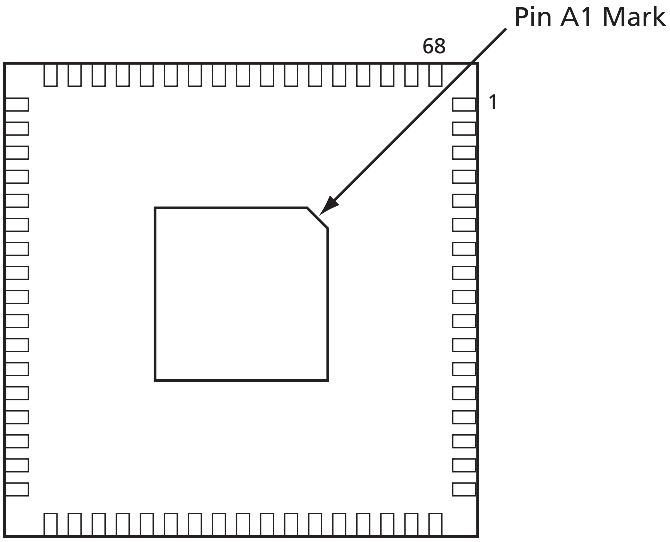
### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

| 48-Pin QFN | |
|---|---|
| **Pin Number** | **AGLN010 Function** |
| 1 | GEC0/IO37RSB1 |
| 2 | IO36RSB1 |
| 3 | GEA0/IO34RSB1 |
| 4 | IO22RSB1 |
| 5 | GND |
| 6 | $V_{CCI}$B1 |
| 7 | IO24RSB1 |
| 8 | IO33RSB1 |
| 9 | IO26RSB1 |
| 10 | IO32RSB1 |
| 11 | IO27RSB1 |
| 12 | IO29RSB1 |
| 13 | IO30RSB1 |
| 14 | FF/IO31RSB1 |
| 15 | IO28RSB1 |
| 16 | IO25RSB1 |
| 17 | IO23RSB1 |
| 18 | $V_{CC}$ |
| 19 | $V_{CCI}$B1 |
| 20 | IO17RSB1 |
| 21 | IO14RSB1 |
| 22 | TCK |
| 23 | TDI |
| 24 | TMS |
| 25 | $V_{PUMP}$ |
| 26 | TDO |
| 27 | TRST |
| 28 | $V_{JTAG}$ |
| 29 | IO11RSB0 |
| 30 | IO10RSB0 |
| 31 | IO09RSB0 |
| 32 | IO08RSB0 |
| 33 | $V_{CCI}$B0 |
| 34 | GND |
| 35 | $V_{CC}$ |
| 36 | IO07RSB0 |

| 48-Pin QFN | |
|---|---|
| **Pin Number** | **AGLN010 Function** |
| 37 | IO06RSB0 |
| 38 | GDA0/IO05RSB0 |
| 39 | IO03RSB0 |
| 40 | GDC0/IO01RSB0 |
| 41 | IO12RSB1 |
| 42 | IO13RSB1 |
| 43 | IO15RSB1 |
| 44 | IO16RSB1 |
| 45 | IO18RSB1 |
| 46 | IO19RSB1 |
| 47 | IO20RSB1 |
| 48 | IO21RSB1 |

# 68-Pin QFN



Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle of the package is tied to ground (GND).*

***Figure 3-5 •***

## *Note*

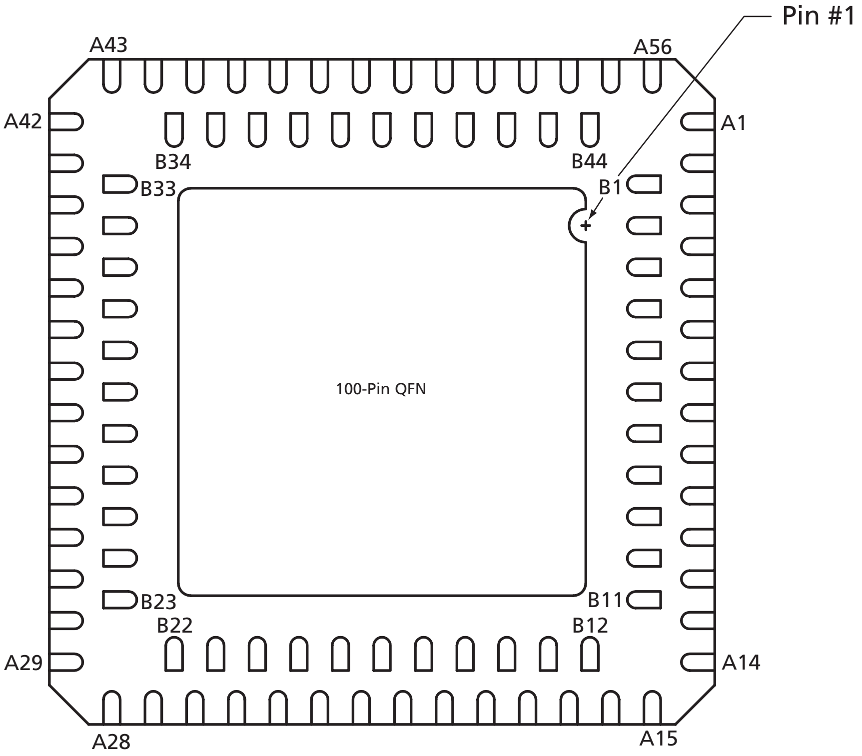
For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

| 68-Pin QFN | |
|---|---|
| Pin Number | AGLN015 Function |
| 1 | IO60RSB2 |
| 2 | IO54RSB2 |
| 3 | IO52RSB2 |
| 4 | IO50RSB2 |
| 5 | IO49RSB2 |
| 6 | GEC0/IO48RSB2 |
| 7 | GEA0/IO47RSB2 |
| 8 | $V_{CC}$ |
| 9 | GND |
| 10 | $V_{CCI}$B2 |
| 11 | IO46RSB2 |
| 12 | IO45RSB2 |
| 13 | IO44RSB2 |
| 14 | IO43RSB2 |
| 15 | IO42RSB2 |
| 16 | IO41RSB2 |
| 17 | IO40RSB2 |
| 18 | FF/IO39RSB1 |
| 19 | IO37RSB1 |
| 20 | IO35RSB1 |
| 21 | IO33RSB1 |
| 22 | IO31RSB1 |
| 23 | IO30RSB1 |
| 24 | $V_{CC}$ |
| 25 | GND |
| 26 | $V_{CCI}$B1 |
| 27 | IO27RSB1 |
| 28 | IO25RSB1 |
| 29 | IO23RSB1 |
| 30 | IO21RSB1 |
| 31 | IO19RSB1 |
| 32 | TCK |
| 33 | TDI |
| 34 | TMS |
| 35 | $V_{PUMP}$ |
| 36 | TDO |
| 37 | TRST |
| 38 | $V_{JTAG}$ |
| 39 | IO17RSB0 |
| 40 | IO16RSB0 |
| 41 | GDA0/IO15RSB0 |
| 42 | GDC0/IO14RSB0 |
| 43 | IO13RSB0 |
| 44 | $V_{CCI}$B0 |
| 45 | GND |
| 46 | $V_{CC}$ |
| 47 | IO12RSB0 |
| 48 | IO11RSB0 |
| 49 | IO09RSB0 |
| 50 | IO05RSB0 |
| 51 | IO00RSB0 |
| 52 | IO07RSB0 |
| 53 | IO03RSB0 |
| 54 | IO18RSB1 |
| 55 | IO20RSB1 |
| 56 | IO22RSB1 |
| 57 | IO24RSB1 |
| 58 | IO28RSB1 |
| 59 | NC |
| 60 | GND |
| 61 | NC |
| 62 | IO32RSB1 |
| 63 | IO34RSB1 |
| 64 | IO36RSB1 |
| 65 | IO61RSB2 |
| 66 | IO58RSB2 |
| 67 | IO56RSB2 |
| 68 | IO63RSB2 |

| 68-Pin QFN | |
|---|---|
| **Pin Number** | **AGLN020 Function** |
| 1 | IO60RSB2 |
| 2 | IO54RSB2 |
| 3 | IO52RSB2 |
| 4 | IO50RSB2 |
| 5 | IO49RSB2 |
| 6 | GEC0/IO48RSB2 |
| 7 | GEA0/IO47RSB2 |
| 8 | $V_{CC}$ |
| 9 | GND |
| 10 | $V_{CCI}$B2 |
| 11 | IO46RSB2 |
| 12 | IO45RSB2 |
| 13 | IO44RSB2 |
| 14 | IO43RSB2 |
| 15 | IO42RSB2 |
| 16 | IO41RSB2 |
| 17 | IO40RSB2 |
| 18 | FF/IO39RSB1 |
| 19 | IO37RSB1 |
| 20 | IO35RSB1 |
| 21 | IO33RSB1 |
| 22 | IO31RSB1 |
| 23 | IO30RSB1 |
| 24 | $V_{CC}$ |
| 25 | GND |
| 26 | $V_{CCI}$B1 |
| 27 | IO27RSB1 |
| 28 | IO25RSB1 |
| 29 | IO23RSB1 |
| 30 | IO21RSB1 |
| 31 | IO19RSB1 |
| 32 | TCK |
| 33 | TDI |
| 34 | TMS |
| 35 | $V_{PUMP}$ |
| 36 | TDO |

| 68-Pin QFN | |
|---|---|
| **Pin Number** | **AGLN020 Function** |
| 37 | TRST |
| 38 | $V_{JTAG}$ |
| 39 | IO17RSB0 |
| 40 | IO16RSB0 |
| 41 | GDA0/IO15RSB0 |
| 42 | GDC0/IO14RSB0 |
| 43 | IO13RSB0 |
| 44 | $V_{CCI}$B0 |
| 45 | GND |
| 46 | $V_{CC}$ |
| 47 | IO12RSB0 |
| 48 | IO11RSB0 |
| 49 | IO09RSB0 |
| 50 | IO05RSB0 |
| 51 | IO00RSB0 |
| 52 | IO07RSB0 |
| 53 | IO03RSB0 |
| 54 | IO18RSB1 |
| 55 | IO20RSB1 |
| 56 | IO22RSB1 |
| 57 | IO24RSB1 |
| 58 | IO28RSB1 |
| 59 | NC |
| 60 | GND |
| 61 | NC |
| 62 | IO32RSB1 |
| 63 | IO34RSB1 |
| 64 | IO36RSB1 |
| 65 | IO61RSB2 |
| 66 | IO58RSB2 |
| 67 | IO56RSB2 |
| 68 | IO63RSB2 |

# 100-Pin QFN



*Notes:*

1. *This is the bottom view of the package.*
2. *The die attach paddle of the package is tied to ground (GND).*

***Figure 3-6 •***

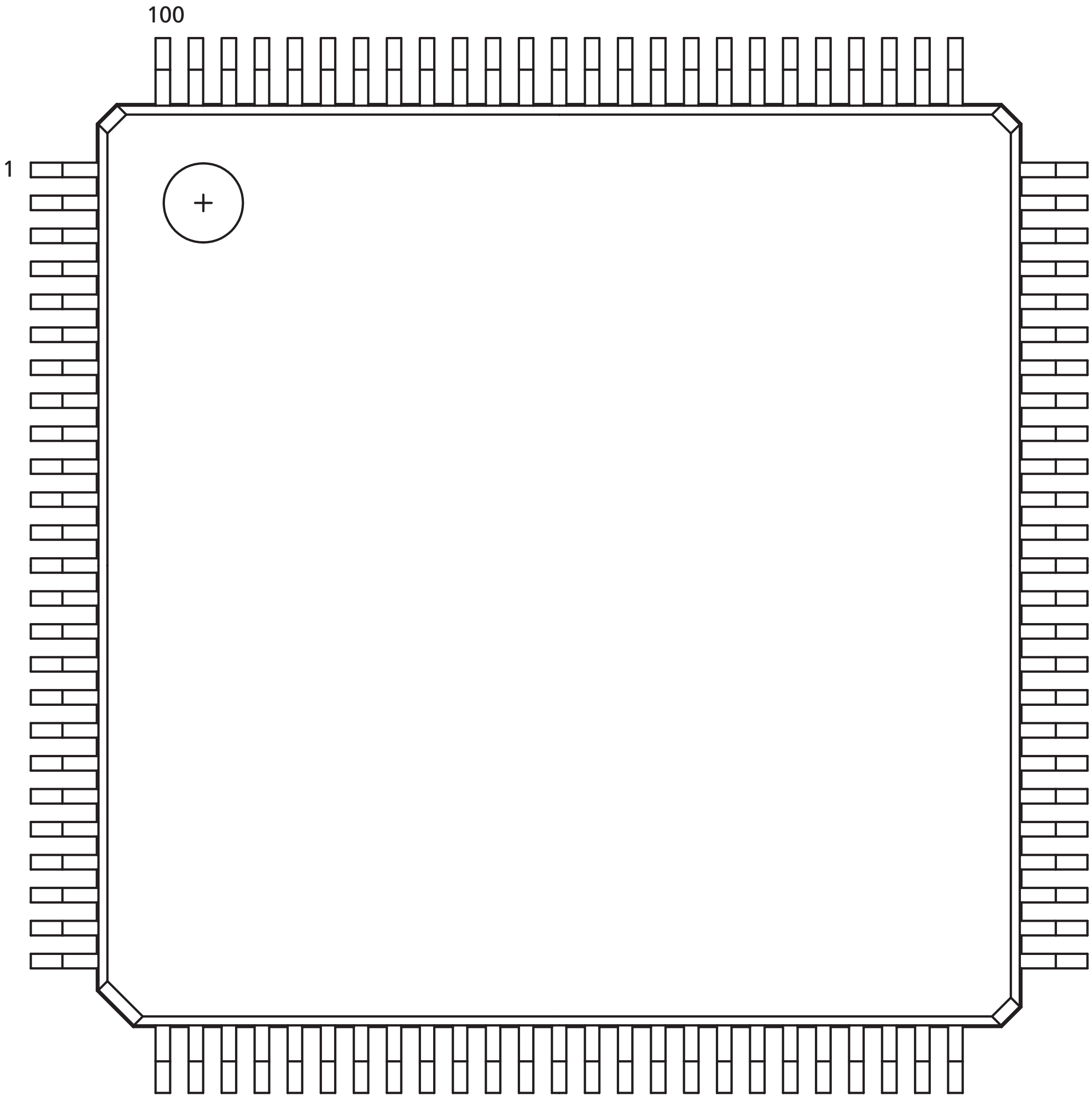
### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

### *Pin Assignments*

Pin assignments for the 100-Pin QFN package will be published in a future version of this document.

## 100-Pin VQFP



*Note: This is the top view of the package.*

***Figure 3-7 •***

### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

| 100-Pin VQFP | |
|---|---|
| **Pin Number** | **AGLN060 Function** |
| 1 | GND |
| 2 | GAA2/IO51RSB1 |
| 3 | IO52RSB1 |
| 4 | GAB2/IO53RSB1 |
| 5 | IO95RSB1 |
| 6 | GAC2/IO94RSB1 |
| 7 | IO93RSB1 |
| 8 | IO92RSB1 |
| 9 | GND |
| 10 | GFB1/IO87RSB1 |
| 11 | GFB0/IO86RSB1 |
| 12 | $V_{COMPLF}$ |
| 13 | GFA0/IO85RSB1 |
| 14 | $V_{CCPLF}$ |
| 15 | GFA1/IO84RSB1 |
| 16 | GFA2/IO83RSB1 |
| 17 | $V_{CC}$ |
| 18 | $V_{CCI}$B1 |
| 19 | GEC1/IO77RSB1 |
| 20 | GEB1/IO75RSB1 |
| 21 | GEB0/IO74RSB1 |
| 22 | GEA1/IO73RSB1 |
| 23 | GEA0/IO72RSB1 |
| 24 | VMV1 |
| 25 | GNDQ |
| 26 | GEA2/IO71RSB1 |
| 27 | FF/GEB2/IO70RSB1 |
| 28 | GEC2/IO69RSB1 |
| 29 | IO68RSB1 |
| 30 | IO67RSB1 |
| 31 | IO66RSB1 |
| 32 | IO65RSB1 |
| 33 | IO64RSB1 |
| 34 | IO63RSB1 |
| 35 | IO62RSB1 |
| 36 | IO61RSB1 |
| 37 | $V_{CC}$ |
| 38 | GND |
| 39 | $V_{CCI}$B1 |
| 40 | IO60RSB1 |
| 41 | IO59RSB1 |
| 42 | IO58RSB1 |
| 43 | IO57RSB1 |
| 44 | GDC2/IO56RSB1 |
| 45 | GDB2/IO55RSB1 |
| 46 | GDA2/IO54RSB1 |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | VMV1 |
| 51 | GND |
| 52 | $V_{PUMP}$ |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | $V_{JTAG}$ |
| 57 | GDA1/IO49RSB0 |
| 58 | GDC0/IO46RSB0 |
| 59 | GDC1/IO45RSB0 |
| 60 | GCC2/IO43RSB0 |
| 61 | GCB2/IO42RSB0 |
| 62 | GCA0/IO40RSB0 |
| 63 | GCA1/IO39RSB0 |
| 64 | GCC0/IO36RSB0 |
| 65 | GCC1/IO35RSB0 |
| 66 | $V_{CCI}$B0 |
| 67 | GND |
| 68 | $V_{CC}$ |
| 69 | IO31RSB0 |
| 70 | GBC2/IO29RSB0 |
| 71 | GBB2/IO27RSB0 |
| 72 | IO26RSB0 |
| 73 | GBA2/IO25RSB0 |
| 74 | VMV0 |
| 75 | GNDQ |
| 76 | GBA1/IO24RSB0 |
| 77 | GBA0/IO23RSB0 |
| 78 | GBB1/IO22RSB0 |
| 79 | GBB0/IO21RSB0 |
| 80 | GBC1/IO20RSB0 |
| 81 | GBC0/IO19RSB0 |
| 82 | IO18RSB0 |
| 83 | IO17RSB0 |
| 84 | IO15RSB0 |
| 85 | IO13RSB0 |
| 86 | IO11RSB0 |
| 87 | $V_{CCI}$B0 |
| 88 | GND |
| 89 | $V_{CC}$ |
| 90 | IO10RSB0 |
| 91 | IO09RSB0 |
| 92 | IO08RSB0 |
| 93 | GAC1/IO07RSB0 |
| 94 | GAC0/IO06RSB0 |
| 95 | GAB1/IO05RSB0 |
| 96 | GAB0/IO04RSB0 |
| 97 | GAA1/IO03RSB0 |
| 98 | GAA0/IO02RSB0 |
| 99 | IO01RSB0 |
| 100 | IO00RSB0 |

| 100-Pin VQFP | |
|---|---|
| Pin Number | AGLN125 Function |
| 1 | GND |
| 2 | GAA2/IO67RSB1 |
| 3 | IO68RSB1 |
| 4 | GAB2/IO69RSB1 |
| 5 | IO132RSB1 |
| 6 | GAC2/IO131RSB1 |
| 7 | IO130RSB1 |
| 8 | IO129RSB1 |
| 9 | GND |
| 10 | GFB1/IO124RSB1 |
| 11 | GFB0/IO123RSB1 |
| 12 | $V_{COMPLF}$ |
| 13 | GFA0/IO122RSB1 |
| 14 | $V_{CCPLF}$ |
| 15 | GFA1/IO121RSB1 |
| 16 | GFA2/IO120RSB1 |
| 17 | $V_{CC}$ |
| 18 | $V_{CCI}$B1 |
| 19 | GEC0/IO111RSB1 |
| 20 | GEB1/IO110RSB1 |
| 21 | GEB0/IO109RSB1 |
| 22 | GEA1/IO108RSB1 |
| 23 | GEA0/IO107RSB1 |
| 24 | VMV1 |
| 25 | GNDQ |
| 26 | GEA2/IO106RSB1 |
| 27 | FF/GEB2/IO105RSB1 |
| 28 | GEC2/IO104RSB1 |
| 29 | IO102RSB1 |
| 30 | IO100RSB1 |
| 31 | IO99RSB1 |
| 32 | IO97RSB1 |
| 33 | IO96RSB1 |
| 34 | IO95RSB1 |
| 35 | IO94RSB1 |
| 36 | IO93RSB1 |
| 37 | $V_{CC}$ |
| 38 | GND |
| 39 | $V_{CCI}$B1 |
| 40 | IO87RSB1 |
| 41 | IO84RSB1 |
| 42 | IO81RSB1 |
| 43 | IO75RSB1 |
| 44 | GDC2/IO72RSB1 |
| 45 | GDB2/IO71RSB1 |
| 46 | GDA2/IO70RSB1 |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | VMV1 |
| 51 | GND |
| 52 | $V_{PUMP}$ |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | $V_{JTAG}$ |
| 57 | GDA1/IO65RSB0 |
| 58 | GDC0/IO62RSB0 |
| 59 | GDC1/IO61RSB0 |
| 60 | GCC2/IO59RSB0 |
| 61 | GCB2/IO58RSB0 |
| 62 | GCA0/IO56RSB0 |
| 63 | GCA1/IO55RSB0 |
| 64 | GCC0/IO52RSB0 |
| 65 | GCC1/IO51RSB0 |
| 66 | $V_{CCI}$B0 |
| 67 | GND |
| 68 | $V_{CC}$ |
| 69 | IO47RSB0 |
| 70 | GBC2/IO45RSB0 |
| 71 | GBB2/IO43RSB0 |
| 72 | IO42RSB0 |
| 73 | GBA2/IO41RSB0 |
| 74 | VMV0 |
| 75 | GNDQ |
| 76 | GBA1/IO40RSB0 |
| 77 | GBA0/IO39RSB0 |
| 78 | GBB1/IO38RSB0 |
| 79 | GBB0/IO37RSB0 |
| 80 | GBC1/IO36RSB0 |
| 81 | GBC0/IO35RSB0 |
| 82 | IO32RSB0 |
| 83 | IO28RSB0 |
| 84 | IO25RSB0 |
| 85 | IO22RSB0 |
| 86 | IO19RSB0 |
| 87 | $V_{CCI}$B0 |
| 88 | GND |
| 89 | $V_{CC}$ |
| 90 | IO15RSB0 |
| 91 | IO13RSB0 |
| 92 | IO11RSB0 |
| 93 | IO09RSB0 |
| 94 | IO07RSB0 |
| 95 | GAC1/IO05RSB0 |
| 96 | GAC0/IO04RSB0 |
| 97 | GAB1/IO03RSB0 |
| 98 | GAB0/IO02RSB0 |
| 99 | GAA1/IO01RSB0 |
| 100 | GAA0/IO00RSB0 |

| 100-Pin VQFP | |
|---|---|
| **Pin Number** | **AGLN250 Function** |
| 1 | GND |
| 2 | GAA2/IO67RSB3 |
| 3 | IO66RSB3 |
| 4 | GAB2/IO65RSB3 |
| 5 | IO64RSB3 |
| 6 | GAC2/IO63RSB3 |
| 7 | IO62RSB3 |
| 8 | IO61RSB3 |
| 9 | GND |
| 10 | GFB1/IO60RSB3 |
| 11 | GFB0/IO59RSB3 |
| 12 | $V_{COMPLF}$ |
| 13 | GFA0/IO57RSB3 |
| 14 | $V_{CCPLF}$ |
| 15 | GFA1/IO58RSB3 |
| 16 | GFA2/IO56RSB3 |
| 17 | $V_{CC}$ |
| 18 | $V_{CCI}$B3 |
| 19 | GFC2/IO55RSB3 |
| 20 | GEC1/IO54RSB3 |
| 21 | GEC0/IO53RSB3 |
| 22 | GEA1/IO52RSB3 |
| 23 | GEA0/IO51RSB3 |
| 24 | VMV3 |
| 25 | GNDQ |
| 26 | GEA2/IO50RSB2 |
| 27 | FF/GEB2/IO49RSB2 |
| 28 | GEC2/IO48RSB2 |
| 29 | IO47RSB2 |
| 30 | IO46RSB2 |
| 31 | IO45RSB2 |
| 32 | IO44RSB2 |
| 33 | IO43RSB2 |
| 34 | IO42RSB2 |
| 35 | IO41RSB2 |
| 36 | IO40RSB2 |
| 37 | $V_{CC}$ |
| 38 | GND |
| 39 | $V_{CCI}$B2 |
| 40 | IO39RSB2 |
| 41 | IO38RSB2 |
| 42 | IO37RSB2 |
| 43 | GDC2/IO36RSB2 |
| 44 | GDB2/IO35RSB2 |
| 45 | GDA2/IO34RSB2 |
| 46 | GNDQ |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | VMV2 |
| 51 | GND |
| 52 | $V_{PUMP}$ |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | $V_{JTAG}$ |
| 57 | GDA1/IO33RSB1 |
| 58 | GDC0/IO32RSB1 |
| 59 | GDC1/IO31RSB1 |
| 60 | IO30RSB1 |
| 61 | GCB2/IO29RSB1 |
| 62 | GCA1/IO27RSB1 |
| 63 | GCA0/IO28RSB1 |
| 64 | GCC0/IO26RSB1 |
| 65 | GCC1/IO25RSB1 |
| 66 | $V_{CCI}$B1 |
| 67 | GND |
| 68 | $V_{CC}$ |
| 69 | IO24RSB1 |
| 70 | GBC2/IO23RSB1 |
| 71 | GBB2/IO22RSB1 |
| 72 | IO21RSB1 |
| 73 | GBA2/IO20RSB1 |
| 74 | VMV1 |
| 75 | GNDQ |
| 76 | GBA1/IO19RSB0 |
| 77 | GBA0/IO18RSB0 |
| 78 | GBB1/IO17RSB0 |
| 79 | GBB0/IO16RSB0 |
| 80 | GBC1/IO15RSB0 |
| 81 | GBC0/IO14RSB0 |
| 82 | IO13RSB0 |
| 83 | IO12RSB0 |
| 84 | IO11RSB0 |
| 85 | IO10RSB0 |
| 86 | IO09RSB0 |
| 87 | $V_{CCI}$B0 |
| 88 | GND |
| 89 | $V_{CC}$ |
| 90 | IO08RSB0 |
| 91 | IO07RSB0 |
| 92 | IO06RSB0 |
| 93 | GAC1/IO05RSB0 |
| 94 | GAC0/IO04RSB0 |
| 95 | GAB1/IO03RSB0 |
| 96 | GAB0/IO02RSB0 |
| 97 | GAA1/IO01RSB0 |
| 98 | GAA0/IO00RSB0 |
| 99 | GNDQ |
| 100 | VMV0 |

## Part Number and Revision Date

Part Number 51700110-003-2
Revised December 2008

## List of Changes

The following table lists critical changes that were made in the current version of the chapter.

| Previous Version | Changes in Current Version (Advance v0.3) | Page |
|---|---|---|
| Advance v0.2 (November 2008) | The "36-Pin UC" pin table is new. | 3-2 |
| Advance v0.1 (October 2008) | The "48-Pin QFN" pin diagram was revised. | 3-5 |
| | Note 2 for the "48-Pin QFN", "68-Pin QFN", and "100-Pin QFN" pin diagrams was changed to "The die attach paddle of the package is tied to ground (GND)." | 3-5, 3-7, 3-10 |
| | The "100-Pin VQFP" pin diagram was revised to move the pin IDs to the upper left corner instead of the upper right corner. | 3-11 |

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