HARRIS

2N6896

P-Channel Enhancement-Mode Power MOS Field-Effect Transistors

August 1991

Features

- -6A, -100V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

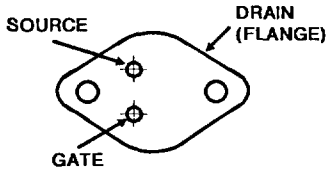
Description

The 2N6896 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

The 2N6896 is supplied in the JEDEC TO-204AA metal package.

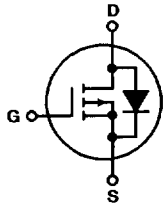
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6896	UNITS
Drain-Source Voltage	V_{DSS}	-100*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	-100*	V
Continuous Drain Current			
RMS Continuous	I_D	-6*	A
Pulsed Drain Current	I_{DM}	-20*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	60*	W
Above T_C = +25°C, Derate Linearly		0.48*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (At distances ≥ ⅛" (3.17mm) from seating plane for 10s max)	T_L	260	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **1874**

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125°C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 3.8 A, V_{GS} = -10 V	—	2.28	V
			I_D = 6 A, V_{GS} = -10 V	—	-6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 3.8 A, V_{GS} = -10 V	—	0.6	Ω
			T_C = 125°C, I_D = 3.8 A, V_{GS} = 10 V	—	0.96	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 3.8 A	1	4	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	200	800	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	100	350	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	40	150	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	60	ns
*	Rise Time	t_r	I_D = 3.8 A	—	100	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	150	
*	Fall Time	t_f	V_{GS} = -10 V	—	100	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	2.083	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 12 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, di_F/dt = 50 A/μs	—	375	ns

*In accordance with JEDEC registration data.
[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

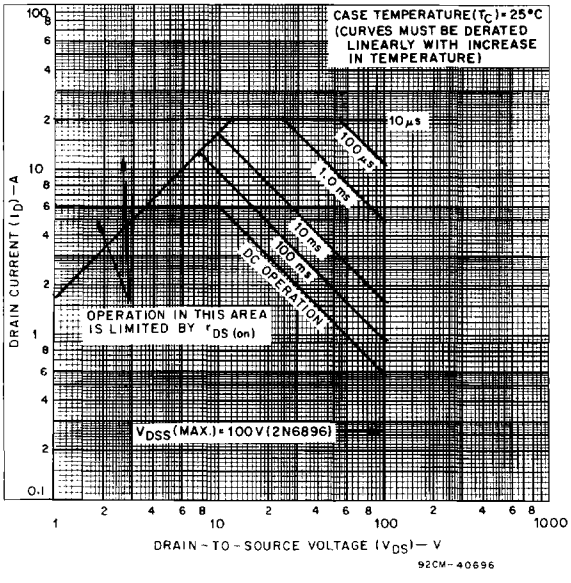


Fig. 1 - Maximum safe operating areas.

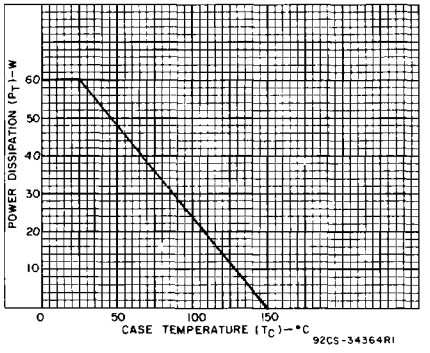


Fig. 2 - Power dissipation vs. temperature derating curve.

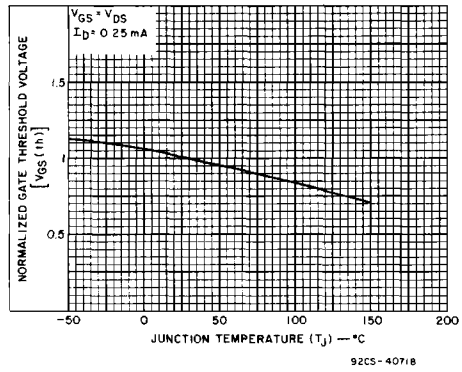


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

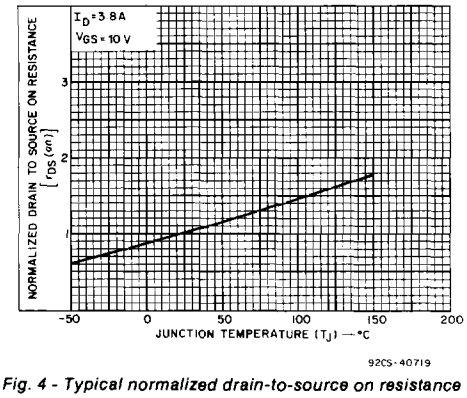


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

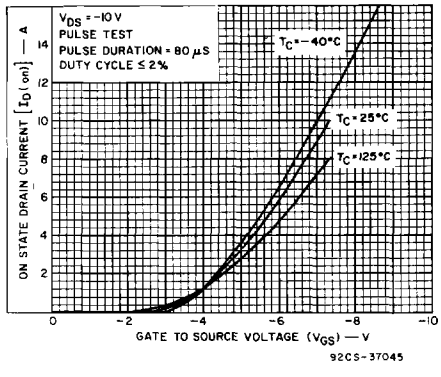


Fig. 5 - Typical transfer characteristics.

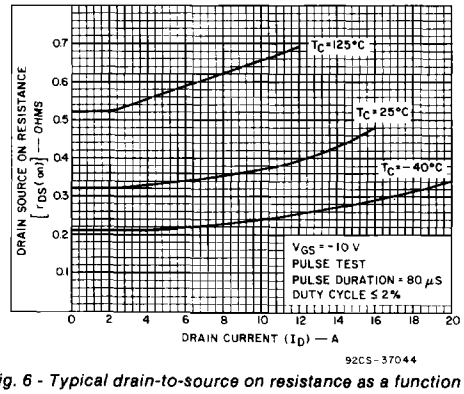


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

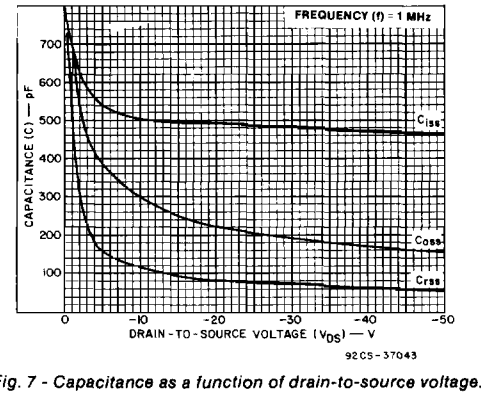


Fig. 7 - Capacitance as a function of drain-to-source voltage.

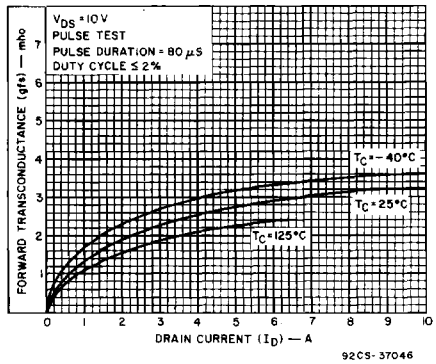


Fig. 8 - Typical forward transconductance as a function of drain current.