TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VHCT9125AFT,TC74VHCT9125AFK TC74VHCT9126AFT,TC74VHCT9126AFK

TC74VHCT9125AFT/FK5-bit Universal Schmitt Buffer with 3-State OutputsTC74VHCT9126AFT/FK5-bit Universal Schmitt Buffer with 3-State Outputs

The TC74VHCT9125A/9126A are an ultra-high-speed 5-bit Schmitt buffer fabricated using silicon-gate CMOS technology. The TC74VHCT9125A/9126A combines low power consumption of CMOS with Schottky TTL speeds.

The input voltage are compatible with TTL output voltage.

This device may be used as a level converter for interfacing 3.3 V to 5 V system.

Y1 to Y4 outputs can be put in the high-impedance state by placing a logic HIGH on the Enable  $(\overline{G})$  input. The CONT input determines the logical inversion of data.A logic LOW on the CONT input configures the TC74VHC9125A/9126A as an inverter; a logic HIGH on the CONT input configures the TC74VHCT9125A/9126A as a buffer.

TC74VHCT9125A Y5 output is an inverting type, and the TC74VHCT9126A Y5 output is a non-inverting type.

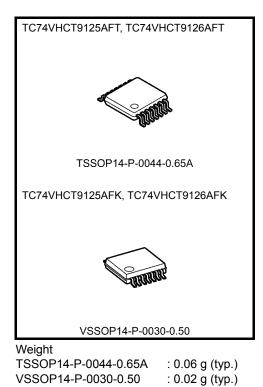
All the inputs have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHC9125A/9126A are capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, etc.

Note: Output in off-state

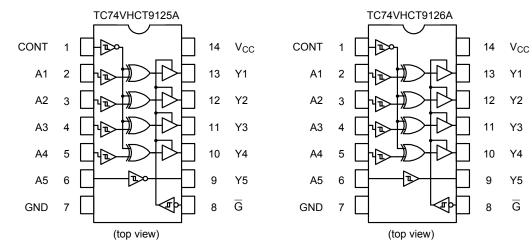
#### Features

- High speed:  $t_{pd} = 6.6 \text{ ns} (typ.) (V_{CC} = 5 \text{ V})$
- Low supply current:  $I_{CC} = 2 \mu A (max) (Ta = 25^{\circ}C)$
- Compatible with TTL inputs  $V_{IL} = 0.5 V (max)$ 
  - $V_{IH} = 2.1 V (min)$
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{pLH} \simeq t_{pHL}$
- Input terminals are at the opposite side of Output terminals



 $\overline{\mathsf{G}}$ 

# **Pin Assignment**



# **Truth Table**

	Inputs	Outputs			
G	CONT	A1~4	Y1~4		
Н	Х	Х	Z		
L	L	L	Н		
L	L	Н	L		
L	Н	L	L		
L	Н	Н	Н		

Inputs	Outputs						
A5	Y5(9125)	Y5(9126)					
L	Н	L					
Н	L	Н					

X : Don't care

Z : High impedance

### Absolute Maximum Ratings (Note1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	-0.5 to 7.0	V
DC input voltage	V <sub>IN</sub>	-0.5 to 7.0	V
DC output voltage	Varia	-0.5 to 7.0 (Note 2)	V
	Vout	-0.5 to V <sub>CC</sub> + 0.5 (Note 3)	v
Input diode current	lık	-20	mA
Output diode current	IOK	±20 (Note 4)	mA
DC output current	IOUT	±25	mA
DC V <sub>CC</sub> /ground current	ICC	±50	mA
Power dissipation	PD	180	mW
Storage temperature	T <sub>stg</sub>	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in off-state

Note 3: High or low state. IOUT absolute maximum rating must be observed.

Note 4:  $V_{OUT} < GND, V_{OUT} > V_{CC}$ 

### **Operating Ranges (Note1)**

Characteristics	Symbol	ol Rating		
Supply voltage	V <sub>CC</sub>	4.5 to 5.5	V	
Input voltage	V <sub>IN</sub>	0 to 5.5	V	
	Varia	0 to 5.5 (Note 2)		
Output voltage	Vout	0 to V <sub>CC</sub> (Note 3)	V	
Operating temperature	T <sub>opr</sub>	-40 to 85	°C	

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

Note 2: Output in off-state

Note 3: High or low state.

# **Electrical Characteristics**

#### **DC Characteristics**

Characteristics	Querrahal	Test Condition		Ta = 25°C			Ta = −40~85°C		Unit	
Characteristics	Symbol			$V_{CC}(V)$	Min	Тур	Max	Min	Max	Onit
Positive threshold VP				4.5	—	—	1.90	—	1.90	V
voltage	٧Þ		—		—	—	2.10	—	2.10	v
Negative threshold	V <sub>N</sub>			4.5	0.50	—	-	0.50	—	V
voltage	۷N			5.5	0.60	_	-	0.60	_	v
Hysteresis voltage	V <sub>H</sub>		_	4.5	0.40	—	1.40	0.40	1.40	V
Trysteresis voltage	чП		—		0.40	_	1.50	0.40	1.50	v
High-level output	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	4.5	4.4	4.5	-	4.4	_	v
voltage	чОн		I <sub>OH</sub> = −8 mA	4.5	3.94	_	-	3.80	_	
Low-level output	V <sub>OL</sub>	VIN	I <sub>OL</sub> = 50 μA	4.5	_	0.0	0.1	_	0.1	V
voltage	۷OL	= $V_{IH}$ or $V_{IL}$	I <sub>OL</sub> = 8 mA	4.5	_	_	0.36	_	0.44	v
3-state output	I <sub>OZ</sub>	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or } GND$		5.5		_	±0.25	_	±2.5	μA
off-state current	102			0.0						
Input leakage current	lin	V <sub>IN</sub> = 5.5 V or GND		0 to 5.5	_	—	±0.1	—	±1.0	μA
	Icc	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	_	_	2.0	_	20.0	μA
Quiescent supply current	ICCT	Per input: V <sub>IN</sub> = 3.4 V		5.5	_		1.35		1.50	mA
			Other input: $V_{CC}$ or GND				1.00		1.00	
Output leakage current	I <sub>OPD</sub>	V <sub>OUT</sub> = 5.5 \	/	0	—	—	0.5	—	5.0	μΑ

#### AC Characteristics (input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Tes	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
Characteristics	Ondiacteristics Symbol		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Тур.	Max	Min	Max	Unit
Propagation delay time	t <sub>pLH</sub>	_	5.0 ± 0.5	15	_	6.6	8.5	1.0	10.0	ns
(A1 to 4 - Y1 to 4)	t <sub>pHL</sub>			50	_	8.1	11.5	1.0	13.0	
Propagation delay time	t <sub>pLH</sub>		$5.0 \pm 0.5$	15	—	8.0	10.5	1.0	12.0	ns
(CONT-Y1 to 4)	tpHL	_	5.0 ± 0.5	50	—	9.9	14.5	1.0	17.0	115
Propagation delay time	t <sub>pLH</sub>		— 5.0 ± 0.5	15	_	6.0	8.0	1.0	9.5	ns
(A5 – Y5)	t <sub>pHL</sub>	_		50	_	7.9	10.5	1.0	12.0	115
3-state output enable	t <sub>pZL</sub>	R <sub>I</sub> = 1 kΩ	5.0 ± 0.5	15	—	6.4	8.5	1.0	10.0	ns
time	t <sub>pZH</sub>	KL – 1 K22	- 1 K22 5.0 ± 0.5	50	—	8.4	12.5	1.0	14.5	115
3-state output disable time	t <sub>pLZ</sub> t <sub>pHZ</sub>	R <sub>L</sub> = 1 kΩ	5.0 ± 0.5	50	_	6.7	11.5	1.0	13.0	ns
Output to output skew	t <sub>osLH</sub> t <sub>osHL</sub>	(Note 1)	5.0 ± 0.5	50	_	_	1.0	_	1.0	ns
Input capacitance	C <sub>IN</sub>		_		_	4	10	—	10	pF
Output capacitance	C <sub>OUT</sub>		_		_	9	_	_	—	pF
Power dissipation capacitance (Note 2)	CPD	f <sub>IN</sub> = 1 MHz			_	14	_	_	_	pF

Note 1: Parameter guaranteed by design.

 $t_{OSLH} = |t_{pLHm} - t_{pLHn}|, t_{OSHL} = |t_{pHLm} - t_{pHLn}|$ 

Note 2: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 5 (per bit)$ 

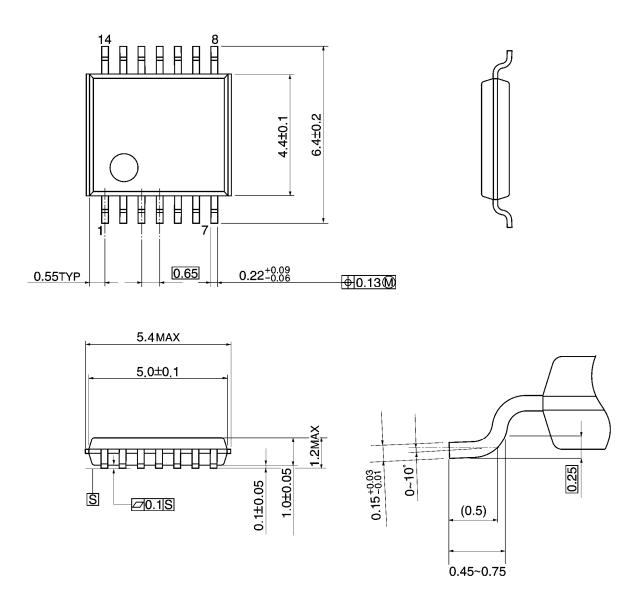
#### Noise Characteristics (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta =		25°C	Unit
Characteristics	Symbol		V <sub>CC</sub> (V)	Тур.	Limit	Unit
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	0.6	0.8	V
Quiet output minimum dynamic $V_{OL}$	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-0.2	-0.8	V
Minimum high level dynamic input voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0		2.1	V
Maximum low level dynamic input voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	_	0.5	V

# **Package Dimensions**

TSSOP14-P-0044-0.65A

Unit: mm



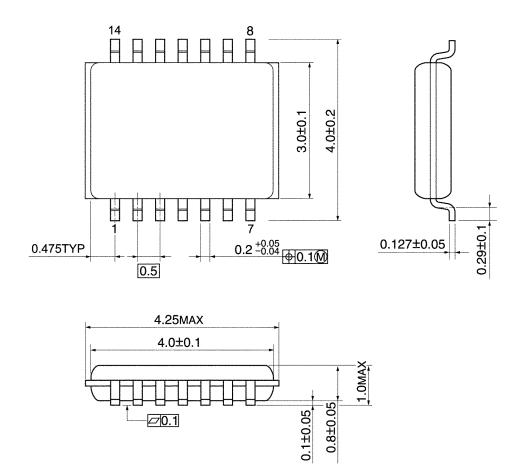
Weight: 0.06 g (typ.)

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# **Package Dimensions**

VSSOP14-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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