# Advance Information

# **Dual Mode PWM/Linear Buck Regulator**

The NCP150x is a dual mode regulator that operates either as a PWM Buck Converter or as a Low Drop Out Linear Regulator. If a synchronization signal is present, the NCP150x operates as a current mode PWM converter with synchronous rectification. The synchronization signal allows the user to control the location of the spurious frequency noise generated by a PWM converter. Linear mode is active when a synchronization signal is not present. The NCP150x configuration allows an efficient high power operation and low noise during system sleep modes.

### **Features**

- Synchronous Rectification for Higher Efficiency in PWM Mode
- Linear Mode Operation for Low Noise Output at Low Loads
- Integrated MOSFETs and Feedback Circuits
- Cycle by Cycle Current Limit
- Automatic Switching Between PWM and Linear Mode
- Operating Frequency Range of 500 to 1000 kHz
- Thermal Limit Protection
- Built-in Slope Compensation for Current Mode PWM Converter
- Fixed Output Voltages 1.05, 1.35, 1.57, 1.8 (NCP1501) 1.0, 1.3, 1.5, 1.9 (NCP1502)
- Shutdown Current Consumption of 0.2 µA

### **Typical Applications**

- Cellular Phones
- PDAs
- Pagers
- Supplies for DSP Cores
- Portable Applications

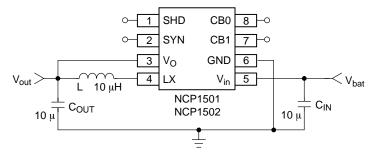


Figure 1. Typical Applications Circuit



http://onsemi.com

### MARKING DIAGRAM



Micro8<sup>™</sup> (MSOP-8) DM SUFFIX CASE 846A



x = 1 or 2

A = Assembly Location

Y = Year

W = Work Week

#### **PIN CONNECTIONS**

SHD 1	0	8	СВО
SYN 2			CB1
V <sub>O</sub> 3		6	GND
LX 4		5	$V_{in}$

(Top View)

#### ORDERING INFORMATION

Device	Package	Shipping
NCP1501DMR2	Micro8	4000/Tape & Reel
NCP1502DMR2	Micro8	4000/Tape & Reel

### **PIN FUNCTION DESCRIPTIONS**

Pin #	Symbol	Pin Description	
1	SHD	Enable Pin for the NCP150x. This pin is active high. Internal pull down resistor forces the part off if the pin is not connected on the board.	
2	SYN	External Synchronization Signal Pin. The device will operate in PWM mode if a clock signal is present. The pin must be pulled low to enter LDO mode. Internal pull down resistor on pin.	
3	Vo	Feedback for the NCP150x. An internal MOSFET is connected across V <sub>O</sub> and LX for LDO mode.	
4	LX	Connection for the pass devices to the inductor.	
5	V <sub>in</sub>	Input voltage to the NCP150x.	
6	GND	Ground Connection for the device.	
7	CB1	Voltage Selection Bit. Internal pull up resistor on pin.	
8	CB0	Voltage Selection Bit. Internal pull down resistor on pin.	

### **MAXIMUM RATINGS**

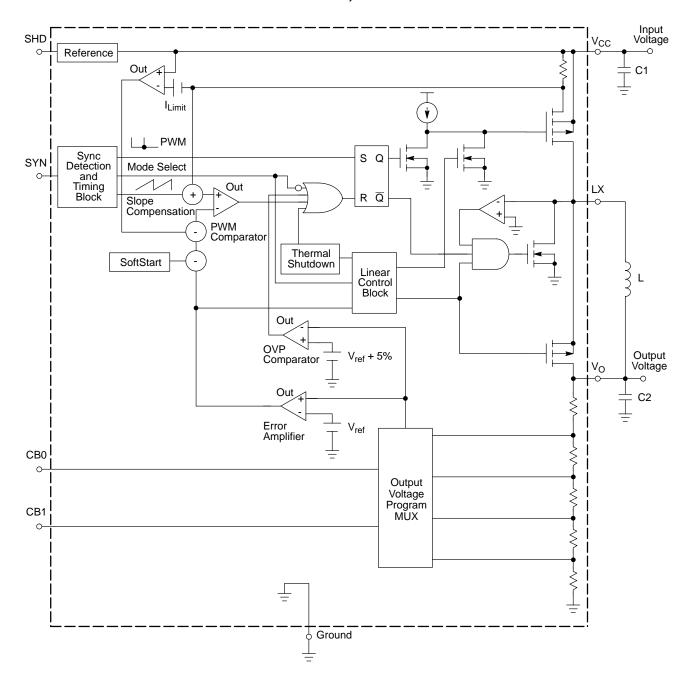
Rating	Symbol	Value	Unit
Maximum Voltage All Pins	V <sub>max</sub>	5.5	V
Maximum operating Voltage All Pins	V <sub>max</sub>	5.2	V
Thermal Resistance, Junction-to-Air	$R_{ heta JA}$	240	°C/W
Operating Ambient Temperature Range	T <sub>A</sub>	-30 to +85	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Junction Operating Temperature Range	TJ	-30 to +125	°C

**ELECTRICAL CHARACTERISTICS** ( $V_{in}$  = 3.6 V,  $V_{O}$  = 1.57 V,  $T_{A}$  = 25°C,  $F_{syn}$  = 600 kHz 50% Duty Cycle square wave for PWM mode;  $T_{A}$  = -30 to 85°C for Min/Max values, unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
V <sub>CC</sub> Pin			•		
Quiescent Current of Switching Mode, I <sub>out</sub> = 0 mA	Iq PWM	-	140	-	μΑ
Quiescent Current of LDO Mode, I <sub>out</sub> = 0 mA	lq LDO	-	32	-	μΑ
Quiescent Current, SHD Low	Iq Off	-	0.2	1.0	μΑ
Input Voltage Range	V <sub>in</sub>	2.7	-	5.2	V
Sync Pin					
Input Voltage	V <sub>sync</sub>	-0.3	-	V <sub>CC</sub> +0.3	V
Frequency Operational Range	F <sub>sync</sub>	500	-	1000	kHz
Minimum Synchronization Pulse Width	Dc <sub>sync(min)</sub>	-	30	-	%
Maximum Synchronization Pulse Width	Dc <sub>sync(max)</sub>	-	70	-	%
SYNC "H" Voltage Threshold	V <sub>sync(H)</sub>	-	920	1200	mV
SYNC "L" Voltage Threshold	V <sub>sync(L)</sub>	400	830	-	mV
SYNC "H" Input Current, V <sub>sync</sub> = 3.6 V	I <sub>sync(H)</sub>	-	1.8	-	μΑ
SYNC "L" Input Current, V <sub>sync</sub> = 0 V	I <sub>sync(L)</sub>	-0.5	0.005	-	μΑ
Output Level Selection Pins					
Input Voltage	$V_{CB}$	-0.3	-	V <sub>CC</sub> +0.3	V
CB0,1 "H" Voltage Threshold	V <sub>CB(H)</sub>	-	910	1200	mV
CB0,1 "L" Voltage Threshold	V <sub>CB(L)</sub>	400	850	-	mV
CB0,1 "H" Input Current, CBx = 3.6 V	I <sub>CB(H)</sub>	-	1.8	-	μΑ
CB0,1 "L" Input Current, CBx = 0 V	I <sub>CB(L)</sub>	-0.5	0	-	μА

**ELECTRICAL CHARACTERISTICS (continued)** ( $V_{in} = 3.6 \text{ V}$ ,  $V_O = 1.57 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ ,  $F_{syn} = 600 \text{ kHz}$  50% Duty Cycle square wave for PWM mode;  $T_A = -30$  to 85°C for Min/Max values, unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
Shutdown Pin	·				
Input Voltage	V <sub>SHD</sub>	-0.3	=	V <sub>CC</sub> +0.3	V
SHD "H" Voltage Threshold	V <sub>SHD(H)</sub>	-	920	1200	mV
SHD "L" Voltage Threshold	V <sub>SHD(L)</sub>	400	850	-	mV
SHD "H" Input Current, SHD = 3.6 V	I <sub>SHD(H)</sub>	-	1.8	-	μΑ
SHD "L" Input Current, SHD = 0 V	I <sub>SHD(L)</sub>	-0.5	0	-	μΑ
Feedback Pin					
Input Voltage	$V_{fb}$	-0.3	-	V <sub>CC</sub> +0.3	V
Input Current, V <sub>fb</sub> = 1.8 V	I <sub>fb</sub>	-	8.5	-	μΑ
PWM Mode Characteristics					
Switching P-FET Current Limit	I <sub>lim</sub>	-	800	-	mA
Duty Cycle	DC	-	-	100	%
Minimum On Time	T <sub>on(min)</sub>	-	100	-	nsec
R <sub>DS(on)</sub> Switching N-FET P-FET	R <sub>DS(on)</sub>		0.7 0.6		Ohms
Switching P-FET and N-FET Leakage Current	I <sub>leak</sub>	-	0.01	10	μΑ
Output Over Voltage Threshold	Vo	-	5.0	-	%
NCP1501 Output Voltage Accuracy, I <sub>out</sub> = 10 to 120 mA, V <sub>out(set)</sub> = 1.05 V 1.35 V 1.57 V 1.8 V	V <sub>out</sub>	1.018 1.309 1.523 1.740	1.050 1.350 1.570 1.800	1.082 1.391 1.617 1.860	V
NCP1502 Output Voltage Accuracy, I <sub>out</sub> = 10 to 120 mA, V <sub>out(set)</sub> = 1.0 V 1.3 V 1.5 V 1.9 V	V <sub>out</sub>	0.970 1.260 1.450 1.843	1.000 1.300 1.500 1.900	1.030 1.340 1.550 1.957	V
Load Transient Response, 10 to 100 mA Load Step	V <sub>out</sub>	-	-	50	mV
Line Transient Response, I <sub>out</sub> = 100 mA, 3.0 to 3.6 V <sub>in</sub> Line Step	V <sub>out</sub>	-	±5	-	$mV_{pp}$
LDO Mode Characteristics	·				
R <sub>DS(on)</sub> LDO FET (Inductor Switch), LX to V <sub>out</sub>	R <sub>DS(on)</sub>	-	7.0	-	Ohms
Dropout Voltage (Limited by V <sub>in(min)</sub> = 2.5 V and V <sub>out(max)</sub> = 1.8 V)	V <sub>in</sub> - V <sub>out</sub>	-	0.7	-	V
NCP1501 Output Voltage Accuracy, I <sub>out</sub> = 0.01 to 50 mA, V <sub>out(set)</sub> = 1.05 V 1.35 V 1.57 V 1.8 V	V <sub>out</sub>	1.018 1.309 1.523 1.740	1.050 1.350 1.570 1.800	1.082 1.391 1.617 1.860	V
NCP1502 Output Voltage Accuracy, I <sub>out</sub> = 0.01 to 50 mA, V <sub>out(set)</sub> = 1.0 V 1.3 V 1.5 V 1.9 V	V <sub>out</sub>	0.970 1.260 1.450 1.843	1.000 1.300 1.500 1.900	1.030 1.340 1.550 1.957	V



Component	Value	Manufacturer
C1, C2	10 μF, 6.3 V	TDK, C2012X5R0J106M
L	10 μΗ	TDK, LLF4017-100 (I <sub>out</sub> = 300 mA) Coilcraft, LPO4812-103MX (I <sub>out</sub> = 300 mA) Coilcraft, 0805PS-103M (I <sub>out</sub> = 150 mA) TDK, NLC252018T-100 (I <sub>out</sub> = 100 mA)

Figure 2. Typical Circuit with the Internal Schematic

#### **DETAILED OPERATING DESCRIPTION**

The Buck regulator is a synchronous rectifier PWM regulator with integrated MOSFETs. This regulator has an LDO function for low power modes to conserve power and lower ripple voltage associated with PFM mode. The NCP150x does not contain an internal oscillator for the switching mode. The Dual PWM/LDO mode is an exclusive Patent Pending circuit.

The PWM clock is generated via an external clock signal on the Synchronization pin. The operating frequency range for the PWM is 450 to 1000 kHz. The output current of the PWM is typically 100 mA with a guarantee of over 300 mA for the 2.5 to 5.2 input voltage range.

If a synchronization pulse is not present, the NCP150x changes into the LDO mode. The LDO function assures the user of an extremely low output ripple voltage and greatly reduced quiescent current when the users system is in a sleep mode. Internally to the NCP150x, the Synchronization pin

has a pull down resistor to force the part into LDO mode when a clock signal is not present. To place the NCP150x in LDO mode, the user must set the Synchronization pin low. The LDO mode guarantees an output in excess of 50 mA.

Pins CB0 and CB1 control the output voltage selection. The four voltages are 1.05, 1.35, 1.57, 1.8 or 1.0, 1.3, 1.5, 1.9 volts. CB0 and CB1 contain pull down resistors internally to the NCP150x. The pull down resistors force the output of the converter to a fixed voltage if the pins are floating connections to the external circuit.

The Shutdown Pin enables the operation of the device. The Shutdown Pin has an internal pull down resistor to force the NCP150x into the off mode if this pin is floating due to the external circuit. During Startup, the NCP150x has a soft start function to limit fast dV/dt and eliminate overshoot on the output.

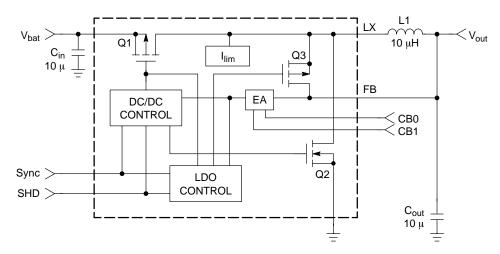


Figure 3. Block Diagram and Circuit Schematic of the NCP150x

The external components required are an input and an output 10  $\mu$ F ceramic capacitor and a 10  $\mu$ H inductor.

### **PWM Mode**

During normal operation, a synchronization pulse acts as the clock for the DC/DC controller. The rising edge of the clock pulls the gate of Q1 low allowing the inductor to charge. When the current through Q1 reaches either the current limit or feedback voltage reaches its limit, Q1 will turn off and Q2 will turn on. Q2 replaces the free wheeling diode typically associated with Buck Converters. Q2 will turn off when either a rising edge sync pulse is present or all the stored energy is depleted from the inductor. Q3 remains off during this mode.

The output voltage accuracy in the PWM mode is well within 3% of the nominal set value. An over voltage

protection circuit is present in the PWM mode to limit the positive voltage spike due to fast load transient conditions. The PWM also has the ability to go to 100% duty cycle for transient conditions and low input to output voltage differentials.

In PWM mode, each switching cycle has a guaranteed on-time of 100 ns. The NCP150x has two protection circuits that can eliminate the cycle. When tripped, the over voltage protection or the thermal shutdown overrides the gate drive of the high side MOSFET.

NCP150x contains a damping circuit for the inductor. The damping circuit is active during discontinuous switching mode. This circuit eliminates the oscillations in the inductor when it is depleted of its energy.

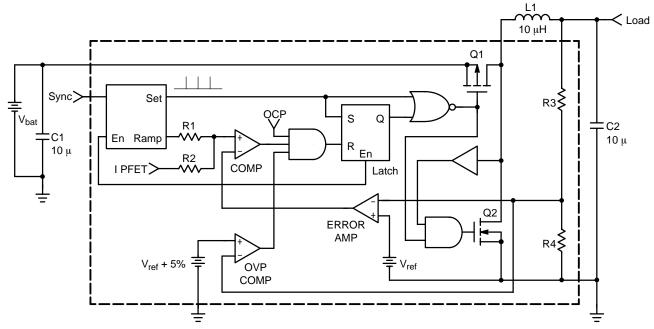


Figure 4. PWM Circuit Schematic

### **LDO Mode**

When the synchronization pulse is not present, the NCP150x operates as an LDO. The DC/DC Control Circuitry will relinquish control of Q1 and turn off Q2. The

LDO Control Circuitry will turn on Q3 as a bypass circuit to the inductor. Q1 is the controlling pass device of the LDO that regulates the input to output voltage dropout. The LDO can source an output current in excess of 50 mA.

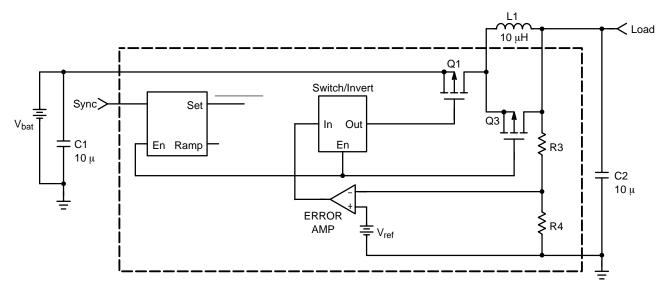


Figure 5. LDO Circuit Schematic

### **Voltage Output Selection**

The output voltage selection is accomplished via two external pins: CB0 and CB1. If CB0 and CB1 pins are left floating by the external circuit, the output voltage will default to 1.35/1.3 V. The corresponding voltages are as follows

		NCP1501	NCP1502
CB0	CB1	V <sub>out</sub> (V)	V <sub>out</sub> (V)
0	0	1.05	1.0
0	1	1.35	1.3
1	0	1.80	1.9
1	1	1.57	1.5

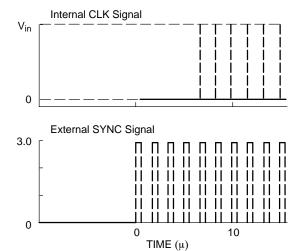


Figure 6. Transition Waveforms from LDO to PWM Mode

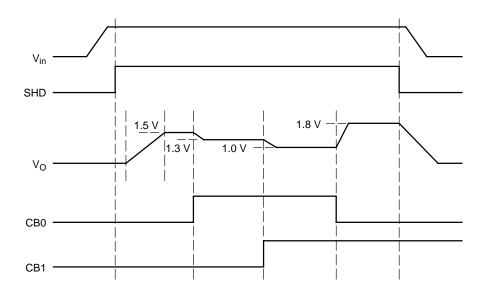


Figure 7. Power Up and Power Down Sequence

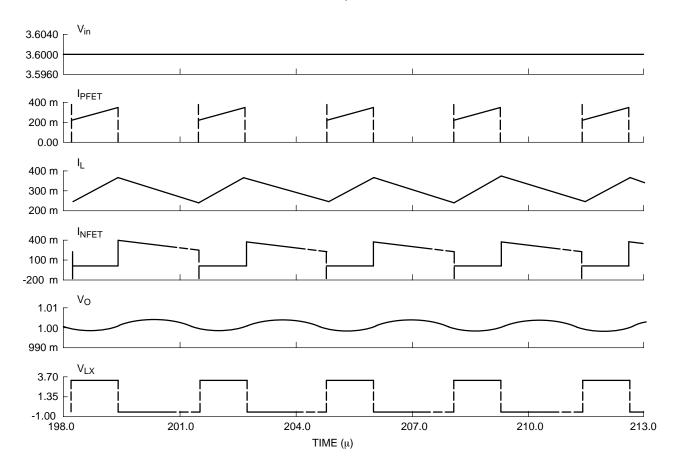


Figure 8. Waveforms During Normal Operation

#### **APPLICATIONS INFORMATION**

NCP150x is a dual mode PWM or LDO step down converter. This dual mode takes advantage of the best of each mode. There are three required external components: an input and output capacitor and an inductor.

The PWM mode allows high efficiency for larger loads. A typical efficiency for an input of 3.6 volts and an output of 1.8 volts and 100 mA is over 90%. Low R<sub>DSon</sub> and synchronous rectification contained within the device contributes to the very high efficiency. As with other synchronous rectification devices, the NCP150x does not require an external diode to supplement the NFET during switching on or off. A synchronization pin allows the user to define the frequency noise spikes of the PWM. The duty cycle of the synchronization signal must be within the range

of 30% to 70%. The rising edge of the signal from the synchronization pin acts as the oscillator signal to set the latch and reset the ramp compensation signal. An Over Voltage Protection circuit ensures the output will respond properly to fast transients from large to small loads. The NCP150x allows the PWM mode to enter a 100% duty cycle for fast load transient conditions and low input to output voltage differentials.

The LDO mode is effective during low load conditions by lowering the quiescent current and reducing the output ripple voltage associated with PWM converters entering PFM mode. NCP150x enters the LDO mode when a synchronization signal is not present. It is recommended to pull the synchronization signal low for LDO mode.

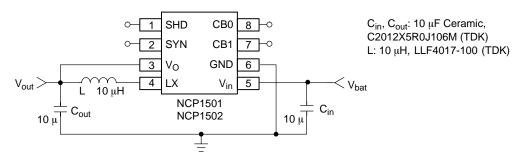


Figure 9. Typical Operating Schematic

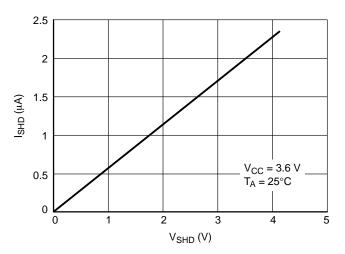


Figure 10. Input Current versus Voltage for the Shutdown Pin

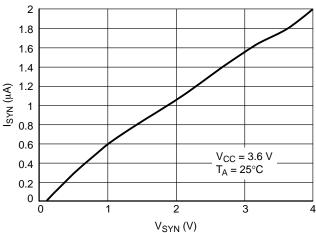


Figure 11. Input Current versus Voltage for the Synchronization Pin

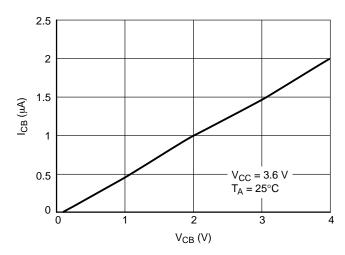


Figure 12. Input Current versus Voltage for the CB Pins

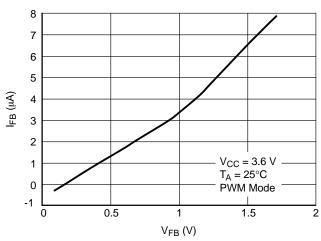


Figure 13. Input Current versus Voltage for the Feedback Pin

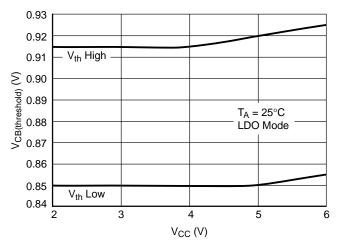


Figure 14. V<sub>CC</sub> Input Voltage versus CB Threshold

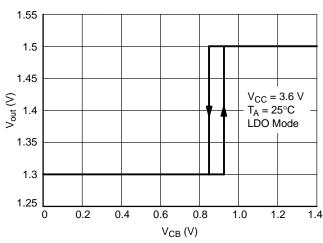


Figure 15. Transition Level of CB Pins

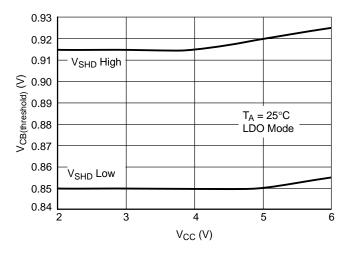


Figure 16. Input Voltage versus Shutdown Voltage

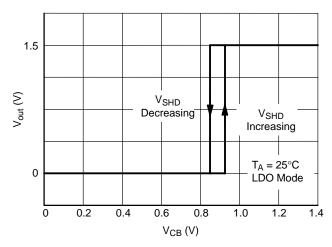


Figure 17. Output Voltage versus Shutdown Pin Voltage

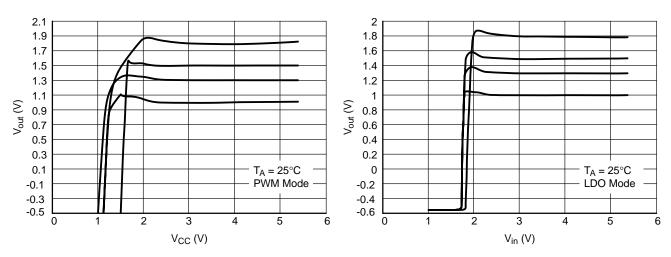


Figure 18. Output Voltage versus Input V<sub>CC</sub> in PWM Mode

Figure 19. Output Voltage versus Input  $V_{CC}$  in LDO Mode

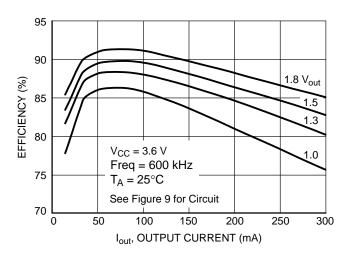
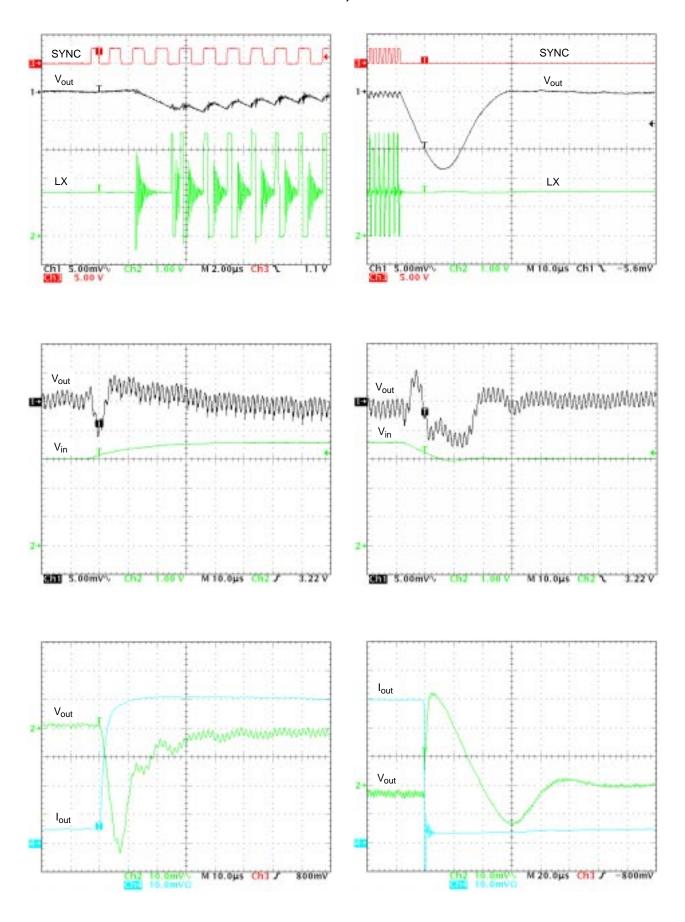
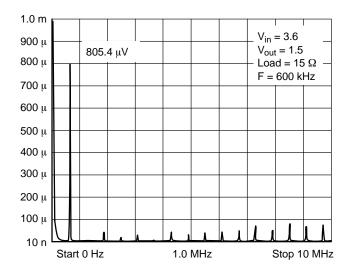


Figure 20. Efficiency versus Output Current



200 μ



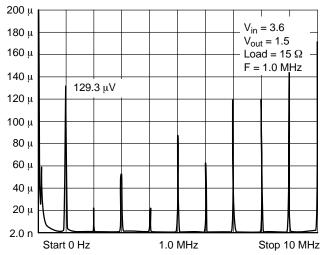
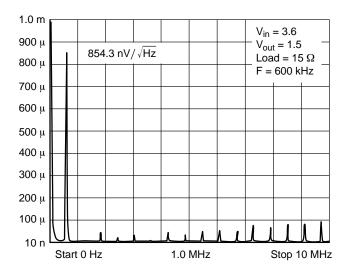


Figure 21. V<sub>rms</sub> versus Frequency

Figure 22. V<sub>rms</sub> versus Frequency



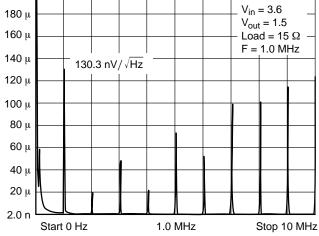
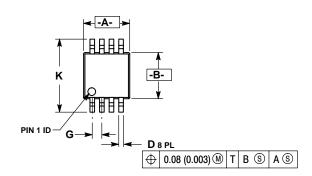


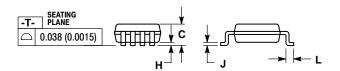
Figure 23. Noise versus Frequency

Figure 24. V<sub>RMS</sub> versus Frequency

#### PACKAGE DIMENSIONS

Micro8 (MSOP-8) **DM SUFFIX** CASE 846A-02 ISSUE F





#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

  4. DIMENSION B DOES NOT INCLUDE INTERLEAD
- FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010)
- 5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.114	0.122
В	2.90	3.10	0.114	0.122
С		1.10		0.043
D	0.25	0.40	0.010	0.016
G	0.65	0.65 BSC		BSC
Н	0.05	0.15	0.002	0.006
L	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

Micro8 is a trademark of International Rectifier.

ON Semiconductor and war registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

#### **PUBLICATION ORDERING INFORMATION**

### Literature Fulfillment:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA

Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada

Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center 2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051

Phone: 81-3-5773-3850

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local

Sales Representative.