Features

128Kx32 bit Flash

- Fast Access Times: 60, 70, 90, 120 and 150ns
- Individual Byte Selects (x8, x16, x32)
- 100,000 Erase/Program Cycles minimum
- Output Enable Function
- TTL Compatible Inputs and Outputs
- 5V Programming

Sector Architecture

- 8 Equal Size Sectors of 16K bytes
- Sectors can be Concurrently Erased in any Combination
- Supports Full Chip Erase

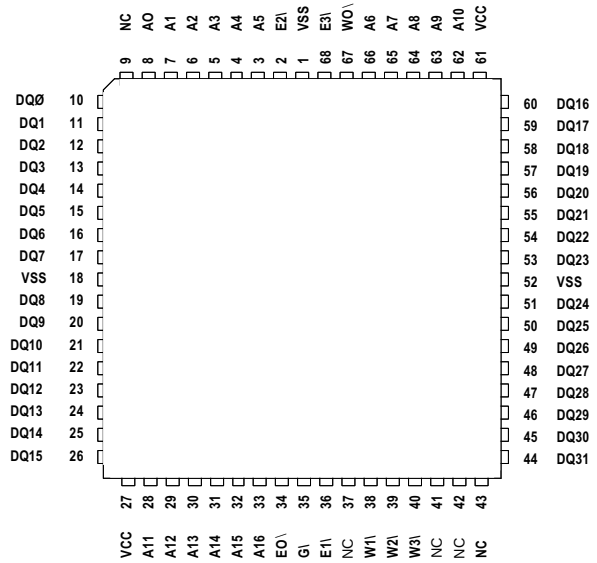
High Density MCM-C Packaging <0.99 in.sq.

- 68 lead CQFP, No. 405
- Multiple Ground Pins for Maximum Noise Immunity

Single +5V (±10%) Supply Operation

DSCC Drawing 5962-94716

Pin Configuration and Block Diagram



128Kx32 High Speed Flash Module

The EDI7C32128C is a high speed, high performance, four megabit density Flash module, organized as 512Kx32 bits, containing four 128Kx8 die mounted in a package.

Four Chip Enables are provided to independently enable each of the four bytes. Reading or writing can be executed on an individual byte or any combination of bytes through proper use of the chip and write enables.

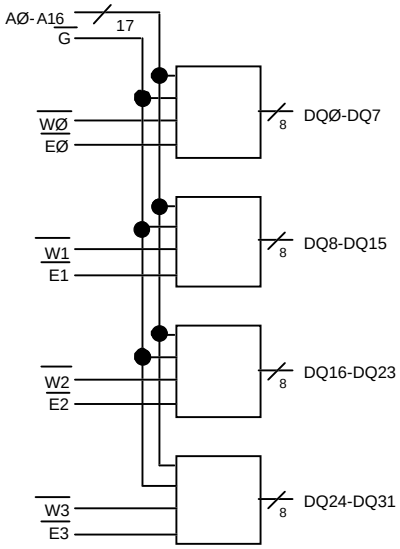
Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

The EDI7C32128C is offered in a 68 lead CQFP package which enables 4 megabits of memory to be placed in less than 0.99 square inches of space, respectively.

The device may be screened in accordance with MIL-PRF-38535. This device is based on the AMD AM29F010 part.

Pin Names

AØ-A16	Address Inputs
$\overline{EØ}$-$\overline{E3}$	Chip Enables
$\overline{WØ}$-$\overline{W3}$	Write Enables
$\overline{G}$	Output Enable
DQØ-DQ31	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS(1)	-2.0V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to + 70°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Power Dissipation	1.1 Watts Max@5MHz
A9 Voltage for Sector Protect(2)	-2.0V to +14.0V

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1. Minimum DC voltage on input or I/O pins is -0.5V during voltage transitions, inputs or I/O pins may undershoot Vss to -2.0V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is Vcc+0.5V during voltage transitions, outputs may overshoot to Vcc+2.0V for periods up to 20ns.
2. Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot Vss to -2V for periods up to 20ns. Maximum DC input voltage on A9 is +13.5V which may overshoot to +14.0 for periods up to 20ns.

Recommended DC Operating Conditions

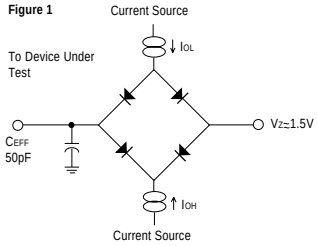
Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.0	--	VCC+0.5	V
Input Low Voltage	VIL	-0.5	--	0.8	V
A9 Voltage for Sector Protect		+11.5	--	+12.5	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

1. Vz is programmable from +2V to +7V.
2. I_{OL} and I_{OH} are programmable from 0 to 16mA.
3. Tester impedance is Zo=75ohms.
4. Vz is typically the midpoint of V_{OL} and V_{OH}.
5. I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

Figure 1



DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Typ	Max	Units
Operating Power Supply Current – x32	ICC1	$\overline{G}$= VIL, f=5MHz E = VIL	60-150ns			140	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$=VIL, $\overline{G}$=VIH f=5MHz, VCC=5.5V	60-150ns			200	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$=VIH f=5MHz, VCC=5.5V	60-150ns			6.5 mA	mA
Input Leakage Current	ILI	VIN = 0V to VCC		--	--	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		--	--	±10	µA
Output High Volltage	VOH	IOH = -2.5mA, VCC=4.5V		0.85xVCC			V
Output Low Voltage	VOL	IOL =12.0mA, VCC=4.5V				0.45	V

Truth Table

G	E	W	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
H	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	50	pF
Data Lines	CD/Q	20	pF
Chip & Write Enable Lines	E, W	20	pF
Output Enable Line	G	50	pF

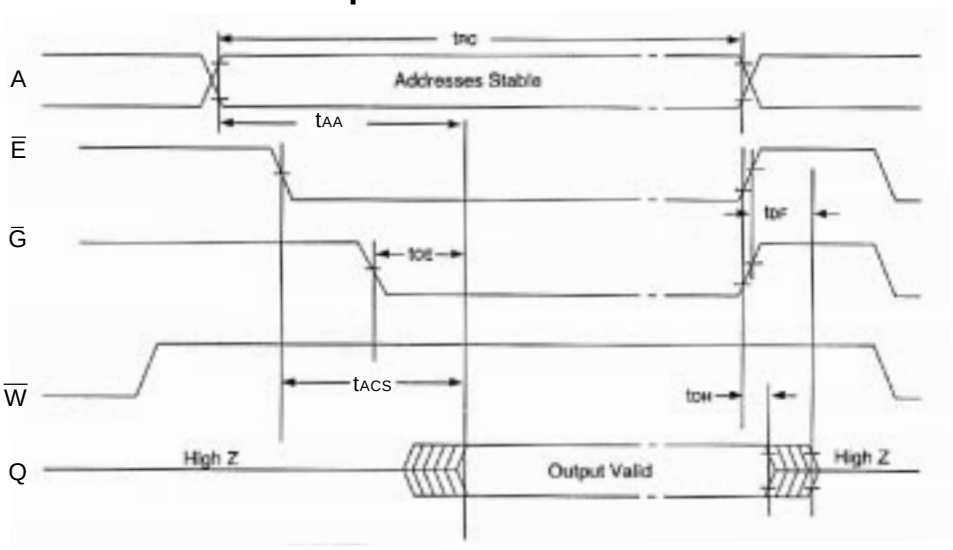
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

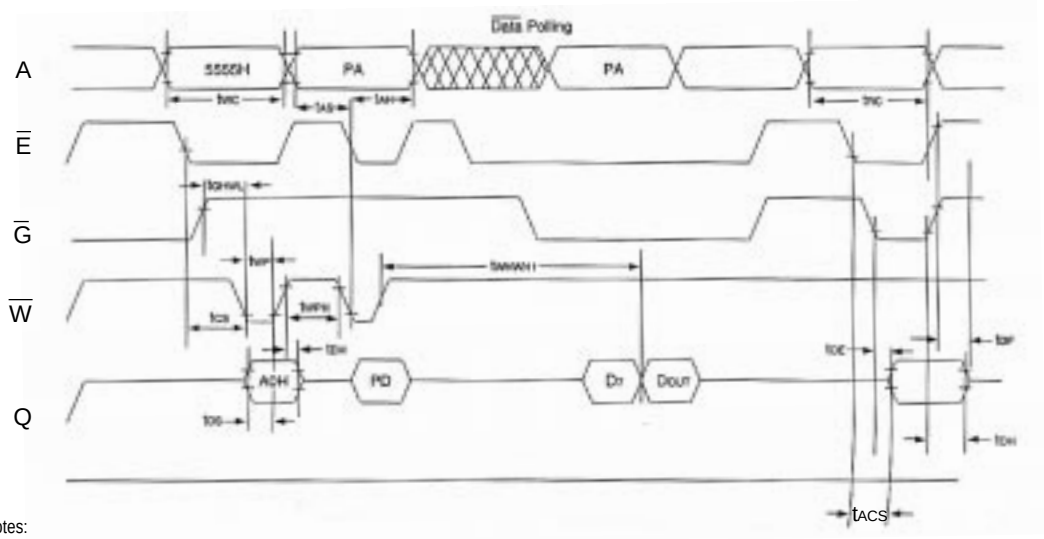
Parameter	Symbol JEDEC	Alt.	60 Min Max	70ns MinMax	90ns Min Max	120ns Min Max	150ns Min Max	Units
Read Cycle Time	TAVAV	TRC	60	70	90	120	150	ns
Address Access Time	TAVQV	TAA	60	70	90	120	150	ns
Chip Enable Access Time	TELQV	TACS	60	70	90	120	150	ns
Chip Enable to Output in High Z(1)	TEHQZ	TDF	20	20	20	30	35	ns
Output Hold from Address Change	TAVQX	TOH	0	0	0	0	0	ns
Output Enable to Output Valid	TGLQV	TOE	30	35	35	50	55	ns
Output Enable to Output High Z(1)	TGHQZ	TDF	20	20	20	30	35	ns

Note 1. Parameter guaranteed, but not tested.

AC Waveforms for Read Operations



Write/Erase/Program Operation, W Controlled

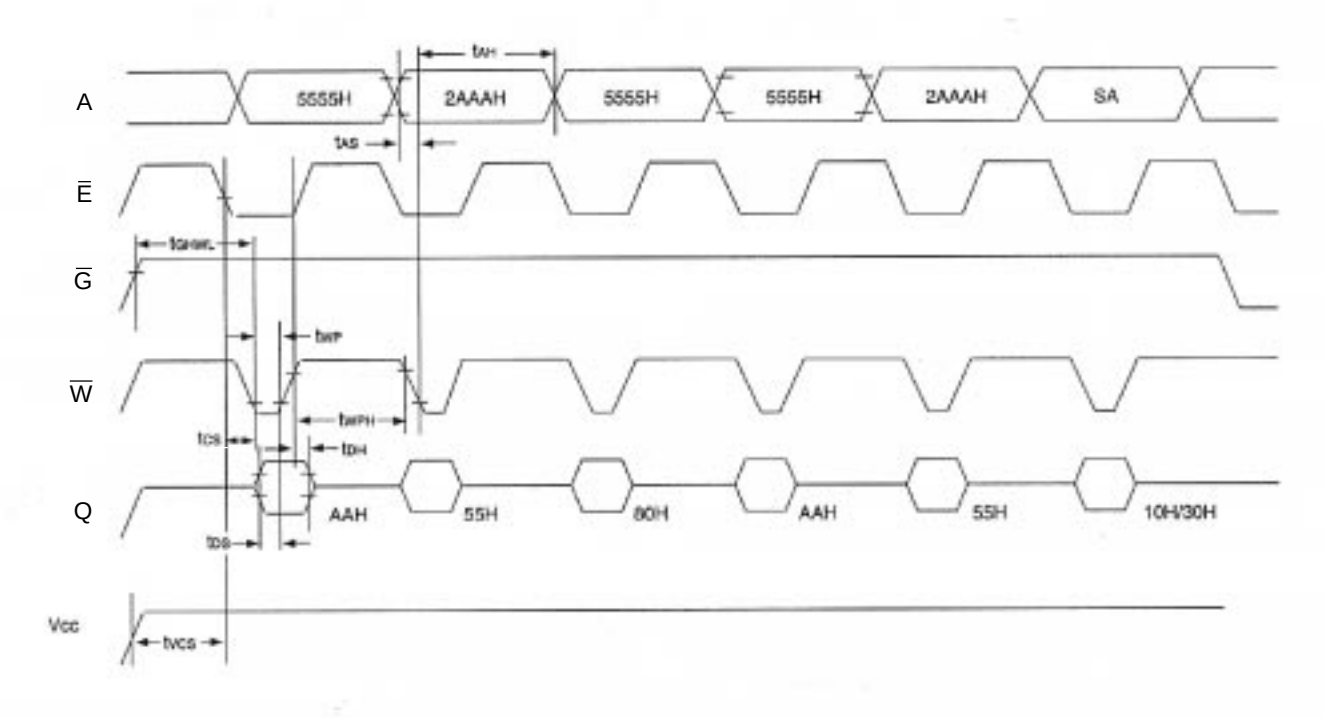


Notes:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device (for each chip).
4. Dout is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

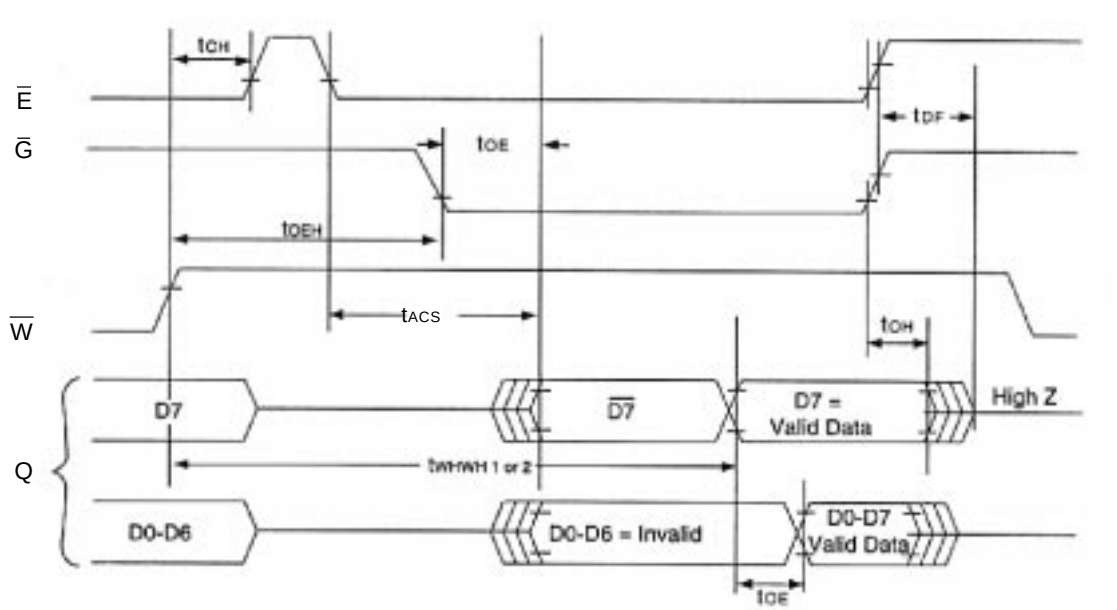
AC Characteristics Write Cycle

	Symbol		60ns		70ns		90ns		120ns		150ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Cycle Time	TAVAV	TWC	60		70		90		120		150		ns
Chip Enable Setup Time	TELWH	TCS	0		0		0		0		0		ns
Chip Enable Pulse Width	TELEH	TCP	30		45		45		50		50		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		0		ns
Write Enable Setup Time	TWLEL	TWS	0		0		0		0		0		ns
Address Hold Time	TWHAX	TAH	45		45		45		50		50		ns
Write Pulse Width	TWLWH	TWP	30		45		45		50		50		ns
Data Setup Time	TDVWH	TDS	30		45		45		50		50		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		0		ns
Write Enable Pulse Width High	TWHWL	TWPH	20		20		20		20		20		ns
Output Enable Setup Time		TOES	0		0		0		0		0		ns
Output Enable Hold Time		TOEH	10		10		10		10		10		ns
Sector Erase Time	TWHWH[2]		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	s
Programming Time				12.5		12.5		12.5		12.5		12.5	s
Read Recovery Time Before Rewrite	TGHWL		0		0		0		0		0		ns
Vcc Setup Time		TVCS	50		50		50		50		50		µs
Duration of Byte Programming Operation	TWHWH[1]		14		14		14		14		14		µs

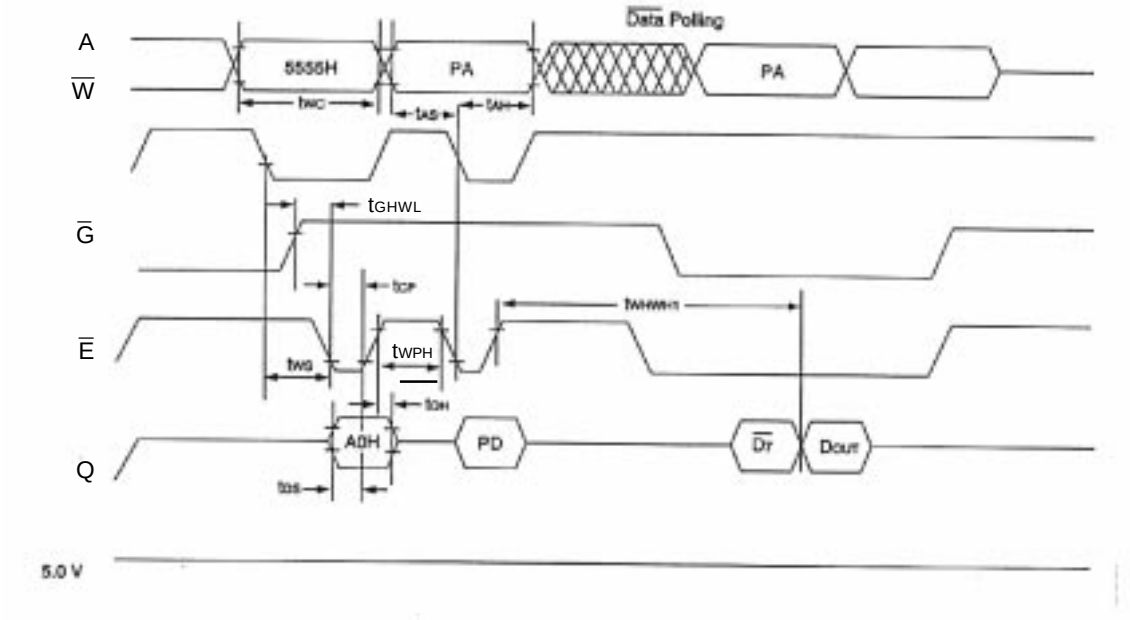
AC Waveforms Chip/Selector Erase Operations



AC Waveforms for Data Polling during Embedded Algorithm Operations



Alternate Ē Controlled Programming Operation Timing



Notes:
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7 is the output of the complement of the data written to the device (for each chip).
4. Dout is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

Ordering Information

Military, Standard Power

Part No.	Speed (ns)	Package No.
EDI7C32128C60EQ	60	405
EDI7C32128C70EQ	70	405
EDI7C32128C90EQ	90	405
EDI7C32128C120EQ	120	405
EDI7C32128C150EQ	150	405

For Commercial, Industrial or MTO grade product, C,I or M replaces Q in part number, e.g. EDI7C32512C70EQ becomes EDI7C32512C70EI (Industrial temp range).

Package Description

68 lead CQFP