

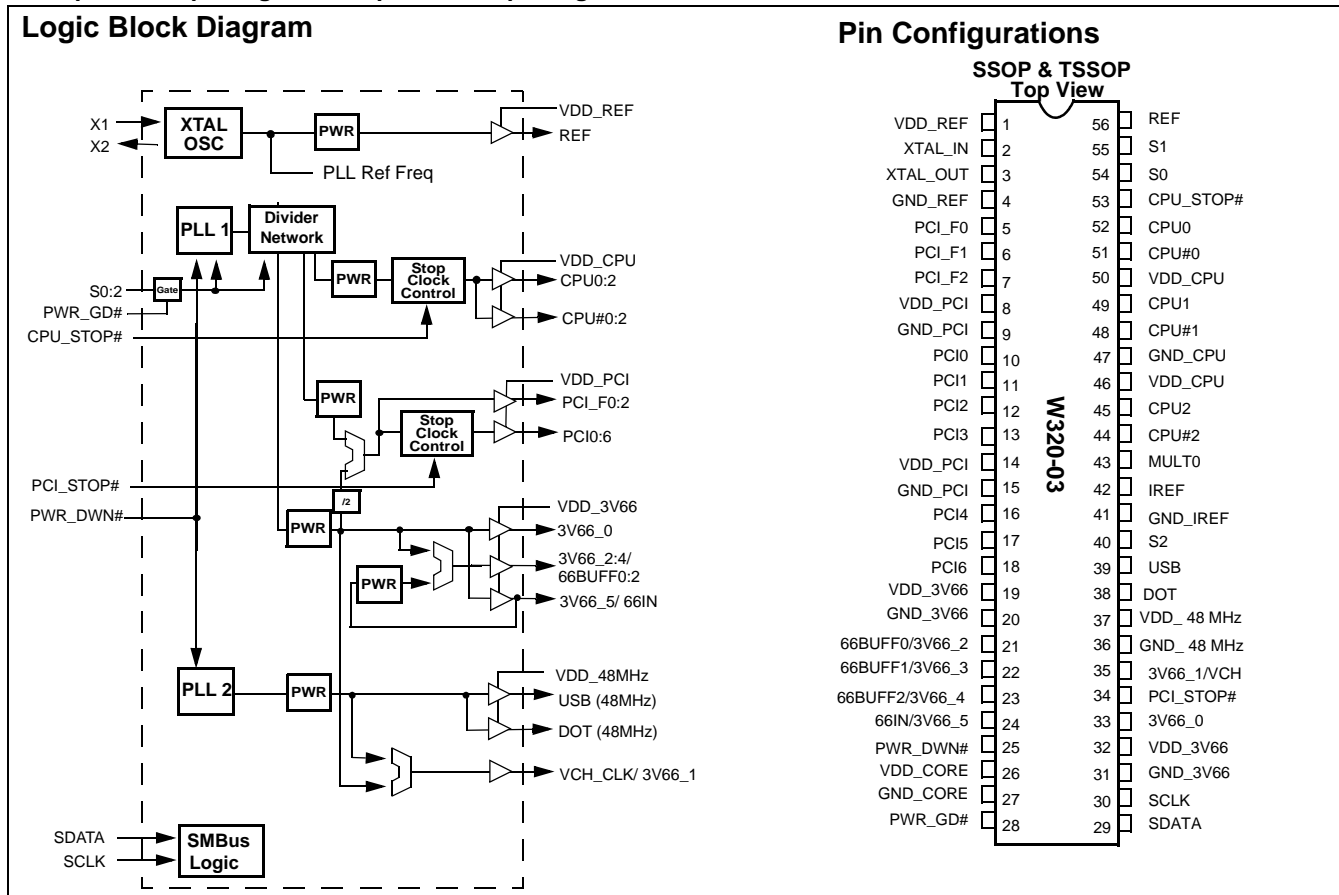
200 MHz Spread Spectrum Clock Synthesizer/Driver with Differential CPU Outputs

Features

- Compliant with Intel® CK-Titan Clock Synthesizer/Driver Specifications
- Multiple output clocks at different frequencies
- Three pairs of differential CPU outputs, up to 200 MHz
- Ten synchronous PCI clocks, three free-running
- Six 3V66 clocks
- Two 48 MHz clocks
- One reference clock at 14.318 MHz
- One VCH clock
- Spread Spectrum clocking (down spread)
- Power-down features (PCI_STOP#, CPU_STOP#, PWR_DWN#)
- Three Select inputs (Mode select & IC Frequency Select)
- OE and Test Mode support
- 56-pin SSOP package and 56-pin TSSOP package

Benefits

- Supports next-generation Pentium® processors using differential clock drivers
- Motherboard clock generator
- Support Multiple CPUs and a chipset
- Support for PCI slots and chipset
- Supports AGP, DRCG reference and Hub Link
- Supports USB host controller and graphic controller
- Supports ISA slots and I/O chip
- Enables reduction of electromagnetic interference (EMI) and overall system cost
- Enables ACPI-compliant designs
- Supports up to four CPU clock frequencies
- Enables ATE and “bed of nails” testing
- Widely available, standard package enables lower cost



Pin Summary

| Name | Pins | Description |
|---|------------------------------|---|
| REF | 56 | 3.3V 14.318 MHz clock output |
| XTAL_IN | 2 | 14.318 MHz crystal input |
| XTAL_OUT | 3 | 14.318 MHz crystal input |
| CPU, CPU# [0:2] | 44, 45, 48, 49, 51, 52 | Differential CPU clock outputs |
| 3V66_0 | 33 | 3.3V 66 MHz clock output |
| 3V66_1/VCH | 35 | 3.3V selectable through SMBus to be 66 MHz or 48 MHz |
| 66IN/3V66_5 | 24 | 66 MHz input to buffered 66BUFF and PCI or 66 MHz clock from internal VCO |
| 66BUFF [2:0] /3V66 [4:2] | 21, 22, 23 | 66 MHz buffered outputs from 66Input or 66 MHz clocks from internal VCO |
| PCI_F [0:2] | 5, 6, 7, | 33 MHz clocks divided down from 66Input or divided down from 3V66 |
| PCI [0:6] | 10, 11, 12, 13, 16, 17, 18 | PCI clock outputs divided down from 66Input or divided down from 3V66 |
| USB | 39 | Fixed 48 MHz clock output |
| DOT | 38 | Fixed 48 MHz clock output |
| S2 | 40 | Special 3.3V 3 level input for Mode selection |
| S1, S0 | 54, 55 | 3.3V LVTTTL inputs for CPU frequency selection |
| IREF | 42 | A precision resistor is attached to this pin which is connected to the internal current reference |
| MULT0 | 43 | 3.3V LVTTTL input for selecting the current multiplier for the CPU outputs |
| PWR_DWN# | 25 | 3.3V LVTTTL input for Power_Down# (active LOW) |
| PCI_STOP# | 34 | 3.3V LVTTTL input for PCI_STOP# (active LOW) |
| CPU_STOP# | 53 | 3.3V LVTTTL input for CPU_STOP# (active LOW) |
| PWRGD# | 28 | 3.3V LVTTTL input is a level sensitive strobe used to determine when S[2:0] and MULTIO inputs are valid and OK to be sampled (Active LOW). Once PWRGD# is sampled LOW, the status of this output will be ignored. |
| SDATA | 29 | SMBus compatible SDATA |
| SCLK | 30 | SMBus compatible Sclk |
| VDD_REF, VDD_PCI, VDD_3V66, VDD_CPU | 1, 8, 14, 19, 32, 46, 50 | 3.3V power supply for outputs |
| VDD_48 MHz | 37 | 3.3V power supply for 48 MHz |
| VDD_CORE | 26 | 3.3V power supply for PLL |
| GND_REF, GND_PCI, GND_3V66, GND_IREF, VDD_CPU | 4, 9, 15, 20, 31, 36, 41, 47 | Ground for outputs |
| GND_CORE | 27 | Ground for PLL |

Function Table [1]

| S2 | S1 | S0 | CPU (MHz) | 3V66[0:1] (MHz) | 66BUFF[0:2]/3V66[2:4] (MHz) | 66IN/3V66_5 (MHz) | PCI_F/PCI (MHz) | REF0(MHz) | USB/DOT (MHz) | Notes |
|-----|----|----|-----------|-----------------|-----------------------------|-------------------|-----------------|------------|---------------|---------|
| 1 | 0 | 0 | 66 MHz | 66 MHz | 66 IN | 66 MHz Input | 66 IN/2 | 14.318 MHz | 48 MHz | 2, 3, 4 |
| 1 | 0 | 1 | 100 MHz | 66 MHz | 66 IN | 66 MHz Input | 66 IN/2 | 14.318 MHz | 48 MHz | 2, 3, 4 |
| 1 | 1 | 0 | 200 MHz | 66 MHz | 66 IN | 66 MHz Input | 66 IN/2 | 14.318 MHz | 48 MHz | 2, 3, 4 |
| 1 | 1 | 1 | 133 MHz | 66 MHz | 66 IN | 66 MHz Input | 66 IN/2 | 14.318 MHz | 48 MHz | 2, 3, 4 |
| 0 | 0 | 0 | 66 MHz | 66 MHz | 66 MHz | 66 MHz | 33 MHz | 14.318 MHz | 48 MHz | 2, 3, 4 |
| 0 | 0 | 1 | 100 MHz | 66 MHz | 66 MHz | 66 MHz | 33 MHz | 14.318 MHz | 48 MHz | 2, 3, 4 |
| 0 | 1 | 0 | 200 MHz | 66 MHz | 66 MHz | 66 MHz | 33 MHz | 14.318 MHz | 48 MHz | 2, 3, 4 |
| 0 | 1 | 1 | 133 MHz | 66 MHz | 66 MHz | 66 MHz | 33 MHz | 14.318 MHz | 48 MHz | 2, 3, 4 |
| Mid | 0 | 0 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | 1, 5 |
| Mid | 0 | 1 | TCLK/2 | TCLK/4 | TCLK/4 | TCLK/4 | TCLK/8 | TCLK | TCLK/2 | 6, 7, 8 |
| Mid | 1 | 0 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | - |
| Mid | 1 | 1 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | - |

Swing Select Functions

| Mult0 | Board Target Trace/Term Z | Reference R, IREF = V _{DD} /(3*Rr) | Output Current | V _{OH} @ Z |
|-------|---------------------------|---|--------------------------|---------------------|
| 0 | 60Ω | Rr = 221 1%, IREF = 5.00 mA | I _{OH} = 4*IREF | 1.0V @ 50 |
| 1 | 50Ω | Rr = 475 1%, IREF = 2.32 mA | I _{OH} = 6*IREF | 0.7V @ 50 |

Clock Driver Impedances

| Buffer Name | V _{DD} Range | Buffer Type | Impedance | | |
|-------------------|-----------------------|-------------|-----------|-----------|-----------|
| | | | Minimum Ω | Typical Ω | Maximum Ω |
| CPU, CPU# | | Type X1 | | 50 | |
| REF | 3.135–3.465 | Type 3 | 20 | 40 | 60 |
| PCI, 3V66, 66BUFF | 3.135–3.465 | Type 5 | 12 | 30 | 55 |
| USB | 3.135–3.465 | Type 3A | 12 | 30 | 55 |
| DOT | 3.135–3.465 | Type 3B | 12 | 30 | 55 |

Clock Enable Configuration

| PWR_DWN# | CPU_STOP# | PCI_STOP# | CPU | CPU# | 3V66 | 66BUFF | PCI_F | PCI | USB/DOT | VCOS/OSC |
|----------|-----------|-----------|--------|-------|------|--------|-------|-----|---------|----------|
| 0 | X | X | IREF*2 | FLOAT | LOW | LOW | LOW | LOW | LOW | OFF |
| 1 | 0 | 0 | IREF*2 | FLOAT | ON | ON | ON | OFF | ON | ON |
| 1 | 0 | 1 | IREF*2 | FLOAT | ON | ON | ON | ON | ON | ON |
| 1 | 1 | 0 | ON | ON | ON | ON | ON | OFF | ON | ON |
| 1 | 1 | 1 | ON | ON | ON | ON | ON | ON | ON | ON |

Notes:

1. TCLK is a test clock driven in on the XTALIN input in test mode.
2. "Normal" mode of operation.
3. Range of reference frequency allowed is min. = 14.316 nominal = 14.31818 MHz, max = 14.32 MHz.
4. Frequency accuracy of 48 MHz must be +167PPM to match USB default.
5. Mid is defined a Voltage level between 1.0V and 1.8V for 3 level input functionality. Low is below 0.8V. High is above 2.0V.
6. TCLK is a test clock over driven on the XTAL_IN input during test mode.
7. Required for DC output impedance verification.
8. These modes are to use the SAME internal dividers as the CPU = 200-MHz mode. The only change is to slow down the internal VCO to allow under clock margining.

Serial Data Interface (SMBus)

To enhance the flexibility and function of the clock synthesizer, a two signal SMBus interface is provided according to the SMBus specification. Through the Serial Data Interface (SDI), various device functions such as individual clock output buffers, etc can be individually enabled or disabled. W320-03 support both block read and block write operations.

The registers associated with the SDI initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte, (most significant bit first) with the

ability to stop after any complete byte has been transferred. Indexed bytes are not allowed.

A block write begins with a slave address and a WRITE condition. The R/W bit is used by the SMBus controller as a data direction bit. A zero indicates a WRITE condition to the clock device. The slave receiver address is 11010010 (D2h).

A command code of 0000 0000 (00h) and the byte count bytes are required for any transfer. After the command code, the core logic issues a byte count which describes number of additional bytes required for the transfer, not including the command code and byte count bytes. For example, if the host has 20 data bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count byte is required to be a minimum of one byte and a maximum of 32 bytes. It may not be 0. *Figure 1* shows an example of a block write.

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller.

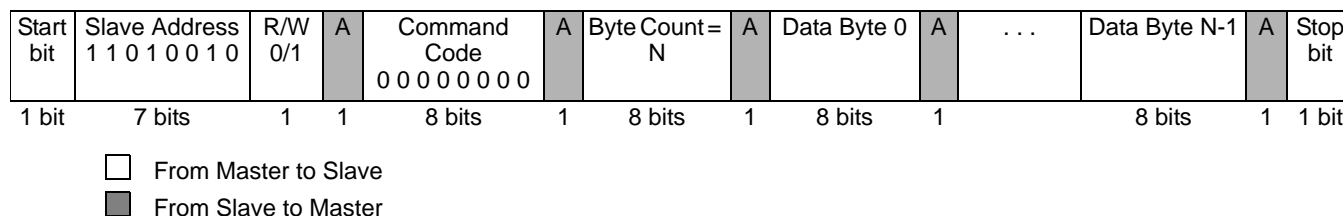


Figure 1. An Example of a Block Write

Data Byte Configuration Map

Data Byte 0: Control Register (0 = Enable, 1 = Disable)

| Bit | Affected Pin# | Name | Description | Type | Power On Default |
|-------|---|------------------------------------|--|------|------------------|
| Bit 7 | 5, 6, 7, 10, 11, 12, 13, 16, 17, 18, 33, 35 | PCI [0:6] CPU[2:0] 3V66[1:0] | Spread Spectrum Enable 0 = Spread Off, 1 = Spread On | R/W | 0 |
| Bit 6 | – | TBD | TBD | R | 0 |
| Bit 5 | 35 | 3V66_1/VCH | VCH Select 66 MHz/48 MHz 0 = 66 MHz, 1 = 48 MHz | R/W | 0 |
| Bit 4 | 44, 45, 48, 49, 51, 52 | CPU [2:0] CPU# [2:0] | CPU_STOP# Reflects the current value of the external CPU_STOP# pin | R | N/A |
| Bit 3 | 10, 11, 12, 13, 16, 17, 18 | PCI [6:0] | PCI_STOP# (Does not affect PCI_F [2:0] pins) | R/W | N/A |
| Bit 2 | – | – | S2 Reflects the value of the S2 pin sampled on Power-up | R | N/A |
| Bit 1 | – | – | S1 Reflects the value of the S1 pin sampled on Power-up | R | N/A |
| Bit 0 | – | – | S0 Reflects the value of the S1 pin sampled on Power-up | R | N/A |

Data Byte 1

| Bit | Pin# | Name | Description | Type | Power On Default |
|-------|--------|---------------|---|------|------------------|
| Bit 7 | – | N/A | CPU Mult0 Value | R | N/A |
| Bit 6 | – | N/A | TBD | R | 0 |
| Bit 5 | 44, 45 | CPU2 CPU2# | Allow Control of CPU2 with assertion of CPU_STOP# 0 = Not free running; 1 = Free running | R/W | 0 |
| Bit 4 | 48, 49 | CPU1 CPU1# | Allow Control of CPU1 with assertion of CPU_STOP# 0 = Not free running; 1 = Free running | R/W | 0 |
| Bit 3 | 51, 52 | CPU0 CPU0# | Allow Control of CPU0 with assertion of CPU_STOP# 0 = Not free running; 1 = Free running | R/W | 0 |
| Bit 2 | 44, 45 | CPU2 CPU2# | CPU2 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |
| Bit 1 | 48, 49 | CPU1 CPU1# | CPU1 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |
| Bit 0 | 51, 52 | CPU0 CPU0# | CPU0 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |

Data Byte 2

| Bit | Pin# | Name | Pin Description | Type | Power On Default |
|-------|------|------|---|------|------------------|
| Bit 7 | – | N/A | N/A | R | 0 |
| Bit 6 | 18 | PCI6 | PCI6 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |
| Bit 5 | 17 | PCI5 | PCI5 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |
| Bit 4 | 16 | PCI4 | PCI4 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |
| Bit 3 | 13 | PCI3 | PCI3 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |
| Bit 2 | 12 | PCI2 | PCI2 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |
| Bit 1 | 11 | PCI1 | PCI1 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |
| Bit 0 | 10 | PCI0 | PCI0 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |

Data Byte 3

| Bit | Pin# | Name | Pin Description | Type | Power On Default |
|-------|------|--------|---|------|------------------|
| Bit 7 | 38 | DOT | DOT 48-MHz Output Enable | R/W | 1 |
| Bit 6 | 39 | USB | USB 48-MHz Output Enable | R/W | 1 |
| Bit 5 | 7 | PCI_F2 | Allow control of PCI_F2 with assertion of PCI_STOP# 0 = Free running; 1 = Stopped with PCI_STOP# | R/W | 0 |
| Bit 4 | 6 | PCI_F1 | Allow control of PCI_F1 with assertion of PCI_STOP# 0 = Free running; 1 = Stopped with PCI_STOP# | R/W | 0 |
| Bit 3 | 5 | PCI_F0 | Allow control of PCI_F0 with assertion of PCI_STOP# 0 = Free running; 1 = Stopped with PCI_STOP# | R/W | 0 |
| Bit 2 | 7 | PCI_F2 | PCI_F2 Output Enable | R/W | 1 |
| Bit 1 | 6 | PCI_F1 | PCI_F1 Output Enable | R/W | 1 |
| Bit 0 | 5 | PCI_F0 | PCI_F0 Output Enable | R/W | 1 |

Data Byte 4

| Bit | Pin# | Name | Pin Description | Type | Power On Default |
|-------|------|-------------|---|------|------------------|
| Bit 7 | -- | TBD | N/A | R | 0 |
| Bit 6 | -- | TBD | N/A | R | 0 |
| Bit 5 | 33 | 3V66_0 | 3V66_0 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |
| Bit 4 | 35 | 3V66_1/VCH | 3V66_1/VCH Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |
| Bit 3 | 24 | 66IN/3V66_5 | 3V66_5 Output Enable 1 = Enable; 0 = Disable NOTE: THIS BIT SHOULD BE USED WHEN PIN 24 IS CONFIGURED AS 3V66_5 OUTPUT. DO NOT CLEAR THIS BIT WHEN PIN 24 IS CONFIGURED AS 66IN INPUT. | R/W | 1 |
| Bit 2 | 23 | 66BUFF2 | 66-MHz Buffered 2 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |
| Bit 1 | 22 | 66BUFF1 | 66-MHz Buffered 1 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |
| Bit 0 | 21 | 66BUFF0 | 66-MHz Buffered 0 Output Enable 1 = Enabled; 0 = Disabled | R/W | 1 |

Data Byte 5

| Bit | Pin# | Name | Pin Description | Type | Power On Default |
|-------|------|--------------|--|------|------------------|
| Bit 7 | | N/A | N/A | R | 0 |
| Bit 6 | | N/A | N/A | R | 0 |
| Bit 5 | | 66BUFF [2:0] | Tpd 66IN to 66BUFF propagation delay control | R/W | 0 |
| Bit 4 | | 66BUFF [2:0] | | R/W | 0 |
| Bit 3 | | DOT | DOT edge rate control | R/W | 0 |
| Bit 2 | | DOT | | R/W | 0 |
| Bit 1 | | USB | USB edge rate control | R/W | 0 |
| Bit 0 | | USB | | R/W | 0 |

Byte 6: Vendor ID

| Bit | Description | Type | Power On Default |
|-------|---------------------|------|------------------|
| Bit 7 | Revision Code Bit 3 | R | 0 |
| Bit 6 | Revision Code Bit 2 | R | 0 |
| Bit 5 | Revision Code Bit 1 | R | 0 |
| Bit 4 | Revision Code Bit 0 | R | 1 |
| Bit 3 | Vendor ID Bit 3 | R | 0 |
| Bit 2 | Vendor ID Bit 2 | R | 1 |
| Bit 1 | Vendor ID Bit 1 | R | 0 |
| Bit 0 | Vendor ID Bit 0 | R | 0 |

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....-0.5 to +7.0V
 Input Voltage..... -0.5V to $V_{DD}+0.5$

Storage Temperature
 (Non-condensing).....-65°C to +150°C
 Max. Soldering Temperature (10 sec) +260°C
 Junction Temperature..... +150°C
 Package Power Dissipation..... 1W
 Static Discharge Voltage
 (per MIL-STD-883, Method 3015) > 2000V

Operating Conditions Over which Electrical Parameters are Guaranteed^[9]

| Parameter | Description | Min. | Max. | Unit |
|---|---|--------|----------|------|
| $V_{DD_REF}, V_{DD_PCI}, V_{DD_CORE}, V_{DD_3V66}, V_{DD_CPU}$ | 3.3V Supply Voltages | 3.135 | 3.465 | V |
| $V_{DD_48\text{ MHz}}$ | 48-MHz Supply Voltage | 2.85 | 3.465 | V |
| T_A | Operating Temperature, Ambient | 0 | 70 | °C |
| C_{in} | Input Pin Capacitance | | 5 | pF |
| C_{XTAL} | XTAL Pin Capacitance | | 22.5 | pF |
| C_L | Max. Capacitive Load on USBCLK, REF, PCICLK, 3V66 | | 20 30 | pF |
| $f_{(REF)}$ | Reference Frequency, Oscillator Nominal Value | 14.318 | 14.318 | MHz |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Max. | Unit | |
|-------------|---------------------------|--|---------------------------|------|------|--|
| V_{IH} | High-level Input Voltage | Except Crystal Pads. Threshold voltage for crystal pads = $V_{DD}/2$ | 2.0 | | V | |
| V_{IL} | Low-level Input Voltage | Except Crystal Pads | | 0.8 | V | |
| V_{OH} | High-level Output Voltage | USB, REF, 3V66 | $I_{OH} = -1\text{ mA}$ | 2.4 | V | |
| | | PCI | $I_{OH} = -1\text{ mA}$ | 2.4 | V | |
| V_{OL} | Low-level Output Voltage | USB, REF, 3V66 | $I_{OL} = 1\text{ mA}$ | 0.4 | V | |
| | | PCI | $I_{OL} = 1\text{ mA}$ | 0.55 | V | |
| I_{IH} | Input High Current | $0 \leq V_{IN} \leq V_{DD}$ | -5 | 5 | mA | |
| I_{IL} | Input Low Current | $0 \leq V_{IN} \leq V_{DD}$ | -5 | 5 | mA | |
| I_{OH} | High-level Output Current | CPU For $I_{OH} = 6 \cdot I_{Ref}$ Configuration | Type X1, $V_{OH} = 0.65V$ | 12.9 | mA | |
| | | | Type X1, $V_{OH} = 0.74V$ | 14.9 | | |
| | | REF, DOT, USB | Type 3, $V_{OH} = 1.00V$ | -29 | | |
| | | | Type 3, $V_{OH} = 3.135V$ | -23 | | |
| | | 3V66, DOT, PCI | Type 5, $V_{OH} = 1.00V$ | -33 | | |
| | | | Type 5, $V_{OH} = 3.135V$ | -33 | | |
| I_{OL} | Low-level Output Current | REF, DOT, USB | Type 3, $V_{OL} = 1.95V$ | 29 | mA | |
| | | | Type 3, $V_{OL} = 0.4V$ | 27 | | |
| | | 3V66, PCI | Type 5, $V_{OL} = 1.95V$ | 30 | | |
| | | | Type 5, $V_{OL} = 0.4V$ | 38 | | |
| I_{OZ} | Output Leakage Current | Three-state | | 10 | mA | |
| I_{DD3} | 3.3V Power Supply Current | $V_{DD_CORE}/V_{DD3.3} = 3.465V, F_{CPU} = 133\text{ MHz}$ | | 360 | mA | |
| I_{DDPD3} | 3.3V Shutdown Current | $V_{DD_CORE}/V_{DD3.3} = 3.465V$ | | 20 | mA | |

Note:

9. **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Switching Characteristics^[10] Over the Operating Range

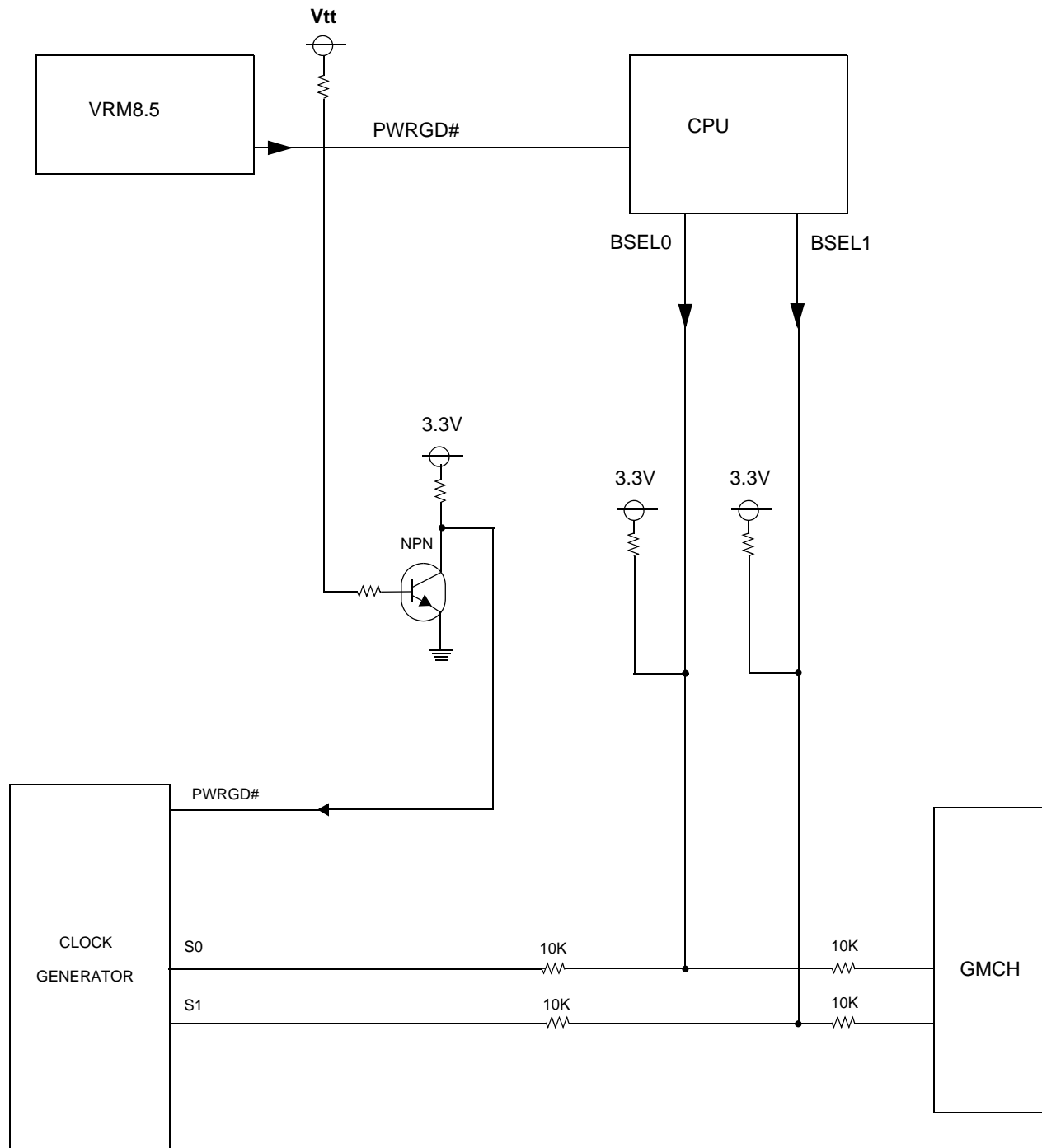
| Parameter | Output | Description | Test Conditions | Min. | Max. | Unit |
|---|---------------|---|--|-------|------|------|
| t ₁ | All | Output Duty Cycle ^[11] | Measured at 1.5V | 45 | 55 | % |
| t ₃ | USB, REF, DOT | Falling Edge Rate | Between 2.4V and 0.4V | 0.5 | 2.0 | ps |
| t ₃ | PCI,3V66 | Falling Edge Rate | Between 2.4V and 0.4V | 1.0 | 4.0 | V/ns |
| t ₅ | 3V66[0:1] | 3V66-3V66 Skew | Measured at 1.5V | | 500 | ps |
| t ₅ | 66BUFF[0:2] | 66BUFF-66BUFF Skew | Measured at 1.5V | | 175 | ps |
| t ₆ | PCI | PCI-PCI Skew | Measured at 1.5V | | 500 | ps |
| t ₇ | 3V66,PCI | 3V66-PCI Clock Jitter | 3V66 leads. Measured at 1.5V | 1.5 | 3.5 | ns |
| t ₉ | 3V66 | Cycle-Cycle Clock Jitter | Measured at 1.5V t ₉ = t _{9A} - t _{9B} | | 250 | ps |
| t ₉ | USB, DOT | Cycle-Cycle Clock Jitter | Measured at 1.5V t ₉ = t _{9A} - t _{9B} | | 350 | ps |
| t ₉ | PCI | Cycle-Cycle Clock Jitter | Measured at 1.5V t ₉ = t _{9A} - t _{9B} | | 500 | ps |
| t ₉ | REF | Cycle-Cycle Clock Jitter | Measured at 1.5V t ₉ = t _{9A} - t _{9B} | | 1000 | ps |
| CPU 1.0V Switching Characteristics | | | | | | |
| t ₂ | CPU | RiseTime | Measured differential waveform from -0.35V to +0.35V | 175 | 467 | ps |
| t ₃ | CPU | Fall Time | Measured differential waveform from -0.35V to +0.35V | 175 | 467 | ps |
| t ₄ | CPU | CPU-CPU Skew | Measured at Crossover | | 150 | ps |
| t ₈ | CPU | Cycle-Cycle Clock Jitter | Measured at Crossover t ₈ = t _{8A} - t _{8B} | | 150 | ps |
| | CPU | Rise/Fall Matching | Measured with test loads ^[12] | | 325 | mV |
| V _{oh} | CPU | High-level Output Voltage including overshoot | Measured with test loads ^[12] | 0.92 | 1.45 | V |
| V _{ol} | CPU | Low-level Output Voltage including undershoot | Measured with test loads ^[12] | -0.2 | 0.35 | V |
| V _{crossover} | CPU | Crossover Voltage | Measured with test loads ^[12] | 0.51 | 0.76 | V |
| CPU 0.7V Switching Characteristics | | | | | | |
| t ₂ | CPU | RiseTime | Measured single ended waveform from 0.175V to 0.525V | 175 | 700 | ps |
| t ₃ | CPU | Fall Time | Measured single ended waveform from 0.175V to 0.525V | 175 | 700 | ps |
| t ₄ | CPU | CPU-CPU Skew | Measured at Crossover | | 150 | ps |
| t ₈ | CPU | Cycle-Cycle Clock Jitter | Measured at Crossover t ₈ = t _{8A} - t _{8B} With all outputs running | | 150 | ps |
| | CPU | Rise/Fall Matching | Measured with test loads ^[13, 14] | | 20 | % |
| V _{oh} | CPU | High-level Output Voltage including overshoot | Measured with test loads ^[14] | | 0.85 | V |
| V _{ol} | CPU | Low-level Output Voltage including undershoot | Measured with test loads ^[14] | -0.15 | | V |
| V _{crossover} | CPU | Crossover Voltage | Measured with test loads ^[14] | 0.28 | 0.43 | V |

Notes:

10. All parameters specified with loaded outputs.
11. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.
12. The 1.0V test load is shown on test circuit page.
13. Determined as a fraction of 2*(Trp - Trn)/(Trp + Trn) Where Trp is a rising edge and Trp is an intersecting falling edge.
14. The 0.7V test load is R_s = 33.2Ω, R_p = 49.9Ω in test circuit.

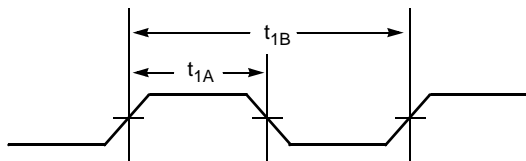


Definition and Application of PWRGD# Signal

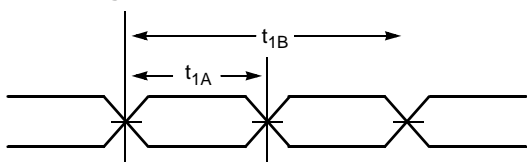


Switching Waveforms

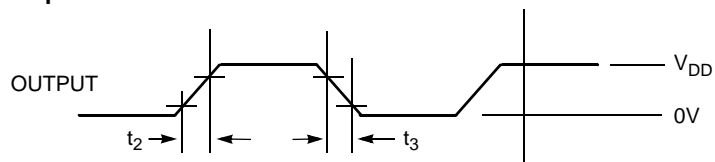
Duty Cycle Timing (Single Ended Output)



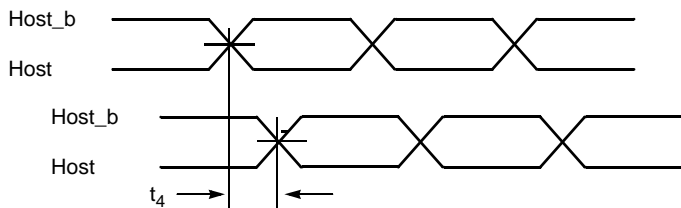
Duty Cycle Timing (CPU Differential Output)



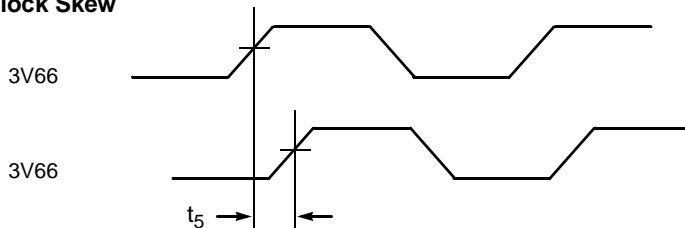
All Outputs Rise/Fall Time



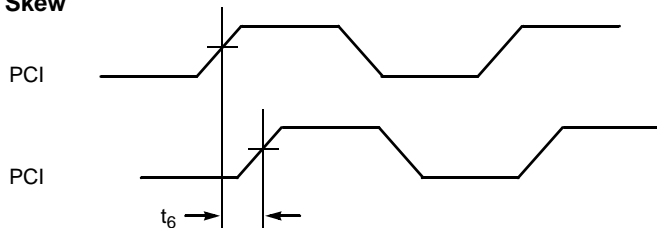
CPU-CPU Clock Skew



3V66-3V66 Clock Skew



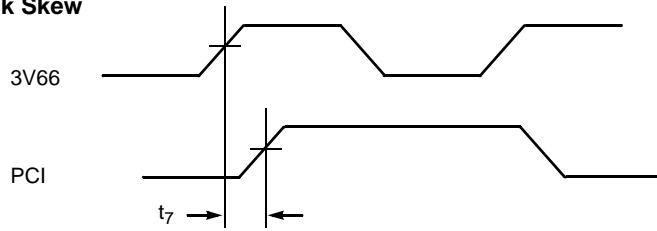
PCI-PCI Clock Skew



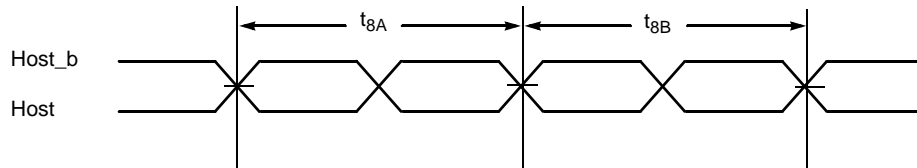


Switching Waveforms (continued)

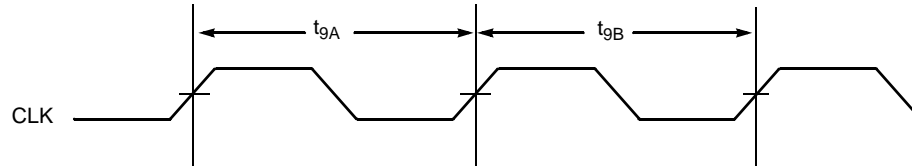
3V66-PCI Clock Skew



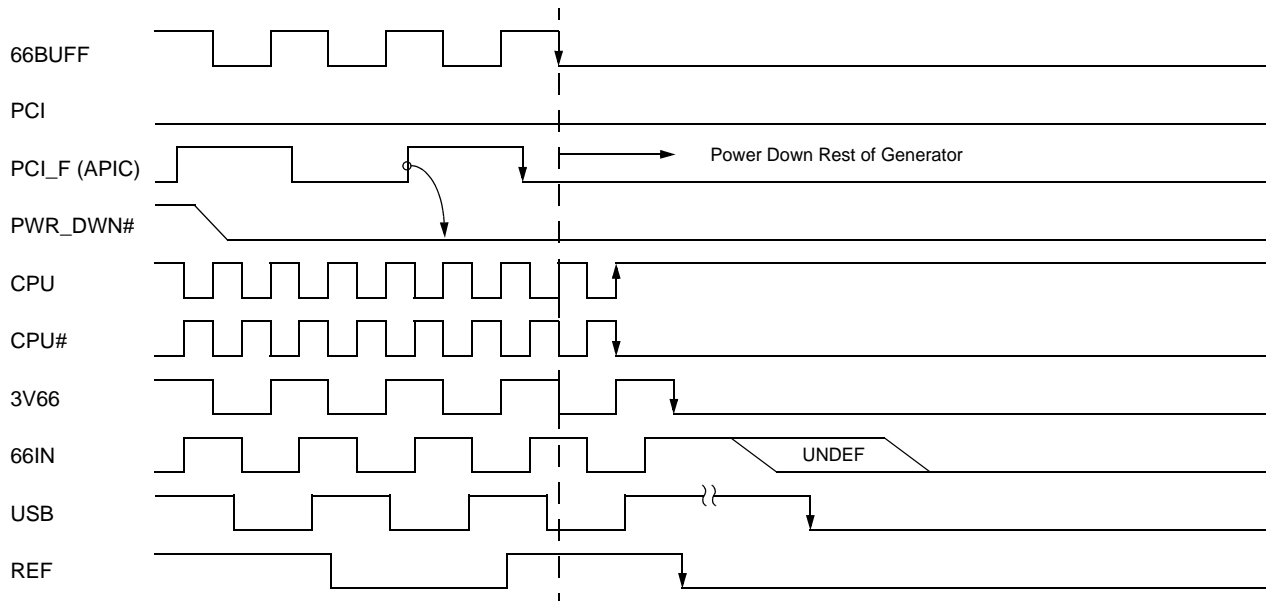
CPU Clock Cycle-Cycle Jitter



Cycle-Cycle Clock Jitter

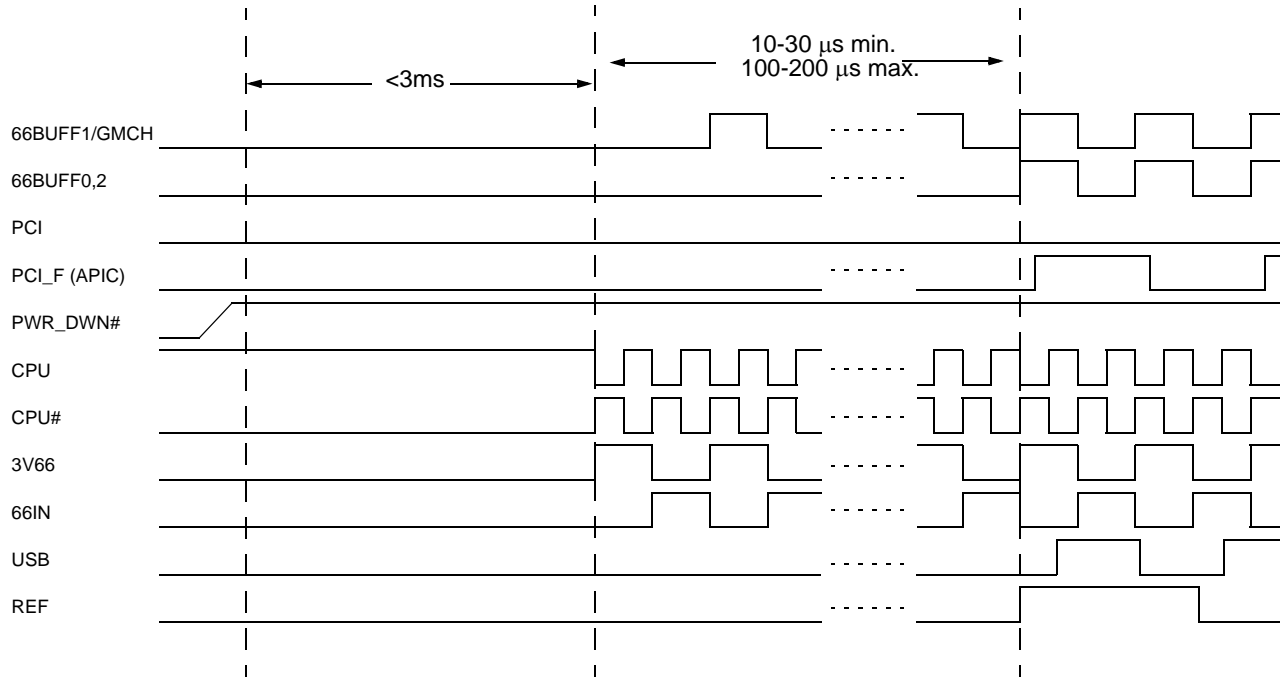


PWRDWN# Assertion^[15]



Note:
15. PCI_STOP# asserted LOW.

PWRDWN# Deassertion^[15]



PWRGD# Timing Diagrams

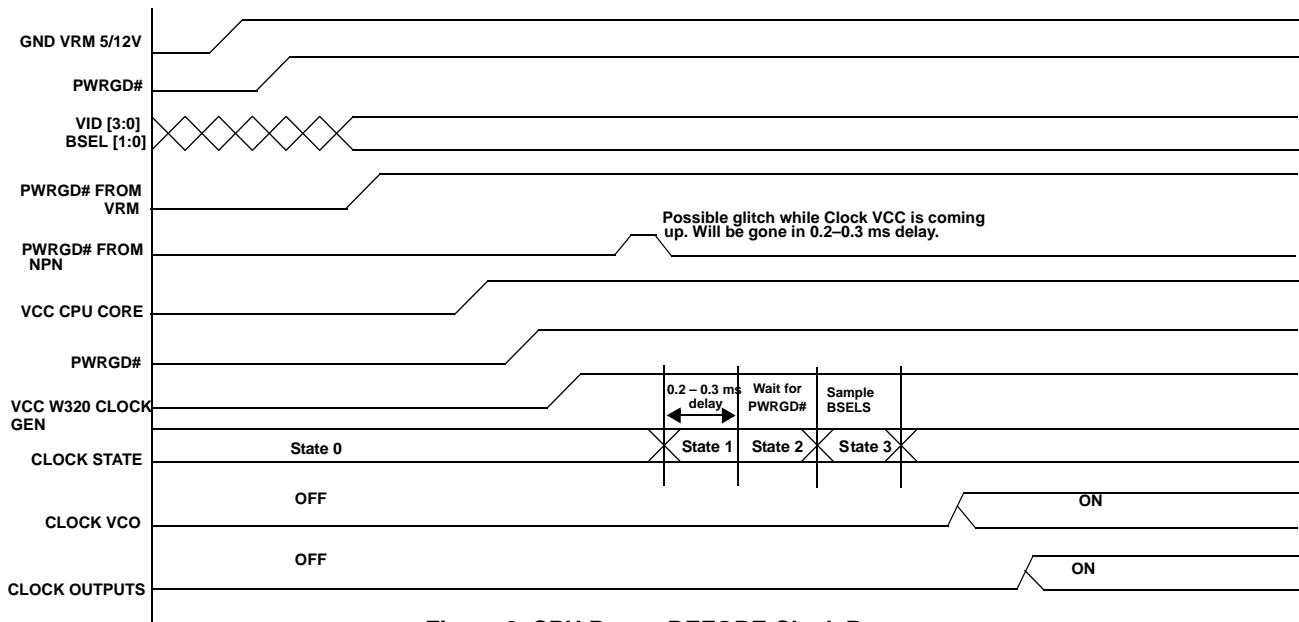


Figure 2. CPU Power BEFORE Clock Power

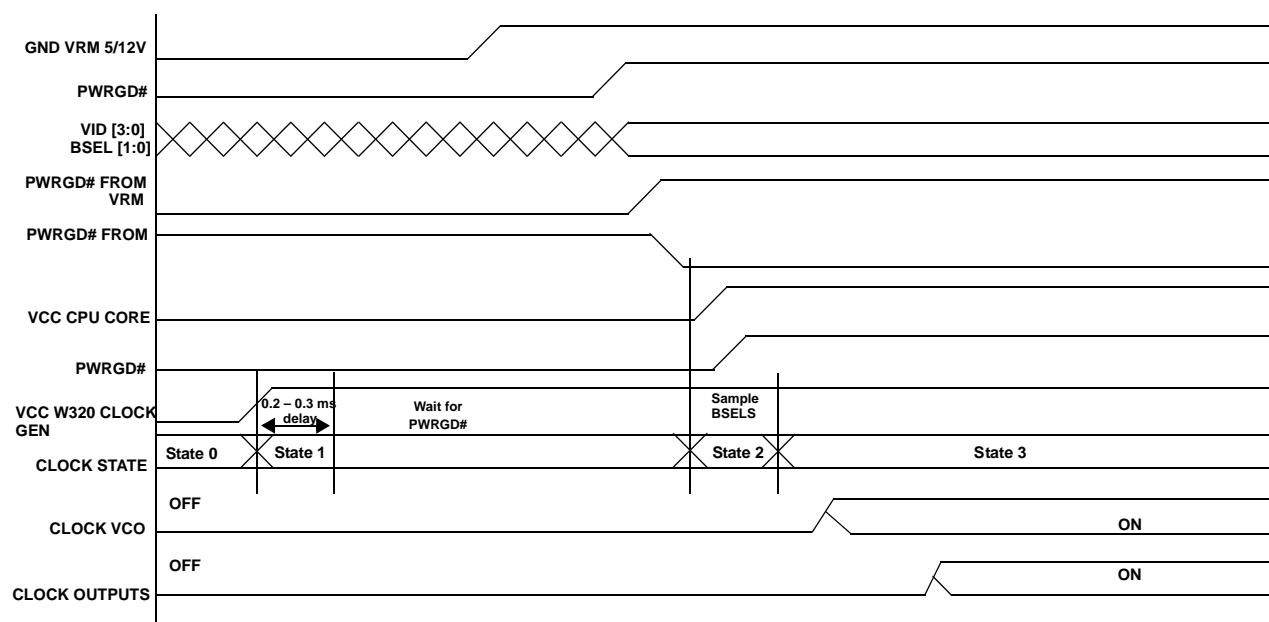
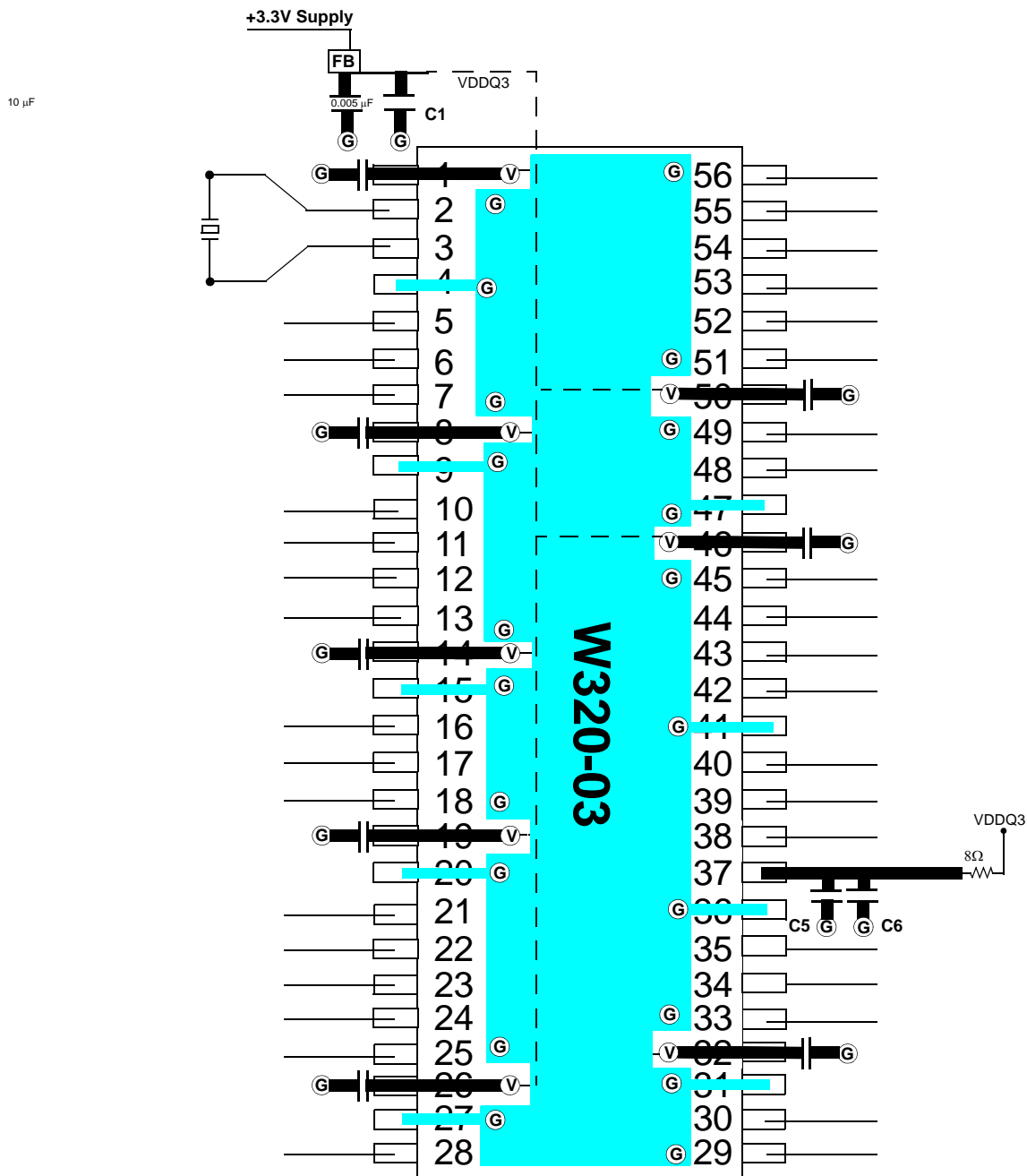


Figure 3. CPU Power AFTER Clock Power



Layout Example



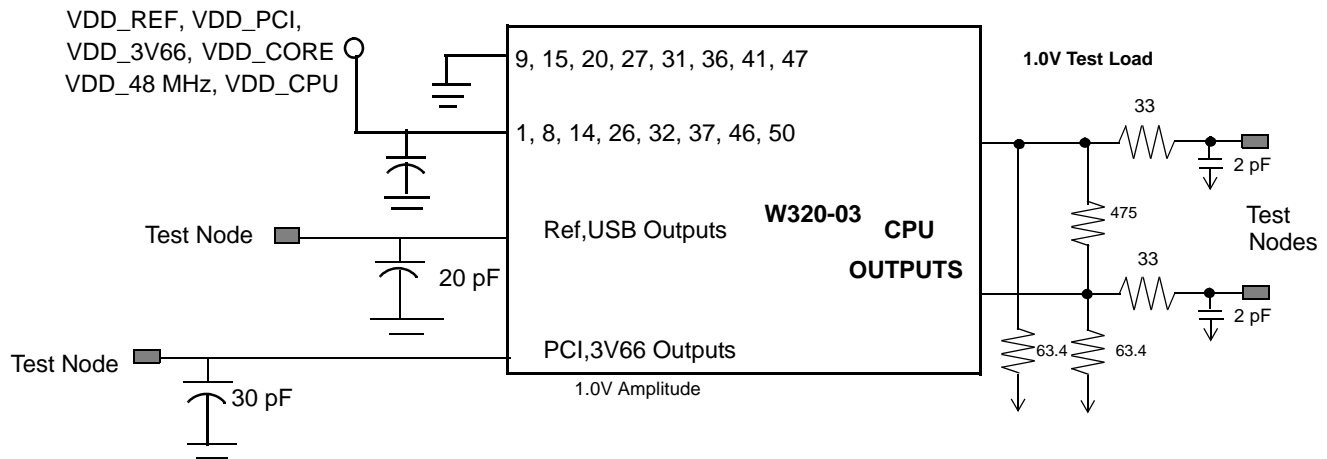
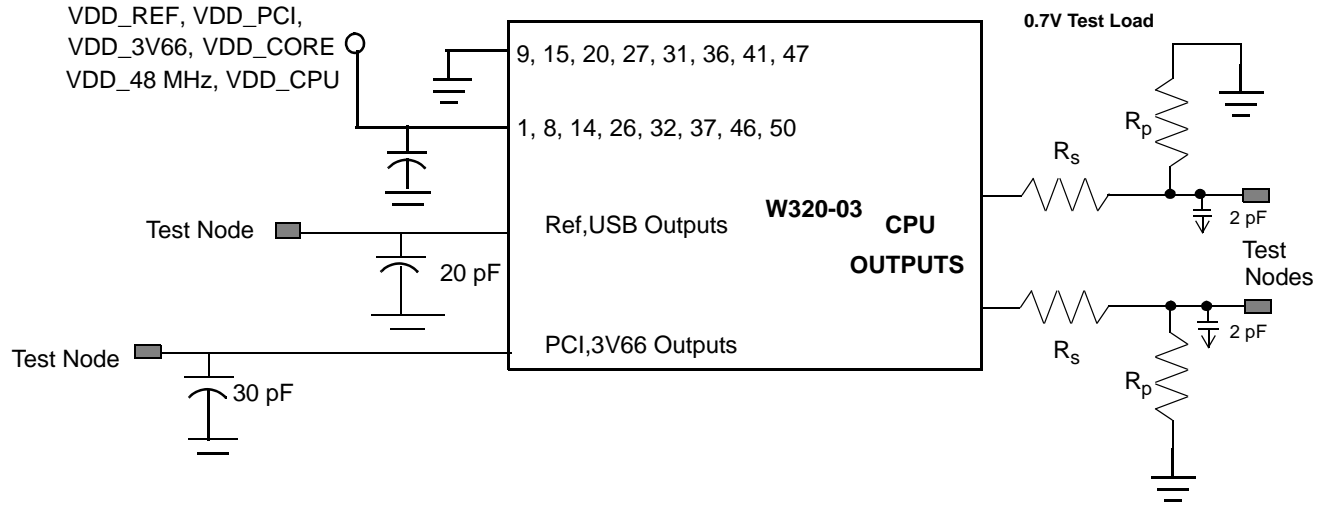
FB = Dale ILB1206 - 300 or 2TDKACB2012L-120 or 2 Murata BLM21B601S

Ceramic Caps C1 = 10–22 μF C2 = 0.005 μF C5 = 0.1 μF C6 = 10 μF

ⓐ = VIA to GND plane layer ⓑ = VIA to respective supply plane layer

Note: Each supply plane or strip should have a ferrite bead and capacitors

Test Circuit^[16, 17]



Ordering Information

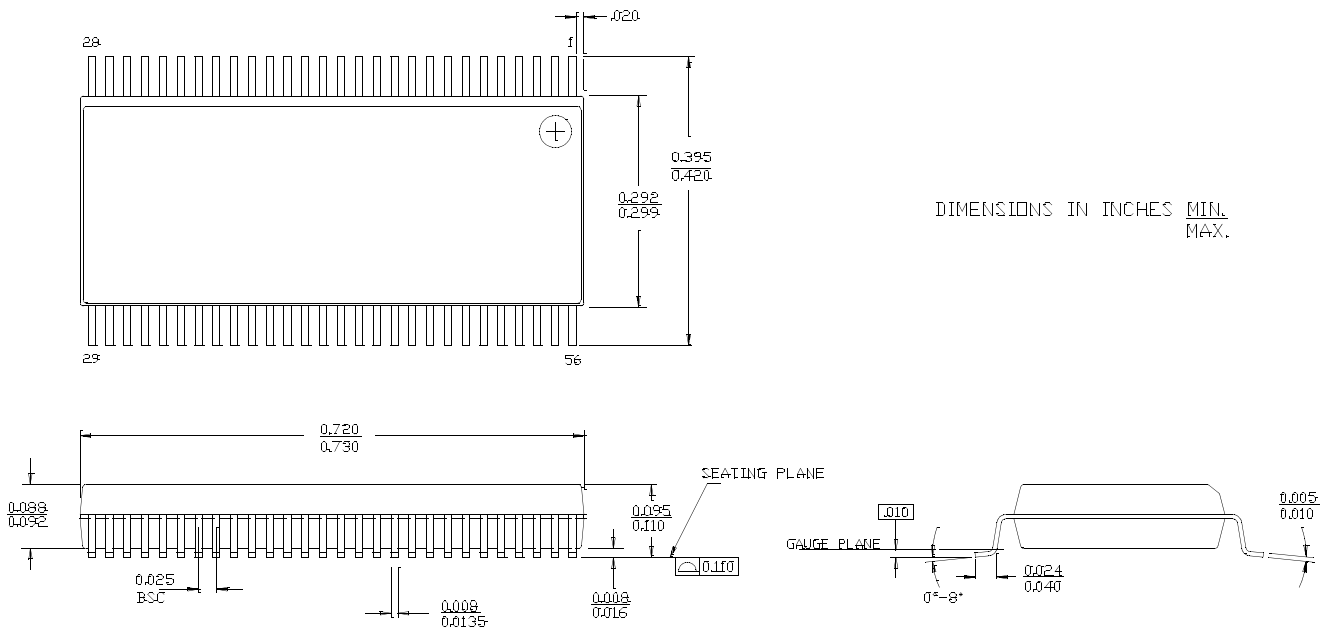
| Ordering Code | Package Type | Operating Range |
|------------------|------------------------------|-----------------|
| W320-03H | 56-pin SSOP | Commercial |
| W320-03HT | 56-pin SSOP - Tape and Reel | Commercial |
| W320-03X | 56-pin TSSOP | Commercial |
| W320-03XT | 56-pin TSSOP - Tape and Reel | Commercial |
| Lead-free | | |
| CYW320OXC-3 | 56-pin SSOP | Commercial |
| CYW320OXC-3T | 56-pin SSOP - Tape and Reel | Commercial |

Notes:

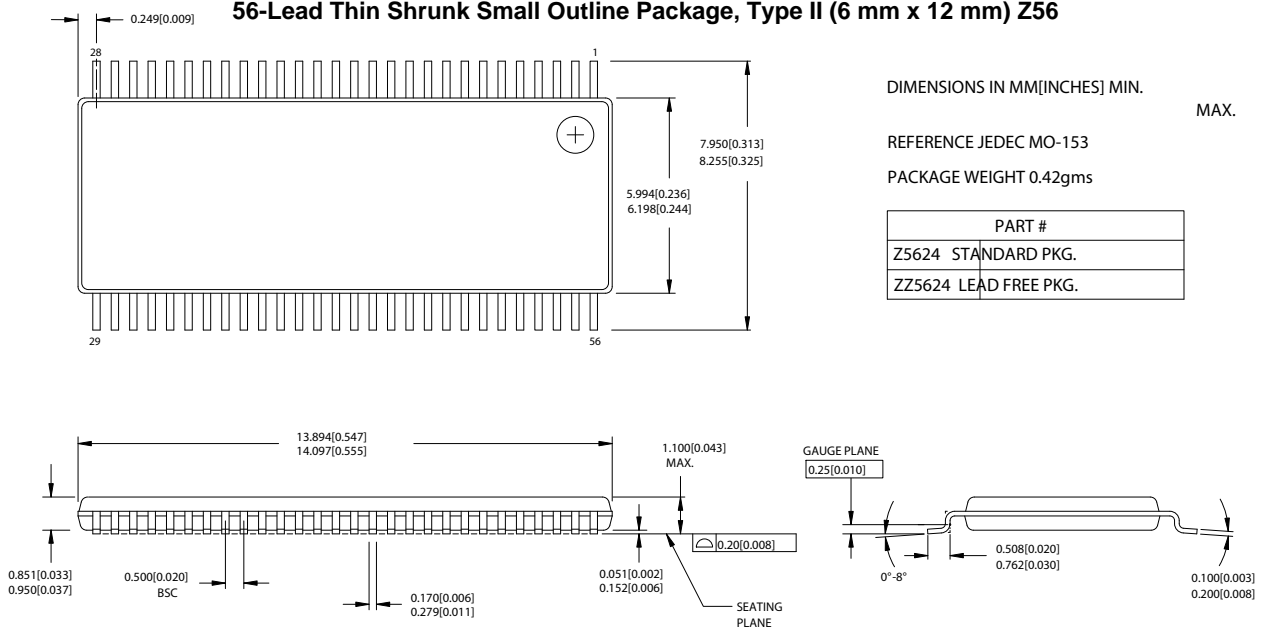
- 16. Each supply pin must have an individual decoupling capacitor.
- 17. All capacitors must be placed as close to the pins as is physically possible. 0.7V amplitude: $R_S = 33\Omega$ $R_P = 50\Omega$.

Package Diagrams

56-lead Shrunken Small Outline Package O56



56-Lead Thin Shrunken Small Outline Package, Type II (6 mm x 12 mm) Z56



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