



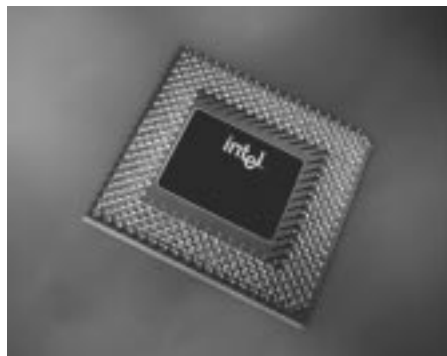
Intel® Celeron™ Processor

Datasheet

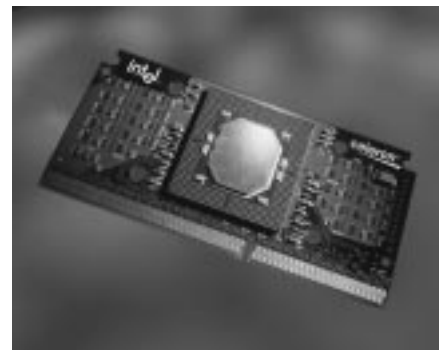
Product Features

- Available at 500 MHz, 466 MHz, 433 MHz, 400 MHz, 366 MHz, 333 MHz, and 300A MHz core frequencies with 128 KB level-two cache; 300 MHz and 266 MHz core frequencies without level-two cache.
- Binary compatible with applications running on previous members of the Intel microprocessor line.
- Dynamic execution microarchitecture.
- Operates on a 66 MHz, transaction-oriented system bus.
- Specifically designed for valued PC systems: based on the same P6 microarchitecture used in the Pentium® II processor with the capabilities of MMX™ technology.
- Power Management capabilities.
- Optimized for 32-bit applications running on advanced 32-bit operating systems.
- Uses cost-effective packaging technology.
 - Single Edge Processor (S.E.P.) Package to maintain compatibility with SC242 (processor core frequencies (MHz): 266, 300, 300A, 333, 366, 400, 433).
 - Plastic Pin Grid Array (PPGA) Package (processor core frequencies (MHz): 300A, 333, 366, 400, 433, 466, 500).
- Integrated high performance 32 KB instruction and data, nonblocking, level-one cache: separate 16 KB instruction and 16 KB data caches.
- Integrated thermal diode.

The Intel® Celeron™ processor is designed for Value PC desktops and is binary compatible with previous generation Intel architecture processors. The Intel® Celeron processor provides good performance for applications running on advanced operating systems such as Windows* 95/98, Windows* NT, and UNIX*. This is achieved by integrating the best attributes of Intel processors—the dynamic execution performance of the P6 microarchitecture plus the capabilities of MMX™ technology—bringing a balanced level of performance to the Value PC market segment. The Intel® Celeron processor offers the dependability you would expect from Intel at an exceptional value. Systems based on Intel® Celeron processors also include the latest features to simplify system management and lower the cost of ownership for small business and home environments.



PPGA Package



S.E.P. Package



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1.0 Introduction

The Intel® Celeron™ processor is based on the P6 microarchitecture and is optimized for the Value PC market segment. The Intel Celeron processor, like the Pentium® II processor, features a Dynamic Execution microarchitecture and executes MMX technology instructions for enhanced media and communication performance. The Intel Celeron processor also utilizes multiple low-power states such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep to conserve power during idle times.

The Intel Celeron processor is capable of running today's most common PC applications with up to 4 GB of cacheable memory space. As this processor is intended for Value PC systems, it does not provide multiprocessor support. The Pentium II and Pentium® III processors should be used for multiprocessor system designs.

To be cost-effective at both the processor and system level, the Intel Celeron processor utilizes two cost-effective packaging technologies. They are the S.E.P. (Single-Edge Processor) Package and PPGA (Plastic Pin Grid Array) package. Refer to the *Intel® Celeron™ Processor Specification Update* for the latest packaging and frequency support information (Order Number 243337).

Note: This datasheet describes the Intel Celeron processor for both the PPGA package and the S.E.P. Package versions. Unless otherwise specified, the information in this document applies to both versions.

1.1 Terminology

In this document, a '#' symbol after a signal name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven to a low level. For example, when FLUSH# is low, a flush has been requested. When NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D#[3:0] = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

The term "system bus" refers to the interface between the processor, system core logic (a.k.a. the AGPset components), and other bus agents. The system bus is an interface to the processor, memory, and I/O.

1.1.1 Package Terminology

The following terms are used often in this document and are explained here for clarification:

- **Processor substrate**—The structure on which passive components (resistors and capacitors) are mounted.
- **Processor core**—The processor's execution engine.
- **S.E.P. Package**—Single-Edge Processor Package, which consists of a processor substrate, processor core, and passive components. This package differs from the S.E.C. Cartridge as this processor has no external plastic cover, thermal plate, or latch arms.
- **PPGA package**—Plastic Pin Grid Array package. The package is a pinned laminated printed circuit board structure.

Additional terms referred to in this and other related documentation:

- **SC242**—242-contact slot connector. A processor in the S.E.P. Package uses this connector to interface with a system board.
- **370-pin socket (PGA370)**—The zero insertion force (ZIF) socket in which a processor in the PPGA package will use to interface with a system board.
- **Retention mechanism**—A mechanical assembly which holds the package in the SC242 connector.

1.2 References^{1,2}

The reader of this specification should also be familiar with material and concepts presented in the following documents:

- Intel® Celeron™ Processor Support Component Suppliers (<http://developer.intel.com/design/celeron/componets/>)
- AP-485, *Intel Processor Identification and the CPUID Instruction* (Order Number 241618)
- AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330)
- AP-586, *Pentium® II Processor Thermal Design Guidelines* (Order Number 243331)
- AP-587, *Pentium® II Processor Power Distribution Guidelines* (Order Number 243332)
- AP-589, *Design for EMI* (Order Number 243334)
- *Pentium® II Processor at 233, 266, 300, and 333 MHz Datasheet* (Order Number 243335)
- *Pentium® II Processor at 350, 400, and 450 MHz Datasheet* (Order Number 243657)
- Intel® Celeron™ Processor Specification Update (Order Number 243337)
- *SC242 Connector Design Guidelines* (Order Number 243397)
- *Pentium® II Processor Developer's Manual* (Order Number 243502)
- *370-Pin Socket (PGA370) Design Guidelines* (Order Number 244410)
- *Intel Architecture Software Developer's Manual* (Order Number 243193)
 - *Volume I: Basic Architecture* (Order Number 243190)
 - *Volume II: Instruction Set Reference* (Order Number 243191)
 - *Volume III: System Programming Guide* (Order Number 243192)

- *Pentium® II Processor I/O Buffer Models*, Quad XTK Format (Electronic Form)
- *Intel® 440EX AGPset Design Guide* (Order Number 290637)
- *Intel® Celeron™ Processor with the Intel® 440LX AGPset Design Guide* (Order Number 245088)
- *Intel® 440BX AGPset Design Guide* (Order Number 290634)
- *Intel® Celeron™ Processor with the Intel® 440ZX-66 AGPset Design Guide* (Order Number 245126)
- *Intel® Celeron™ Processor (PPGA) at 466 MHz Thermal Solutions Guidelines* (Order Number 245156)

Notes:

1. This reference material can be found on the Intel Developer's Website located at:
<http://developer.intel.com>
2. For a complete listing of the Intel® Celeron™ processor reference material, refer to the Intel Developer's Website when this processor is formally launched. The website is located at:
<http://developer.intel.com/design/celeron/>

2.0 Electrical Specifications

2.1 The Intel® Celeron™ Processor System Bus and V_{REF}

Intel® Celeron processor signals use a variation of the low voltage Gunning Transceiver Logic (GTL) signaling technology. The Intel Celeron processor system bus specification is similar to the GTL specification, but has been enhanced to provide larger noise margins and reduced ringing. The improvements are accomplished by increasing the termination voltage level and controlling the edge rates. Because this specification is different from the standard GTL specification, it is referred to as Assisted Gunning Transceiver Logic (AGTL+) in this document.

The Intel® Celeron processor varies from the Pentium Pro processor in its output buffer implementation. The buffers that drive the system bus signals on the Intel® Celeron processor are actively driven to $V_{CC_{CORE}}$ for one clock cycle during the low-to-high transition. This improves rise times and reduces overshoot. These signals should still be considered open-drain and require termination to a supply that provides the logic-high signal level.

The AGTL+ inputs use differential receivers which require a reference signal (V_{REF}). V_{REF} is used by the receivers to determine if a signal is a logic-high or a logic-low, and is provided to the processor core by either the processor substrate (S.E.P. Package) or the motherboard (PPGA package). Local V_{REF} copies should be generated on the motherboard for all other devices on the AGTL+ system bus.

Termination is used to pull the bus up to the high voltage level and to control reflections on the transmission line. The processor may contain termination resistors (S.E.P. Package only) that provide termination for one end of the Intel Celeron processor system bus. Otherwise, this termination must exist on the motherboard.

The AGTL+ bus depends on incident wave switching. Therefore timing calculations for AGTL+ signals are based on motherboard **flight time** as opposed to capacitive deratings. Analog signal simulation of the Intel Celeron processor system bus, including trace lengths, is highly recommended when designing a system. See the *Pentium® II Processor AGTL+ Layout Guidelines* and the *Pentium® II Processor I/O Buffer Models, Quad Format* (Electronic Form) for details.

2.2 Clock Control and Low Power States

Intel® Celeron processors allow the use of AutoHALT, Stop-Grant, Sleep, and Deep Sleep states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See [Figure 1](#) for a visual representation of the Intel Celeron processor low power states.

For the processor to fully realize the low current consumption of the Stop-Grant, Sleep, and Deep Sleep states, a Model Specific Register (MSR) bit must be set. For the MSR at 02AH (Hex), bit 26 must be set to a '1' (this is the power on default setting) for the processor to stop all internal clocks during these modes. For more information, see the *Pentium® II Processor Developer's Manual* (Order Number 243502).

2.2.1 Normal State—State 1

This is the normal operating state for the processor.

2.2.2 AutoHALT Power Down State—State 2

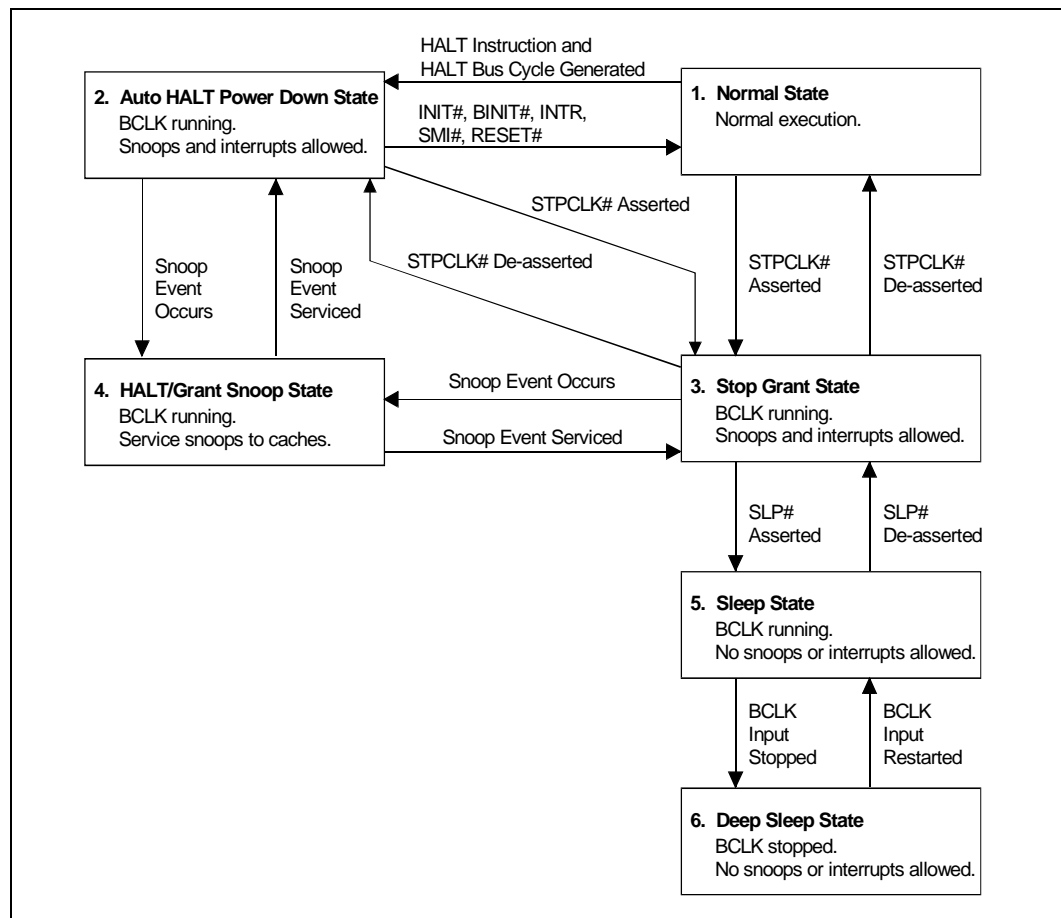
AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* (Order Number 243192) for more information.

FLUSH# will be serviced during the AutoHALT state, and the processor will return to the AutoHALT state.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

Figure 1. Clock Control State Machine



2.2.3 Stop-Grant State—State 3

The Stop-Grant state on the processor is entered when the STPCLK# signal is asserted.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from Stop-Grant state.

FLUSH# will not be serviced during Stop-Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the deassertion of the STPCLK# signal.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see [Section 2.2.4](#)). A transition to the Sleep state (see [Section 2.2.4](#)) will occur with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT#, and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

2.2.4 HALT/Grant Snoop State—State 4

The processor will respond to snoop transactions on the Intel® Celeron processor system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the Intel Celeron processor system bus has been serviced (whether by the processor or another agent on the Intel Celeron processor system bus). After the snoop is serviced, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

2.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the SLP# pin can be asserted, causing the processor to enter the Sleep state. The SLP# pin is not recognized in the Normal or AutoHALT states.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering its lowest power state, the Deep Sleep state, by stopping the BCLK input. (See [Section 2.2.6](#).) Once in the Sleep state, the SLP# pin can be deasserted if another asynchronous system bus event occurs. The SLP# pin has a minimum assertion of one BCLK period.

2.2.6 Deep Sleep State—State 6

The Deep Sleep state is the lowest power state the processor can enter while maintaining context. The Deep Sleep state is entered by stopping the BCLK input (after the Sleep state was entered from the assertion of the SLP# pin). The processor is in Deep Sleep state immediately after BCLK is stopped. It is recommended that the BCLK input be held low during the Deep Sleep State. Stopping of the BCLK input lowers the overall current consumption to leakage levels.

To re-enter the Sleep state, the BCLK input must be restarted. A period of 1 ms (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep State. Once in the Sleep state, the SLP# pin can be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals are allowed on the system bus while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

2.2.7 Clock Control

When the processor is in the Sleep or Deep Sleep states, it will not respond to interrupts or snoop transactions. PICCLK should not be removed during the AutoHALT Power Down or Stop-Grant states. PICCLK can be removed during the Sleep or Deep Sleep states. When transitioning from the Deep Sleep state to the Sleep state, PICCLK must be restarted with BCLK.

2.3 Intel® Celeron™ Processor Power and Ground Pins

There are five pins defined on the S.E.P. Package for voltage identification (VID) and there are four pins on the PPGA package. These pins specify the voltage required by the processor core. These have been added to cleanly support voltage specification variations on current and future Intel® Celeron processors.

For clean on-chip power distribution, Intel Celeron processors in the S.E.P. Package have 27 V_{CC} (power) and 30 V_{SS} (ground) inputs. The 27 V_{CC} pins are further divided to provide the different voltage levels to the components. $V_{CC_{CORE}}$ inputs for the processor core account for 19 of the V_{CC} pins, while 4 V_{TT} inputs (1.5 V) are used to provide a AGTL+ termination voltage to the processor. For only the S.E.P. Package, one V_{CC_5} pin is provided for Voltage Transient Tools. V_{CC_5} and $V_{CC_{CORE}}$ must remain electrically separated from each other.

The PPGA package has more power (88) and ground (80) pins than the S.E.P. Package. Of the power pins, 77 are used for the processor core ($V_{CC_{CORE}}$) and 8 are used as a AGTL+ reference voltage (V_{REF}). The other 3 power pins are $V_{CC_{1.5}}$, $V_{CC_{2.5}}$ and $V_{CC_{CMOS}}$ and are used for future processor compatibility.

The $V_{CC_{CMOS}}$ pin is provided as a feature for future processor support in a flexible design. In such a design, the $V_{CC_{CMOS}}$ pin is used to provide the CMOS voltage for use by the platform. Additionally, 2.5 V must be provided to the $V_{CC_{2.5}}$ input and 1.5 V must be provided to the $V_{CC_{1.5}}$ input. The processor routes the CMOS voltage level through the package that it is compatible with. For example, future processors requiring 1.5 V CMOS voltage levels route 1.5 V to the $V_{CC_{CMOS}}$ output.

Each power signal, regardless of package, must meet the specifications stated in Table 4. In addition, all $V_{CC_{CORE}}$ pins must be connected to a voltage island while all V_{SS} pins have to connect to a system ground plane.

2.4 Intel® Celeron™ Processor Decoupling

Due to the large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This causes voltages on power planes to sag below their nominal values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 4. Failure to do so can result in timing violations or a reduced lifetime of the component.

2.4.1 Intel® Celeron™ Processor System Bus AGTL+ Decoupling

The S.E.P. Package contains high frequency decoupling capacitance on the processor substrate, where the PPGA package does not. Therefore, Intel® Celeron™ processors in the PPGA package require high frequency decoupling on the system motherboard. Bulk decoupling must be provided on the motherboard for proper AGTL+ bus operation for both packages. See AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330), AP-587, *Pentium® II Processor Power Distribution Guidelines* (Order Number 243332), and the *Pentium® II Processor Developer's Manual* (Order Number 243502) for more information.

2.5 Voltage Identification

The processor's voltage identification (VID) pins can be used to automatically select the $V_{CC_{CORE}}$ voltage from a compatible voltage regulator. There are five VID pins (VID[4:0]) on the S.E.P. Package, while there are only four (VID[3:0]) on the PPGA package. This is because there are no Intel® Celeron™ processors in the PPGA package that require more than 2.05 V (see Table 1).

VID pins are not signals, but rather are an open or short circuit to V_{SS} on the processor. The combination of opens and shorts defines the processor core's required voltage. The VID pins also allow for compatibility with current and future Intel Celeron processors.

Note that the '1111' (all opens) ID can be used to detect the absence of a processor core in a given slot (S.E.P. Package only), as long as the power supply used does not affect the VID signals. Detection logic and pull-ups should not affect VID inputs at the power source (see Section 7.0).

External logic monitoring the VID signals or the voltage regulator may require the VID pins to be pulled-up. If this is the case, the VID pins should be pulled up to a TTL-compatible level with external resistors to the power source of the regulator.

The power source chosen must be guaranteed to be stable whenever the voltage regulator's supply is stable. This will prevent the possibility of the processor supply going above the specified $V_{CC_{CORE}}$ in the event of a failure in the supply for the VID lines. In the case of a DC-to-DC converter, this can be accomplished by using the input voltage to the converter for the VID line pull-ups. In addition, the power supply must supply the requested voltage or disable itself.

Table 1. Voltage Identification Definition ^{1, 2, 3, 5}

Processor Pins					
VID4 (S.E.P. Only)	VID3	VID2	VID1	VID0	V _{CC} CORE
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00 ³
0	0	0	0	0	2.05
1	1	1	1	1	No Core
1	1	1	1	0	2.1

NOTES:

- 0 = Processor pin connected to V_{SS}.
- 1 = Open on processor; may be pulled up to TTL V_{IH} on motherboard.
- The Intel® Celeron™ processor core will be powered off 2.0 V.
- VID4 applies only to the S.E.P. Package. VID[3:0] applies to both S.E.P. and PPGA packages.
- For PPGA, only the shaded area applies.

2.6 Intel® Celeron™ Processor System Bus Unused Pins

All RESERVED pins must remain unconnected. Connection of these pins to V_{CC}CORE, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future Intel® Celeron™ processor products. See [Section 5.0](#) for a pin listing of the processor and the location of each RESERVED pin.

For Intel Celeron processors in the S.E.P. Package, the TESTHI pin must be at a logic-high level when the core power supply comes up. For more information, please refer to erratum C26 of the *Intel® Celeron™ Processor Specification Update* (Order Number 243748). Also note that the TESTHI signal is not available on Intel Celeron processors in the PPGA package.

PICCLK must be driven with a valid clock input and the PICD[1:0] lines must be pulled-up to 2.5 V even when the APIC will not be used. A separate pull-up resistor must be provided for each PICD line.

For reliable operation, always connect unused inputs or bi-directional signals to their deasserted signal level. The pull-up or pull-down resistor value is system dependent and should be chosen such that the logic-high (V_{IH}) and logic-low (V_{IL}) requirements are met.

For the S.E.P. Package, unused AGTL+ inputs should not be connected as the package substrate has termination resistors. On the other hand, PPGA does not have AGTL+ termination in its package and must have any unused AGTL+ inputs terminated through a pull-up resistor.

For unused CMOS inputs, active-low signals should be connected through a pull-up resistor to meet V_{IH} requirements and active-high signals should be connected through a pull-down resistor to meet V_{IL} requirements. Unused CMOS outputs can be left unconnected. A resistor must be used when tying bi-directional signals to power or ground. For any signal pulled to either power or ground, a resistor will allow for system testability.

2.7 Intel® Celeron™ Processor System Bus Signal Groups

To simplify the following discussion, the Intel® Celeron™ processor system bus signals have been combined into groups by buffer type. **All Intel® Celeron™ processor system bus outputs are open drain** and require a high-level source provided externally by the termination or pull-up resistor.

AGTL+ input signals have differential input buffers, which use V_{REF} as a reference signal. AGTL+ output signals require termination to 1.5 V. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

EMI pins (S.E.P. Package only) should be connected to motherboard ground and/or to chassis ground through zero ohm ($0\ \Omega$) resistors. The zero ohm resistors should be placed in close proximity to the SC242 connector. The path to chassis ground should be short in length and have a low impedance.

The CMOS, Clock, APIC, and TAP inputs can each be driven from ground to 2.5 V. The CMOS, APIC, and TAP outputs are open drain and should be pulled high to 2.5 V. This ensures not only correct operation for current Intel Celeron processors, but compatibility for future Intel Celeron processor products as well.

The groups and the signals contained within each group are shown in [Table 2](#). Refer to [Section 7.0](#) for descriptions of these signals.

Table 2. Intel® Celeron™ Processor System Bus Signal Groups

Group Name	Signals
AGTL+ Input	BPRI#, DEFER#, RESET#, RS[2:0]#, TRDY#
AGTL+ Output	PRDY#
AGTL+ I/O	A[31:3]#, ADS#, BNR#, BP[3:2]#, BPM[1:0]#, BR0#, D[63:0]#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#,
CMOS Input ⁴	A20M#, FLUSH#, IGNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, PWRGOOD ¹ , SMI#, SLP# ² , STPCLK#
CMOS Output ⁴	FERR#, IERR#, THERMTRIP# ³
System Bus Clock	BCLK
APIC Clock	PICCLK
APIC I/O ⁴	PICD[1:0]
TAP Input ⁴	TCK, TDI, TMS, TRST#
TAP Output ⁴	TDO
Power/Other ⁵	BSEL, CPUPRES# ⁷ , EDGTRL ⁷ , EMI ⁶ , PLL[2:1] ⁷ , SLOTOCC# ⁶ , THERMDP, THERMDN, VCC _{1.5} ⁷ , VCC _{2.5} ⁷ , VCC _{L2} ⁵ , VCC ₅ ⁶ , VCC _{CMOS} ⁷ , VCC _{CORE} , VCC _{COREDET} ⁷ , VID[3:0] ⁷ , VID[4:0] ⁶ , VREF[7:0] ⁷ , VSS, VTT ⁶

NOTES:

1. See [Section 7.0](#) for information on the PWRGOOD signal.
2. See [Section 7.0](#) for information on the SLP# signal.
3. See [Section 7.0](#) for information on the THERMTRIP# signal.
4. These signals are specified for 2.5 V operation.

5. $V_{CC_{CORE}}$ is the power supply for the processor core. VID[4:0] and VID[3:0] are described in [Section 2.0](#). VTT is used to terminate the system bus and generate VREF on the processor substrate. Vss is system ground. V_{CC_5} is not connected to the Intel® Celeron™ processor. This supply is used for Voltage Transient Tools. SLOTOCC# is described in [Section 7.0](#). BSEL is described in [Section 2.7.2](#) and [Section 7.0](#). EMI pins are described in [Section 7.0](#). $V_{CC_{L2}}$ is a Pentium® II processor reserved signal provided to maintain compatibility with the Pentium® II processor and may be left as a no-connect for “Intel Celeron processor-only” designs.
6. Only applies to Intel Celeron processors in the S.E.P. Package.
7. Only applies to Intel Celeron processors in the PPGA package.

2.7.1 Asynchronous Vs. Synchronous for System Bus Signals

All AGTL+ signals are synchronous to BCLK. All of the CMOS, APIC, and TAP signals can be applied asynchronously to BCLK. All APIC signals are synchronous to PICCLK. All TAP signals are synchronous to TCK.

2.7.2 System Bus Frequency Select Signal (BSEL)

The BSEL pin has two functions. First, it acts as an output and can be used by an external clock generator to select the proper system bus frequency. Second, it acts as an input and can be used by a system BIOS to detect and report the processor core frequency. Please see the *Intel® Celeron™ Processor with the Intel® 440ZX-66 AGPset Design Guide* (Order Number 245126) for an example implementation of BSEL.

BSEL is 3.3 V tolerant for the S.E.P. Package, while it is 2.5 V tolerant on the PPGA package. A logic-low on BSEL is defined as 66 MHz.

2.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the Intel® Celeron™ processor be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting a 2.5 V input. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required with each driving a different voltage level.

A Debug Port may be placed at the start and end of the TAP chain with the TDI of the first component coming from the Debug Port and the TDO from the last component going to the Debug Port.

2.9 Maximum Ratings

[Table 3](#) contains the Intel® Celeron™ processor stress ratings only. Functional operation at the absolute maximum and minimum is not implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 3. Intel® Celeron™ Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T _{STORAGE}	Processor storage temperature	-40	85	°C	
V _{CC(All)}	Any processor supply voltage with respect to V _{SS}	-0.5	Operating voltage + 1.0	V	1, 2
V _{inAGTL+}	AGTL+ buffer DC input voltage with respect to V _{SS}	-0.3	V _{CC_{CORE}} + 0.7	V	
V _{inCMOS}	CMOS buffer DC input voltage with respect to V _{SS}	-0.3	3.3	V	3
I _{VID}	Max VID pin current		5	mA	
I _{SLOTOCC}	Max SLOTOCC# pin current		5	mA	5
I _{CPUPRES}	Max CPUPRES# pin current		5	mA	6
Mech Max Edge Fingers ⁵	Mechanical integrity of processor edge fingers		50	Insertions/Extractions	4, 5

NOTES:

1. Operating voltage is the voltage to which the component is designed to operate. See [Table 4](#).
2. This rating applies to the V_{CC_{CORE}}, V_{CC₅}, and any input (except as noted below) to the processor.
3. Parameter applies to CMOS, APIC, and TAP bus signal groups only.
4. The electrical and mechanical integrity of the processor edge fingers are specified to last for 50 insertion/extraction cycles.
5. S.E.P. Package Only
6. PPGA Package Only

2.10 Processor DC Specifications

The processor DC specifications in this section are defined for the Intel® Celeron™ processor. See [Section 7.0](#) for signal definitions and [Section 5.0](#) for signal listings.

Most of the signals on the Intel Celeron processor system bus are in the AGTL+ signal group. These signals are specified to be terminated to 1.5 V. The DC specifications for these signals are listed in [Table 5](#).

To allow connection with other devices, the Clock, CMOS, APIC, and TAP signals are designed to interface at non-AGTL+ levels. The DC specifications for these pins are listed in [Table 6](#).

[Table 4](#) through [Table 7](#) list the DC specifications for Intel Celeron processors operating at 66 MHz Intel Celeron processor system bus frequencies. Specifications are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 4. Intel® Celeron™ Processor Voltage and Current Specifications ¹

Symbol	Parameter	Core Freq	Min	Typ	Max	Unit	Notes
VCC _{CORE}	VCC for processor core			2.00		V	2, 3, 4
VREF	AGTL+ input reference voltage		$\frac{2}{3}V_{TT} - 2\%$		$\frac{2}{3}V_{TT} + 2\%$	V	± 2%, 11
VCC _{1.5}	VCC for future VCC _{CMOS}		1.365	1.50	1.635	V	1.5 ± 9%
VCC _{2.5}	VCC for VCC _{CMOS}		2.375	2.5	2.625	V	2.5 ± 5%
VTT	AGTL+ bus termination voltage		1.365	1.50	1.635	V	1.5 ± 9% ⁵
Baseboard Tolerance, Static	Processor core voltage static tolerance level at SC242 pins		-0.070		0.100	V	6
Baseboard Tolerance, Transient	Processor core voltage transient tolerance level at SC242 pins		-0.120		0.120	V	6
VCC _{CORE} Tolerance, Static	Processor core voltage static tolerance level at SC242 edge fingers		-0.085		0.100	V	7
VCC _{CORE} Tolerance, Transient	Processor core voltage transient tolerance level at SC242 edge fingers		-0.140		0.140	V	7
VCC _{CORE} Tolerance, Static	Processor core voltage static tolerance level at PPGA processor pins		-0.089		0.100	V	8
VCC _{CORE} Tolerance, Transient	Processor core voltage transient tolerance level at PPGA processor pins		-0.144		0.144	V	8
ICC _{CORE}	Icc for processor core	266 MHz			8.2	A	9, 10
		300 MHz			9.3		
		300A MHz			9.3		
		333 MHz			10.1		
		366 MHz			11.2		
		400 MHz			12.2		
		433 MHz			12.6		
		500 MHz			14.2		
IVTT	Termination voltage supply current				2.7	A	11
ISGnt	Icc Stop-Grant for processor core	266 MHz			1.12	A	12
		300 MHz			1.15		
		300A MHz			1.15		
		333 MHz			1.18		
		366 MHz			1.21		
		400 MHz			1.25		
		433 MHz			1.30		
		500 MHz			1.43		

Table 4. Intel® Celeron™ Processor Voltage and Current Specifications ¹

Symbol	Parameter	Core Freq	Min	Typ	Max	Unit	Notes
ISLP	I _{CC} Sleep for processor core	266 MHz			0.90	A	
		300 MHz			0.94		
		300A MHz			0.94		
		333 MHz			0.96		
		366 MHz			0.97		
		400 MHz			0.99		
		433 MHz			1.01		
		466 MHz			1.03		
		500 MHz			1.09		
IDSLP	I _{CC} Deep Sleep for processor core				0.80	A	
I _{CC} CMOS	I _{CC} for V _{CC} CMOS				500	mA	
dI _{CC} CORE/dt	Power supply current slew rate				20	A/μs	13, 14, 15
dI _{CC} CORE/dt	Power supply current slew rate				240	A/μs	13, 14, 16
dI _{CC} VTT/dt	Termination current slew rate				8	A/μs	See Table 7, Table 16, Table 17

NOTES:

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- V_{CC}CORE and I_{CC}CORE supply the processor core.
- These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required.
- Use the Typical Voltage specification with the Tolerance specifications to provide correct voltage regulation to the processor.
- V_{TT} must be held to 1.5 V ± 9%. It is recommended that V_{TT} be held to 1.5 V ± 3% while the Intel® Celeron™ processor system bus is idle. This is measured at the processor edge fingers.
- These are the tolerance requirements, across a 20 MHz bandwidth, **at the SC242 connector pin on the bottom side of the baseboard**. The requirements at the SC242 connector pins account for voltage drops (and impedance discontinuities) across the connector, processor edge fingers, and to the processor core. V_{CC}CORE must return to within the static voltage specification within 100 μs after a transient event.
- These are the tolerance requirements, across a 20 MHz bandwidth, **at the processor edge fingers**. The requirements at the processor edge fingers account for voltage drops (and impedance discontinuities) at the processor edge fingers and to the processor core. V_{CC}CORE must return to within the static voltage specification within 100 μs after a transient event.
- These are the tolerance requirements, across a 20 MHz bandwidth, **at the top of the PPGA package**. V_{CC}CORE must return to within the static voltage specification within 100 μs after a transient event.
- Max I_{CC}CORE measurements are measured at V_{CC}CORE max voltage (V_{CC}CORE_TYP + maximum static tolerance), under maximum signal loading conditions.
- Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e., typical) voltage level of V_{CC}CORE (V_{CC}CORE_TYP). In this case, the maximum current level for the regulator, I_{CC}CORE_REG, can be reduced from the specified maximum current I_{CC}CORE_MAX and is calculated by the equation:

$$I_{CC_CORE_REG} = I_{CC_CORE_MAX} \times V_{CC_CORE_TYP} / (V_{CC_CORE_TYP} + V_{CC_CORE_Tolerance, Transient})$$
- The current specified is the current required for a single Intel Celeron processor. A similar amount of current is drawn through the termination resistors on the opposite end of the AGTL+ bus, unless single-ended termination is used (see Section 2.1).
- The current specified is also for AutoHALT state.
- Maximum values are specified by design/characterization at nominal V_{CC}CORE.
- Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
- dI_{CC}/dt specifications are measured and specified at the SC242 connector pins.
- dI_{CC}/dt specifications are measured and specified at the PPGA package's processor pins.

Table 5. AGTL+ Signal Groups DC Specifications ¹

Symbol	Parameter	Min	Max	Unit	Notes
V _{IL}	Input Low Voltage	-0.3	0.82	V	
V _{IH}	Input High Voltage	1.22	V _{TT}	V	2, 3
R _{ON}	Buffer On Resistance		16.67	Ω	8
I _L	Leakage Current for inputs, outputs, and I/O		±100	μA	6, 7

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies and cache sizes.
2. V_{IH} and V_{OH} for the Intel Celeron processor may experience excursions of up to 200 mV above V_{TT} for a single system bus clock. However, input signal drivers must comply with the signal quality specifications in Section 3.0.
3. Minimum and maximum V_{TT} are given in Table 7.
4. Parameter correlated to measurement into a 25 Ω resistor terminated to 1.5 V.
5. I_{OH} for the Intel Celeron processor may experience excursions of up to 12 mA for a single system bus clock.
6. (0 ≤ V_{IN} ≤ 2.0 V +5%).
7. (0 ≤ V_{OUT} ≤ 2.0 V +5%).
8. Refer to the I/O Buffer Models for IV characteristics.

Table 6. Non-AGTL+ Signal Group DC Specifications ¹

Symbol	Parameter	Min	Max	Unit	Notes
V _{IL}	Input Low Voltage	-0.3	0.7	V	
V _{IH}	Input High Voltage	1.7	2.625	V	2.5 V +5% maximum
V _{OL}	Output Low Voltage		0.4	V	2
V _{OH}	Output High Voltage	N/A	2.625	V	All outputs are open-drain to 2.5 V +5%
I _{OL}	Output Low Current	14		mA	
I _L	Leakage Current for Inputs, Outputs, and I/O		±100	μA	3, 4

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Parameter measured at 14 mA (for use with TTL inputs).
3. (0 ≤ V_{IN} ≤ 2.5 V +5%).
4. (0 ≤ V_{OUT} ≤ 2.5 V +5%).

2.11 AGTL+ System Bus Specifications

It is recommended that the AGTL+ bus be routed in a daisy-chain fashion with termination resistors to V_{TT} at each end of the signal trace. These termination resistors are placed electrically between the ends of the signal traces and the V_{TT} voltage supply and generally are chosen to approximate the substrate impedance. The valid high and low levels are determined by the input buffers using a reference voltage called V_{REF}. Single ended termination may be possible if trace lengths are tightly controlled, see the *Intel® 440EX AGPset Design Guide* (Order Number 290637) or the *Intel® Celeron™ Processor (PPGA) with the Intel® 440LX AGPset Design Guide* (Order Number 245088) for more information.

Table 7 below lists the nominal specification for the AGTL+ termination voltage (V_{TT}). The AGTL+ reference voltage (V_{REF}) is generated on the processor substrate (S.E.P. Package only) for the processor core, but should be set to $\frac{2}{3}$ V_{TT} for other AGTL+ logic using a voltage divider on

the motherboard. It is important that the motherboard impedance be specified and held to a $\pm 20\%$ tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled. For more details on AGTL+, see the *Pentium® II Processor Developer's Manual* (Order Number 243502) and AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330).

Table 7. Intel® Celeron™ Processor AGTL+ Bus Specifications ¹

Symbol	Parameter	Min	Typ	Max	Units	Notes
V _{TT}	Bus Termination Voltage	1.365	1.50	1.635	V	1.5 V \pm 9% ²
R _{TT}	Termination Resistor		56		Ω	\pm 5%
V _{REF}	Bus Reference Voltage		$\frac{2}{3}$ V _{TT}		V	\pm 2% ³

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. V_{TT} must be held to 1.5 V \pm 9%; dlCC_{V_{TT}}/dt is specified in [Table 4](#). It is recommended that V_{TT} be held to 1.5 V \pm 3% while the Intel Celeron processor system bus is idle. This is measured at the processor edge fingers.
3. V_{REF} is generated on the processor substrate to be $\frac{2}{3}$ V_{TT} nominally with the S.E.P. package. It must be created on the motherboard for processors in the PPGA package.

2.12 Intel® Celeron™ Processor System Bus AC Specifications

The Intel® Celeron™ processor system bus timings specified in this section are defined at the Intel Celeron processor edge fingers and the processor core pads. Timings specified at the processor edge fingers only apply to the S.E.P. Package and timings given at the processor core pads apply to both the S.E.P. Package and the PPGA package. Unless otherwise specified, timings are tested at the processor core during manufacturing. Timings at the processor edge fingers are specified by design characterization. See [Section 7.0](#) for the Intel Celeron processor signal definitions. **Note that at 66 MHz system bus operation, the Intel Celeron processor timings at the processor edge fingers are identical to the Pentium II processor timings at the edge fingers.** See the *Pentium® II Processor at 233, 266, 300, and 333 MHz* (Order Number 243335) for more detail.

[Table 8](#) through [Table 20](#) list the AC specifications associated with the Intel Celeron processor system bus. These specifications are broken into the following categories: [Table 8](#) through [Table 10](#) contain the system bus clock specifications, [Table 11](#) and [Table 12](#) contain the AGTL+ specifications, [Table 14](#) and [Table 15](#) are the CMOS signal group specifications, [Table 16](#) contains timings for the Reset conditions, [Table 17](#) and [Table 18](#) cover APIC bus timing, and [Table 19](#) and [Table 20](#) cover TAP timing. For each pair of tables, the first table contains timing specifications for measurement or simulation at the processor edge fingers. The second table contains specifications for simulation at the processor core pads.

All Intel Celeron processor system bus AC specifications for the AGTL+ signal group are relative to the rising edge of the BCLK input. All AGTL+ timings are referenced to V_{REF} for both '0' and '1' logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the I/O buffer models provided by Intel. These I/O buffer models, which include package information, are available for the Pentium II processor in Quad format as the *Pentium® II Processor I/O Buffer Models*, Quad XTK Format (Electronic Form). AGTL+ layout guidelines are also available in AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330).

Care should be taken to read all notes associated with a particular timing parameter.

Table 8. Intel® Celeron™ Processor System Bus AC Specifications (Clock) at the Processor Edge Fingers For the S.E.P. Package ^{1, 2, 3}

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency		66.67		MHz		
T1': BCLK Period	15.0			ns	6	4, 5, 6
T1B': SC242 to Core Logic BCLK Offset		0.78		ns	6	Absolute Value ^{7,8}
T2': BCLK Period Stability				± 300ps		See Table 9
T3': BCLK High Time	4.44			ns	6	@>2.0 V ⁶
T4': BCLK Low Time	4.44			ns	6	@<0.5 V ⁶
T5': BCLK Rise Time	0.84		2.31	ns	6	(0.5 V–2.0 V) ^{6, 9}
T6': BCLK Fall Time	0.84		2.31	ns	6	(2.0 V–0.5 V) ^{6, 9}

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 0.70 V at the processor edge fingers. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor edge fingers.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 0.70 V at the processor edge fingers. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor edge fingers.
4. The internal core clock frequency is derived from the Intel Celeron processor system bus clock. The system bus clock to core clock ratio is determined during initialization. [Table 10](#) shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
6. This specification applies to Intel Celeron processors when operating at a system bus frequency of 66 MHz.
7. The BCLK offset time is the absolute difference needed between the BCLK signal arriving at the Intel Celeron processor edge finger at 0.5 V vs. arriving at the core logic at 1.25 V. The positive offset is needed to account for the delay between the SC242 connector and processor core. The positive offset ensures both the processor core and the core logic receive the BCLK edge concurrently.
8. See [Section 3.1](#) for Intel Celeron processor system bus clock signal quality specifications.
9. Not 100% tested. Specified by design characterization as a clock driver requirement.

Table 9. Intel® Celeron™ Processor System Bus AC Specifications (Clock) at the Processor Core Pins For Both S.E.P. and PPGA Packages ^{1, 2, 3}

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency		66.67		MHz		
T1: BCLK Period	15.0			ns	6	4, 5, 6
T2: BCLK Period Stability			± 300	ps	6	6, 8, 9
T3: BCLK High Time	4.94			ns	6	@>2.0 V ⁶
T4: BCLK Low Time	4.94			ns	6	@<0.5 V ⁶
T5: BCLK Rise Time	0.34		1.36	ns	6	(0.5 V–2.0 V) ^{6, 10}
T6: BCLK Fall Time	0.34		1.36	ns	6	(2.0 V–0.5 V) ^{6, 10}

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor core pins.
4. The internal core clock frequency is derived from the Intel Celeron processor system bus clock. The system bus clock to core clock ratio is determined during initialization. [Table 10](#) shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
6. This specification applies to the Intel Celeron processor when operating at a system bus frequency of 66 MHz.
7. See [Section 3.1](#) for Intel Celeron processor system bus clock signal quality specifications.
8. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the **rising edges of adjacent BCLKs crossing 1.25 V at the processor core pin**. The jitter present must be accounted for as a component of BCLK timing skew between devices.
9. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer.
10. Not 100% tested. Specified by design characterization as a clock driver requirement.

Table 10. Valid Intel® Celeron™ Processor System Bus, Core Frequency ^{1, 2}

Core Frequency (MHz)	BCLK Frequency (MHz)	Frequency Multiplier
266	66	4
300	66	4.5
333	66	5
366	66	5.5
400	66	6
433	66	6.5
466	66	7
500	66	7.5

NOTES:

1. Contact your local Intel representative for the latest information on processor frequencies and/or frequency multipliers.
2. While other bus ratios are defined, operation at frequencies other than those listed are not supported.

Table 11. Intel® Celeron™ Processor System Bus AC Specifications (AGTL+ Signal Group) at the Processor Edge Fingers For the S.E.P. Package ^{1, 2, 3, 4}

T# Parameter	Min	Max	Unit	Figure	Notes
T7': AGTL+ Output Valid Delay	1.07	6.37	ns	7	4, 5
T8': AGTL+ Input Setup Time	1.96		ns	8	4, 6, 7, 8
T9': AGTL+ Input Hold Time	1.53		ns	8	4, 9
T10': RESET# Pulse Width	1.00		ms	10	10

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 0.50 V at the processor edge fingers. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor edge fingers.
4. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
5. Valid delay timings for these signals are specified into 50 Ω to 1.5 V and with VREF at 1.0 V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. Specification is for a minimum 0.40 V swing.
9. Specification is for a maximum 1.0 V swing.
10. After VCC_{CORE} and BCLK become stable.

Table 12. Intel® Celeron™ Processor System Bus AC Specifications (AGTL+ Signal Group) at the Processor Core Pins For the S.E.P. Package ^{1, 2, 3, 4}

T# Parameter	Min	Max	Unit	Figure	Notes
T7: AGTL+ Output Valid Delay	0.17	5.16	ns	7	5
T8: AGTL+ Input Setup Time	2.10		ns	8	5, 6, 7, 8
T9: AGTL+ Input Hold Time	0.77		ns	8	9
T10: RESET# Pulse Width	1.00		ms	10	7, 10

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor core pins.
4. This specification applies to the Intel Celeron processor operating with a 66 MHz Intel Celeron processor system bus only.
5. Valid delay timings for these signals are specified into 25 Ω to 1.5 V and with VREF at 1.0 V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. Specification is for a minimum 0.40 V swing.
9. Specification is for a maximum 1.0 V swing.
10. After VCC_{CORE} and BCLK become stable.

Table 13. Processor System Bus AC Specifications (AGTL+ Signal Group) at the Processor Core Pins for the PPGA Package ^{1, 2, 3, 4}

T# Parameter	Min	Max	Unit	Figure	Notes
T7: AGTL+ Output Valid Delay	0.30	4.43	ns		5
T8: AGTL+ Input Setup Time	2.10		ns		5, 6, 7
T9: AGTL+ Input Hold Time	0.85		ns		
T10: RESET# Pulse Width	1.00		ms		7, 8

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor pin. All GTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor pins.
4. This specification applies to the processor operating with a 66 MHz system bus only.
5. Valid delay timings for these signals are specified into 25 Ω to 1.5 V and with VREF at 1.0 V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. After VCC_{CORE} and BCLK become stable.

Table 14. Intel® Celeron™ Processor System Bus AC Specifications (CMOS Signal Group) at the Processor Edge Fingers For S.E.P. Package ^{1, 2, 3, 4}

T# Parameter	Min	Max	Unit	Figure	Notes
T14': CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	7	Active and Inactive states
T14B: LINT[1:0] Input Pulse Width	6		BCLKs	7	5
T15': PWRGOOD Inactive Pulse Width	10		BCLKs	7, 10	6, 7

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 0.50 V at the processor edge fingers. All CMOS signal timings (address bus, data bus, etc.) are referenced at 1.25 V.
4. These signals may be driven asynchronously.
5. This specification only applies when the APIC is enabled and the LINT1 or LINT0 pin is configured as an edge-triggered interrupt with fixed delivery; otherwise, specification T14 applies.

PWRGOOD must remain below V_{IL,max} (Table 5) until all the voltage planes meet the voltage tolerance specifications in Table 4 and BCLK has met the BCLK AC specifications in Table 9 for at least 10 clock cycles. PWRGOOD must rise glitch-free and monotonically to 2.5 V.

6. When driven inactive or after VCC_{CORE} and BCLK become stable.
7. If the BCLK signal meets its AC specification within 150 ns of turning on, then the PWRGOOD inactive pulse width specification (T15) is waived and BCLK may start after PWRGOOD is asserted. PWRGOOD must still remain below V_{IL,max} until all the voltage planes meet the voltage tolerance specifications.

Table 15. Intel® Celeron™ Processor System Bus AC Specifications (CMOS Signal Group) at the Processor Core Pins For Both S.E.P. and PPGA Packages ^{1, 2, 3, 4}

T# Parameter	Min	Max	Unit	Figure	Notes
T14: CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	7	Active and Inactive states
T14B: LINT[1:0] Input Pulse Width (S.E.P.P. Only)	6		BCLKs	7	5
T15: PWRGOOD Inactive Pulse Width	10		BCLKs	7,10	6, 7

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25 V at the processor core pins. All CMOS signal timings (address bus, data bus, etc.) are referenced at 1.25 V.
4. These signals may be driven asynchronously.
5. This specification only applies when the APIC is enabled and the LINT1 or LINT0 pin is configured as an edge-triggered interrupt with fixed delivery; otherwise, specification T14 applies.
6. When driven inactive or after $V_{CC_{CORE}}$ and BCLK become stable.
7. If the BCLK signal meets its AC specification within 150 ns of turning on, then the PWRGOOD inactive pulse width specification (T15) is waived and BCLK may start after PWRGOOD is asserted. PWRGOOD must still remain below $V_{IL,max}$ until all the voltage planes meet the voltage tolerance specifications.

PWRGOOD must remain below $V_{IL,max}$ (Table 5) until all the voltage planes meet the voltage tolerance specifications in Table 4 and BCLK has met the BCLK AC specifications in Table 9 for at least 10 clock cycles. PWRGOOD must rise glitch-free and monotonically to 2.5 V.

Table 16. Intel® Celeron™ Processor System Bus AC Specifications (Reset Conditions) ¹

T# Parameter	Min	Max	Unit	Figure	Notes
T16: Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup Time	4		BCLKs	9	Before deassertion of RESET#
T17: Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold Time	2	20	BCLKs	9	After clock that deasserts RESET#

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.

Table 17. Intel® Celeron™ Processor System Bus AC Specifications (APIC Clock and APIC I/O) at the Processor Edge Fingers For S.E.P. Package ^{1, 2, 3, 4}

T# Parameter	Min	Max	Unit	Figure	Notes
T21': PICCLK Frequency	2.0	33.3	MHz		
T22': PICCLK Period	30.0	500.0	ns	6	
T23': PICCLK High Time	12.0		ns	6	
T24': PICCLK Low Time	12.0		ns	6	
T25': PICCLK Rise Time	0.25	3.0	ns	6	
T26': PICCLK Fall Time	0.25	3.0	ns	6	
T27': PICD[1:0] Setup Time	8.5		ns	8	5
T28': PICD[1:0] Hold Time	3.0		ns	8	5
T29': PICD[1:0] Valid Delay	3.0	12.0	ns	7	5, 6, 7

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 0.7 V at the processor edge fingers. All APIC I/O signal timings are referenced at 1.25 V at the processor edge fingers.
4. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
5. Referenced to PICCLK rising edge.
6. For open drain signals, valid delay is synonymous with float delay.
7. Valid delay timings for these signals are specified to 2.5 V +5%.

Table 18. Intel® Celeron™ Processor System Bus AC Specifications (APIC Clock and APIC I/O) at the Processor Core Pins For S.E.P. and PPGA Packages ^{1, 2, 3, 4}

T# Parameter	Min	Max	Unit	Figure	Notes
T21: PICCLK Frequency	2.0	33.3	MHz		
T22: PICCLK Period	30.0	500.0	ns	6	
T23: PICCLK High Time	11.0		ns	6	@>2.0V
T24: PICCLK Low Time	11.0		ns	6	@<0.5V
T25: PICCLK Rise Time	0.25	3.0	ns	6	(0.5V-2.0V)
T26: PICCLK Fall Time	0.25	3.0	ns	6	(2.0V-0.5V)
T27: PICD[1:0] Setup Time	8.0		ns	8	5
T28: PICD[1:0] Hold Time	2.5		ns	8	5
T29: PICD[1:0] Valid Delay	1.5	10.0	ns	7	5, 6, 7

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 1.25 V at the processor core pins. All APIC I/O signal timings are referenced at 1.25 V at the processor core pins.
4. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
5. Referenced to PICCLK rising edge.
6. For open drain signals, valid delay is synonymous with float delay.
7. Valid delay timings for these signals are specified to 2.5 V +5%.

Table 19. Intel® Celeron™ Processor System Bus AC Specifications (TAP Connection) at the Processor Edge Fingers For S.E.P. Package ^{1, 2, 3}

T# Parameter	Min	Max	Unit	Figure	Notes
T30': TCK Frequency		16.667	MHz		
T31': TCK Period	60.0		ns	6	
T32': TCK High Time	25.0		ns	6	@1.7 V
T33': TCK Low Time	25.0		ns	6	@0.7 V
T34': TCK Rise Time		5.0	ns	6	(0.7 V–1.7 V) ⁴
T35': TCK Fall Time		5.0	ns	6	(1.7 V–0.7 V) ⁴
T36': TRST# Pulse Width	40.0		ns	12	Asynchronous
T37': TDI, TMS Setup Time	5.5		ns	11	5
T38': TDI, TMS Hold Time	14.5		ns	11	5
T39': TDO Valid Delay	2.0	13.5	ns	11	6, 7
T40': TDO Float Delay		28.5	ns	11	6, 7
T41': All Non-Test Outputs Valid Delay	2.0	27.5	ns	11	6, 8, 9
T42': All Non-Test Inputs Setup Time		27.5	ns	11	6, 8, 9
T43': All Non-Test Inputs Setup Time	5.5		ns	11	5, 8, 9
T44': All Non-Test Inputs Hold Time	14.5		ns	11	5, 8, 9

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. All AC timings for the TAP signals are referenced to the TCK rising edge at 0.70 V at the processor edge fingers. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor edge fingers.
3. Not 100% tested. Specified by design characterization.
4. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
5. Referenced to TCK rising edge.
6. Referenced to TCK falling edge.
7. Valid delay timing for this signal is specified to 2.5 V +5%.
8. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to TAP operations.
9. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.

Table 20. Intel® Celeron™ Processor System Bus AC Specifications (TAP Connection) at the Processor Core Pins For Both S.E.P. and PPGA Packages ^{1, 2, 3}

T# Parameter	Min	Max	Unit	Figure	Notes
T30: TCK Frequency		16.667	MHz		
T31: TCK Period	60.0		ns	6	
T32: TCK High Time	25.0		ns	6	@1.7 V ¹⁰
T33: TCK Low Time	25.0		ns	6	@0.7 V ¹⁰
T34: TCK Rise Time		5.0	ns	6	(0.7 V–1.7 V) ^{4, 10}
T35: TCK Fall Time		5.0	ns	6	(1.7 V–0.7 V) ^{4, 10}
T36: TRST# Pulse Width	40.0		ns	12	Asynchronous ¹⁰
T37: TDI, TMS Setup Time	5.0		ns	11	5
T38: TDI, TMS Hold Time	14.0		ns	11	5
T39: TDO Valid Delay	1.0	10.0	ns	11	6, 7
T40: TDO Float Delay		25.0	ns	11	6, 7, 10
T41: All Non-Test Outputs Valid Delay	2.0	25.0	ns	11	6, 8, 9
T42: All Non-Test Inputs Setup Time		25.0	ns	11	6, 8, 9, 10
T43: All Non-Test Inputs Setup Time	5.0		ns	11	5, 8, 9
T44: All Non-Test Inputs Hold Time	13.0		ns	11	5, 8, 9

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. All AC timings for the TAP signals are referenced to the TCK rising edge at 1.25 V at the processor core pins.
All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor core pins.
3. These specifications are tested during manufacturing, unless otherwise noted.
4. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
5. Referenced to TCK rising edge.
6. Referenced to TCK falling edge.
7. Valid delay timing for this signal is specified to 2.5 V +5%.
8. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to TAP operations.
9. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.
10. Not 100% tested. Specified by design characterization.

Note: For Figure 3 through Figure 9, the following apply:

1. Figure 3 through Figure 9 are to be used in conjunction with Table 8 through Table 20.
2. All AC timings for the AGTL+ signals at the processor edge fingers are referenced to the BCLK rising edge at 0.50 V. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor edge fingers.
3. All AC timings for the AGTL+ signals at the processor core pins are referenced to the BCLK rising edge at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.
4. All AC timings for the CMOS signals at the processor edge fingers are referenced to the BCLK rising edge at 0.50 V. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor edge fingers.
5. All AC timings for the APIC I/O signals at the processor edge fingers are referenced to the PICCLK rising edge at 0.7 V. All APIC I/O signal timings are referenced at 1.25 V at the processor edge fingers.
6. All AC timings for the TAP signals at the processor edge fingers are referenced to the TCK rising edge at 0.70 V. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor edge fingers.

Figure 2. BCLK to Core Logic Offset

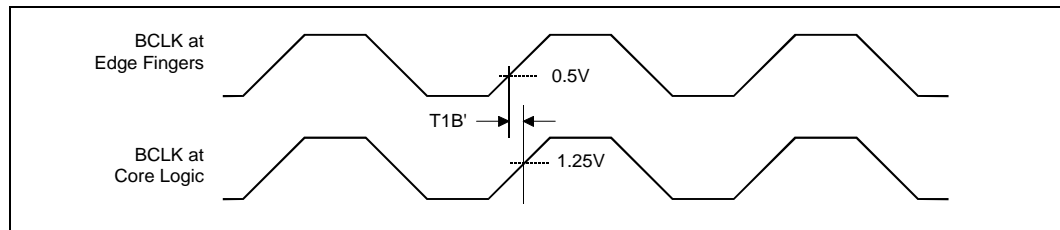


Figure 3. BCLK*, PICCLK, and TCK Generic Clock Waveform

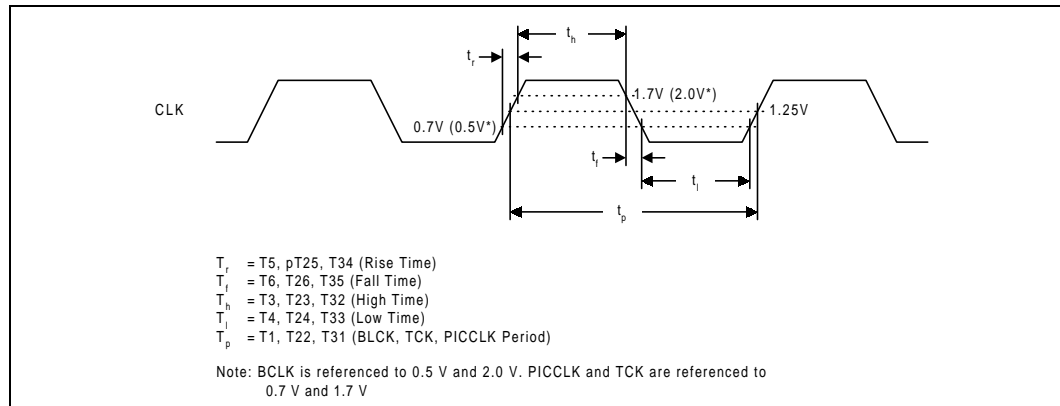


Figure 4. Intel® Celeron™ Processor System Bus Valid Delay Timings

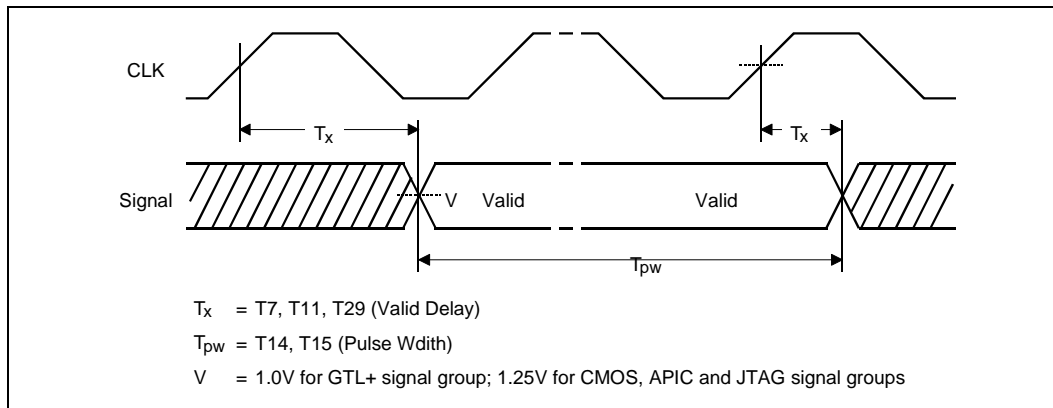


Figure 5. Intel® Celeron™ Processor System Bus Setup and Hold Timings

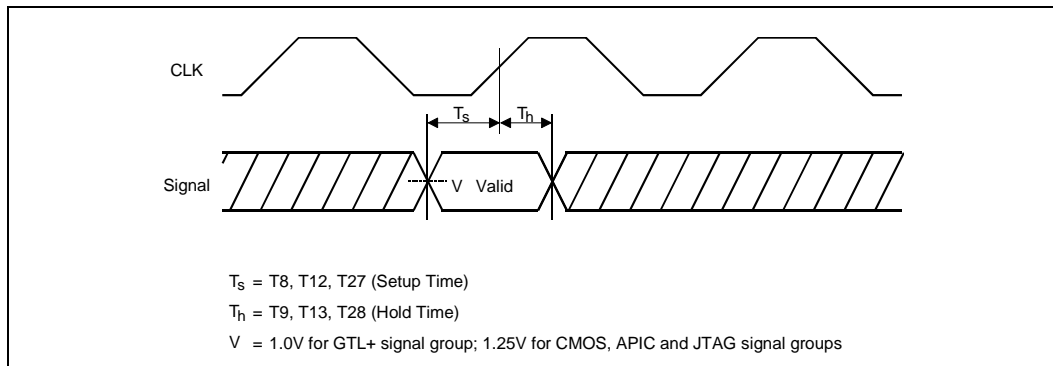


Figure 6. Intel® Celeron™ Processor System Bus Reset and Configuration Timings

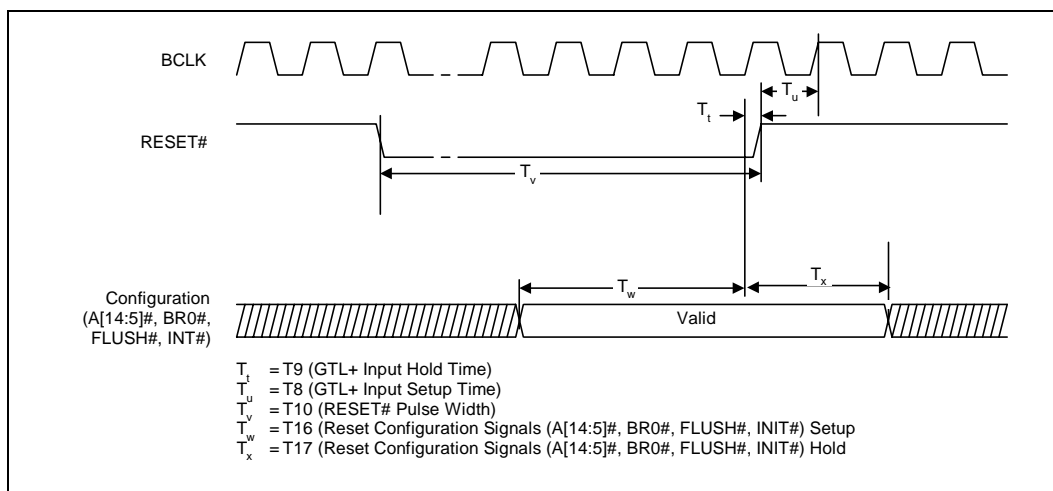


Figure 7. Power-On Reset and Configuration Timings

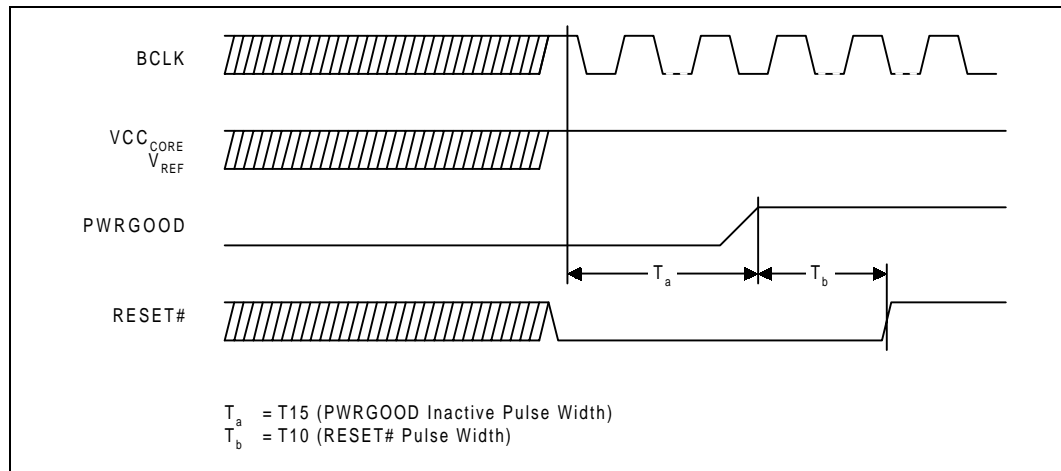


Figure 8. Test Timings (TAP Connection)

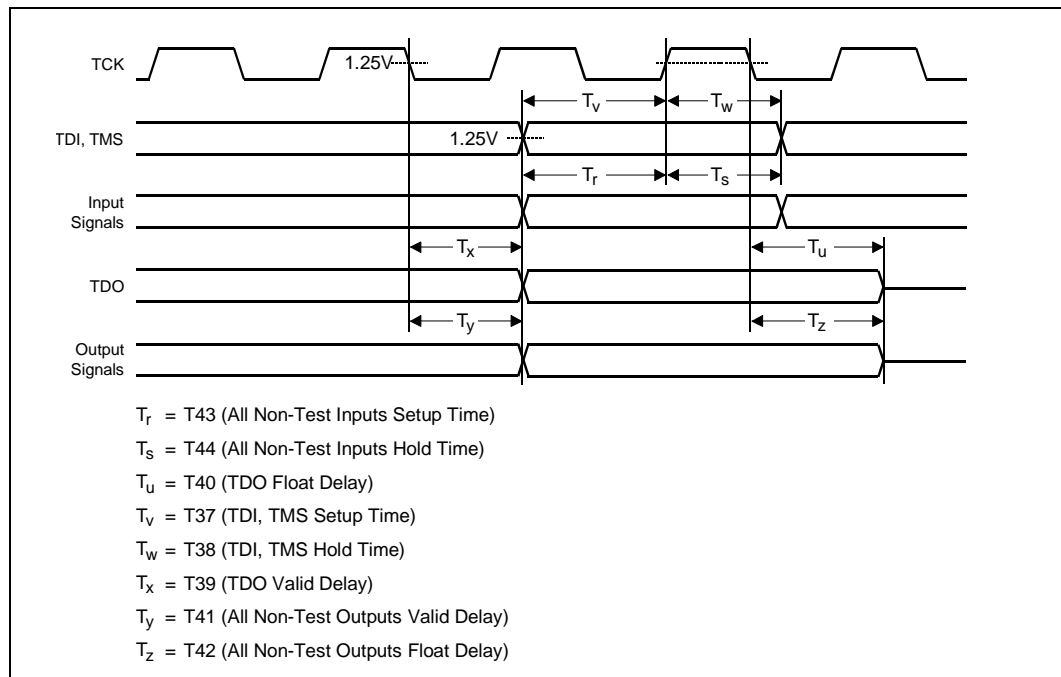
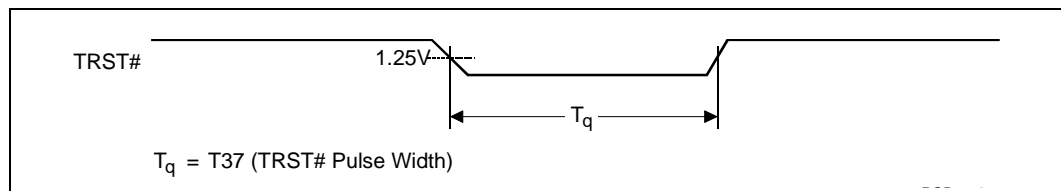


Figure 9. Test Reset Timings



3.0 System Bus Signal Simulations

Signals driven on the Intel® Celeron™ processor system bus should meet signal quality specifications to ensure that the components read data properly and to ensure that incoming signals do not affect the long term reliability of the component. Specifications are provided for simulation at the processor core; guidelines are provided for correlation to the processor edge fingers. These edge finger guidelines are intended for use during testing and measurement of system signal integrity. Violations of these guidelines are permitted, but if they occur, simulation of signal quality at the processor core should be performed to ensure that no violations of signal quality specifications occur. Meeting the specifications at the processor core in [Table 21](#), [Table 23](#), and [Table 25](#) ensures that signal quality effects will not adversely affect processor operation, but does not necessarily guarantee that the guidelines in [Table 22](#), [Table 24](#), and [Table 26](#) will be met.

3.1 Intel® Celeron™ Processor System Bus Clock (BCLK) Signal Quality Specifications and Measurement Guidelines

[Table 21](#) describes the signal quality specifications at the processor core for the Intel® Celeron™ processor system bus clock (BCLK) signal. [Table 22](#) describes guidelines for signal quality measurement at the processor edge fingers. [Figure 10](#) describes the signal quality waveform for the system bus clock at the processor core pins; [Figure 11](#) describes the signal quality waveform for the system bus clock at the processor edge fingers.

Table 21. BCLK Signal Quality Specifications for Simulation at the Processor Core For Both S.E.P. and PPGA Packages ¹

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1: BCLK V _{IL}			0.5	V	14	
V2: BCLK V _{IH}	2.0			V	14	2
V3: V _{IN} Absolute Voltage Range	-0.7		3.5	V	14	2
V4: Rising Edge Ringback	1.7			V	14	3
V5: Falling Edge Ringback			0.7	V	14	3

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. This is the Intel Celeron processor system bus clock overshoot and undershoot specification for 66 MHz system bus operation.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

Figure 10. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Core Pins

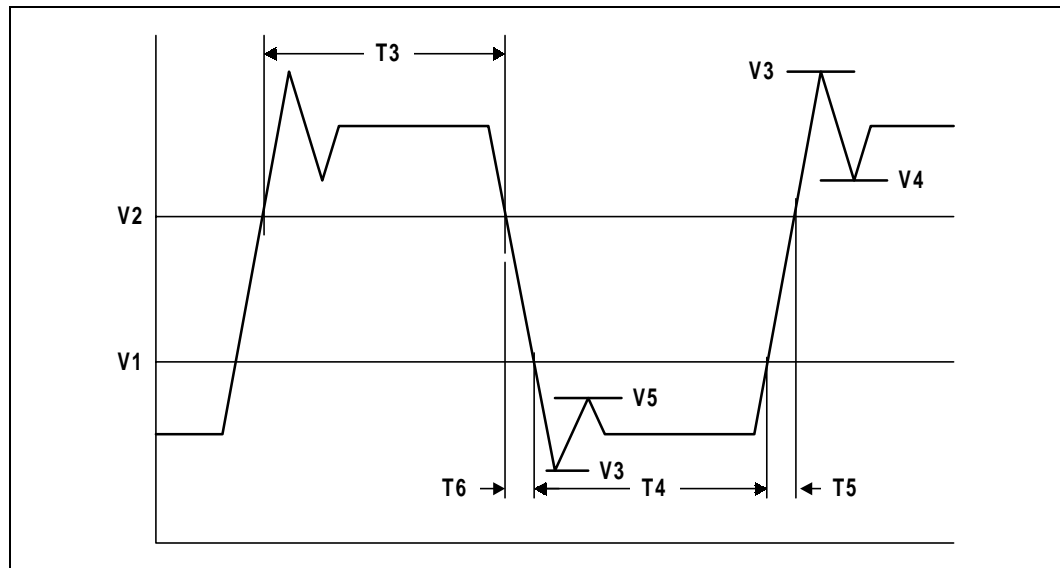


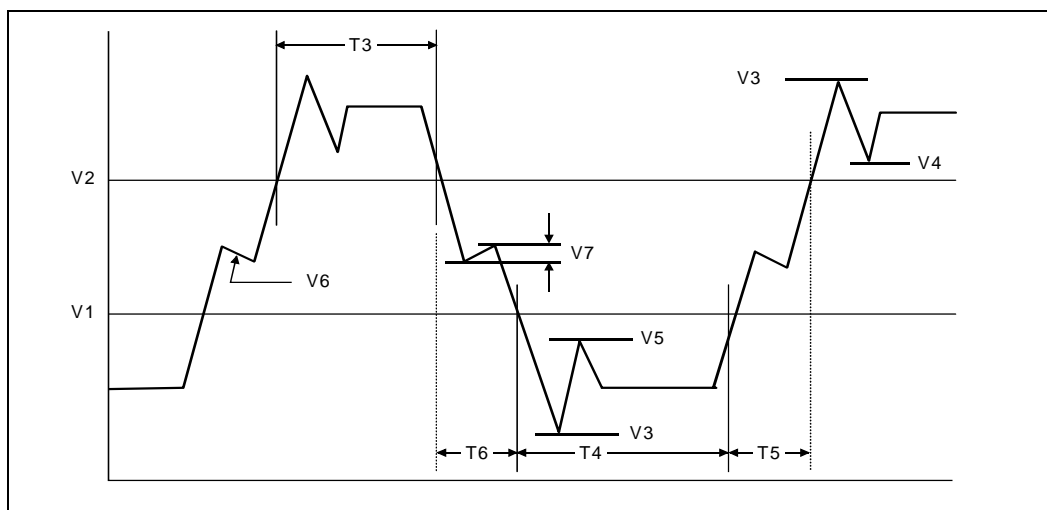
Table 22. BCLK Signal Quality Guidelines for Edge Finger Measurement on the S.E.P. Package¹

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1': BCLK V _{IL}			0.5	V	14	
V2': BCLK V _{IH}	2.0			V	14	
V3': V _{IN} Absolute Voltage Range	-0.5		3.3	V	14	2
V4': Rising Edge Ringback	2.0			V	14	3
V5': Falling Edge Ringback			0.5	V	14	3
V6': T _{line} Ledge Voltage	1.0		1.7	V	14	At Ledge Midpoint ⁴
V7': T _{line} Ledge Oscillation			0.2	V	14	Peak-to-Peak ⁵

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. This is the Intel Celeron processor system bus clock overshoot and undershoot measurement guideline.
3. The rising and falling edge ringback voltage guideline is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal may dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This guideline is an absolute value.
4. The BCLK at the processor edge fingers may have a dip or ledge midway on the rising or falling edge. The midpoint voltage level of this ledge should be within the range of the guideline.
5. The ledge (V7) is allowed to have peak-to-peak oscillation as given in the guideline.

Figure 11. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Edge Fingers



3.2 AGTL+ Signal Quality Specifications and Measurement Guidelines

Many scenarios have been simulated to generate a set of AGTL+ layout guidelines which are available in AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330). Refer to the *Pentium® II Processor Developer's Manual* (Order Number 243502) for the AGTL+ buffer specification.

Table 23 provides the AGTL+ signal quality specifications for Intel® Celeron™ processors for use in simulating signal quality at the processor core. Table 24 provides AGTL+ signal quality guidelines for measuring and testing signal quality at the processor edge fingers. Figure 12 describes the signal quality waveform for AGTL+ signals at the processor core and edge fingers. For more information on the AGTL+ interface, see the *Pentium® II Processor Developer's Manual* (Order Number 243502).

Table 23. AGTL+ Signal Groups Ringback Tolerance Specifications at the Processor Core For Both the S.E.P. and PPGA Packages ^{1, 2, 3}

T# Parameter	Min	Unit	Figure	Notes
α: Overshoot	100	mV	15	4
τ: Minimum Time at High	1.00	ns	15	4
ρ: Amplitude of Ringback	-100	mV	15	4, 5
φ: Final Settling Voltage	100	mV	15	4
δ: Duration of Squarewave Ringback	N/A	ns	15	

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Specifications are for the edge rate of 0.3 - 0.8 V/ns. See Figure 12 for the generic waveform.
3. All values specified by design characterization.
4. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
5. Ringback below VREF + 20 mV is not supported.

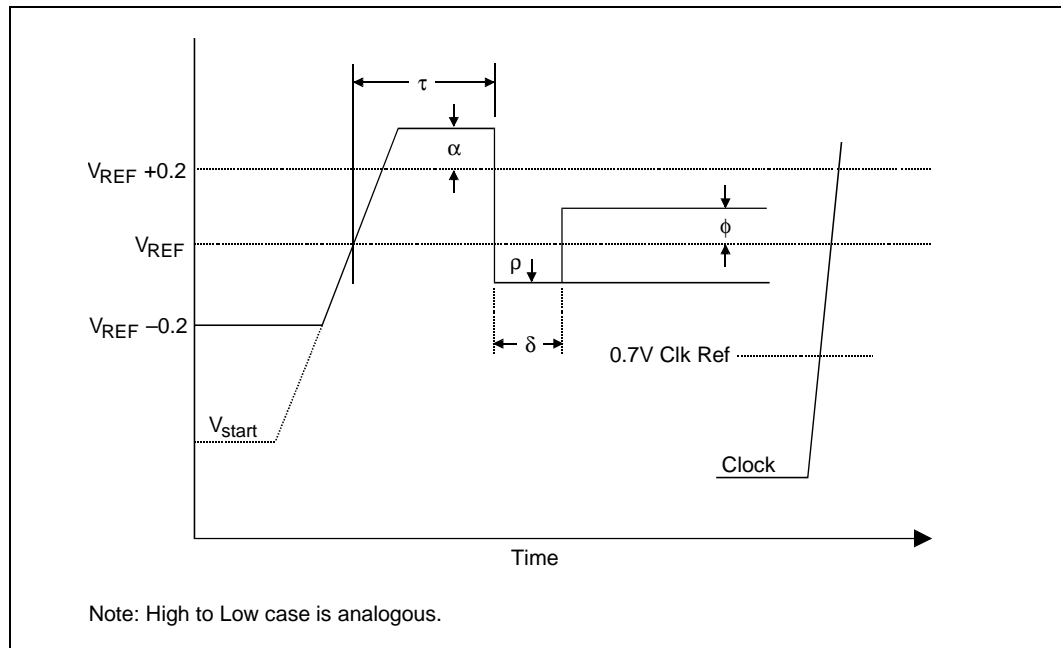
Table 24. AGTL+ Signal Groups Ringback Tolerance Guidelines for Edge Finger Measurement on the S.E.P. Package ^{1, 2, 3}

T# Parameter	Min	Unit	Figure	Notes
α' : Overshoot	100	mV	15	
τ' : Minimum Time at High	1.5	ns	15	4
ρ' : Amplitude of Ringback	-250	mV	15	4, 5
ϕ' : Final Settling Voltage	250	mV	15	4
δ' : Duration of Squarewave Ringback	N/A	ns	15	

NOTES:

1. Unless otherwise noted, all guidelines in this table apply to all Intel® Celeron™ processor frequencies.
2. Guidelines are for the edge rate of 0.3 - 0.8 V/ns. See Figure 12 for the generic waveform.
3. All values specified by design characterization.
4. This guideline applies to Intel Celeron processors operating with a 66 MHz system bus only.
5. Ringback below $V_{REF} + 250$ mV is not supported.

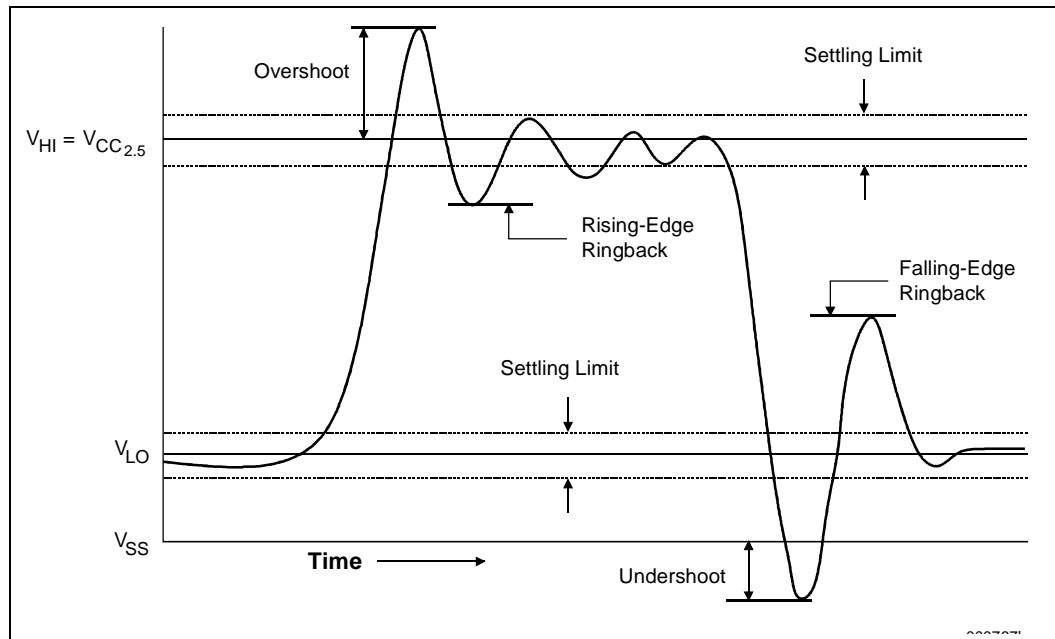
Figure 12. Low to High AGTL+ Receiver Ringback Tolerance



3.3 Non-AGTL+ Signal Quality Specifications and Measurement Guidelines

There are three signal quality parameters defined for non-AGTL+ signals: overshoot/undershoot, ringback, and settling limit. All three signal quality parameters are shown in Figure 13 for the non-AGTL+ signal group.

Figure 13. Non-AGTL+ Overshoot/Undershoot, Settling Limit, and Ringback



3.3.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below V_{SS} . The overshoot/undershoot guideline limits transitions beyond V_{CC} or V_{SS} due to the fast signal edge rates. (See Figure 13 for non-AGTL+ signals.) The processor can be damaged by repeated overshoot events on 2.5 V tolerant buffers if the charge is large enough (i.e., if the overshoot is great enough). However, excessive ringback is the dominant detrimental system timing effect resulting from overshoot/undershoot (i.e., violating the overshoot/undershoot guideline will make satisfying the ringback specification difficult). **The overshoot/undershoot guideline is 0.7 V** and assumes the absence of diodes on the input. These guidelines should be verified in simulations **without the on-chip ESD protection diodes present** because the diodes will begin clamping the 2.5 V tolerant signals beginning at approximately 0.7 V above the 2.5 V supply and 0.7 V below V_{SS} . If signals are not reaching the clamping voltage, this will not be an issue. A system should not rely on the diodes for overshoot/undershoot protection as this will negatively affect the life of the components and make meeting the ringback specification very difficult.

3.3.2 Ringback Specification

Ringback refers to the amount of reflection seen after a signal has switched. The ringback specification is **the voltage that the signal rings back to after achieving its maximum absolute value**. (See Figure 13 for an illustration of ringback.) Excessive ringback can cause false signal detection or extend the propagation delay. The ringback specification applies to the input pin of each receiving agent. Violations of the signal ringback specification are not allowed under any circumstances for non-AGTL+ signals.

Ringback can be simulated with or without the input protection diodes that can be added to the input buffer model. However, signals that reach the clamping voltage should be evaluated further. See Table 25 for the signal ringback specifications for non-AGTL+ signals for simulations at the processor core, and Table 26 for guidelines on measuring ringback at the edge fingers.

Table 25. Signal Ringback Specifications for Non-AGTL+ Signal Simulation at the Processor Core For Both S.E.P. and PPGA Packages ¹

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
Non-AGTL+ Signals	0 → 1	1.7	V	16	
Non-AGTL+ Signals	1 → 0	0.7	V	16	

NOTE:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.

Table 26. Signal Ringback Guidelines for Non-AGTL+ Signal Edge Finger Measurement on the S.E.P. Package ¹

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
Non-AGTL+ Signals	0 → 1	2.0	V	16	
Non-AGTL+ Signals	1 → 0	0.7	V	16	

NOTE:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.

3.3.3 Settling Limit Guideline

Settling limit defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. The amount allowed is 10 percent of the total signal swing ($V_{HI} - V_{LO}$) above and below its final value. A signal should be within the settling limits of its final value, when either in its high state or low state, before it transitions again.

Signals that are not within their settling limit before transitioning are at risk of unwanted oscillations which could jeopardize signal integrity. Simulations to verify settling limit may be done either with or without the input protection diodes present. Violation of the settling limit guideline is acceptable if simulations of 5 to 10 successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions.

4.0 Thermal Specifications and Design Considerations

4.1 Thermal Specifications

Table 27 and Table 28 provide both the Processor Power and Heat Sink Design Target for Intel® Celeron™ processors. Processor Power is defined as the total power dissipated by the processor core and its package. Therefore, the S.E.P. Package's Processor Power would also include power dissipated by the AGTL+ termination resistors. The overall system chassis thermal design must comprehend the entire Processor Power. The Heat Sink Design Target consists of only the processor core, which dissipates the majority of the thermal power.

Systems should design for the highest possible thermal power, even if a processor with a lower thermal dissipation is planned. The processor's heatslug is the attach location for all thermal solutions. The maximum and minimum case temperatures are also specified in Table 27 and Table 28. A thermal solution should be designed to ensure the temperature of the case never exceeds these specifications.

Table 27. Intel® Celeron™ Processor Power for the S.E.P. Package ¹

Processor Core Frequency (MHz)	L2 Cache Size (KB)	Processor Power (W) ²	Heat Sink Design Target (W) ³	Minimum TCASE (°C)	Maximum TCASE (°C)
266	0	16.6	16.0	5	85
300	0	18.4	17.8	5	85
300A	128	18.4	17.8	5	85
333	128	20.2	19.7	5	85
366	128	22.2	21.7	5	85
400	128	24.2	23.7	5	85
433	128	24.6	24.1	5	85

NOTES:

1. These values are specified at nominal V_{CC}CORE for the processor core.
2. Processor Power is power generated from the S.E.P. Package's substrate, which includes the processor core and the AGTL+ termination resistors.
3. Heat Sink Design Target refers to the power consumption of the processor core.

Table 28. Intel® Celeron™ Processor Power for the PPGA Package ^{1,2}

Processor Core Frequency (MHz)	L2 Cache Size (KB)	Processor Power (W)	Heat Sink Design Target (W)	Minimum TCASE (°C)	Maximum TCASE (°C)
300A	128	17.8	17.8	5	85
333	128	19.7	19.7	5	85
366	128	21.7	21.7	5	85
400	128	23.7	23.7	5	85
433	128	24.1	24.1	5	85
466	128	25.6	25.6	5	70
500	128	27.0	27.0	5	70

NOTES:

1. These values are specified at nominal V_{CC}CORE for the processor core.
2. Processor Power and Heat Sink Design Target are the same value because the PPGA package does not have AGTL+ termination resistors.

4.1.1 Thermal Diode

The Intel® Celeron™ Processor incorporates an on-die diode that can be used to monitor the die temperature. A thermal sensor located on the motherboard may monitor the die temperature of the Intel Celeron processor for thermal management purposes. Table 29 and Table 30 provide the diode parameter and interface specifications.

Table 29. Thermal Diode Parameters⁴

Symbol	Min	Typ	Max	Unit	Notes
I _{forward bias}	5		500	uA	1
n_ideality	1.0000	1.0065	1.0173		2,3

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. At room temperature with a forward bias of 630 mV.
3. n_ideality is the diode ideality factor parameter, as represented by the diode equation:

$$I = I_0(e^{(V_d/q)/(nkT)} - 1)$$
4. Not 100% tested. Specified by design characterization.

Table 30. Thermal Diode Interface

Pin Name	SC242 Connector Signal #	370-Pin Socket Pin #	Pin Description
THERMDP	B14	AL31	diode anode (p junction)
THERMDN	B15	AL29	diode cathode (n junction)

4.2 Thermal Parameters

This section defines the terms used for Intel® Celeron™ processor thermal analysis.

4.2.1 Ambient Temperature

Ambient temperature, T_A, is the temperature of the ambient air surrounding the package. The design recommendation of T_A is 45 °C. In a system environment, ambient temperature is the temperature of the air upstream from the package and in its close vicinity; or in an active cooling system, it is the inlet air to the active cooling device.

4.2.2 Thermal Resistance

The thermal resistance value for the case to ambient, Θ_{CA} is used as a measure of the cooling solution's performance. Θ_{CA} is comprised of the case to sink thermal, Θ_{CS} and the sink to ambient thermal resistance, Θ_{SA}. Θ_{CS} is a measure of the thermal resistance along the heat flow path from the top of the heatslug to the bottom of the cooling solution. This value is strongly dependent on the material, conductivity, and thickness of the thermal interface used. Θ_{SA} is a measure of the thermal resistance from the top of the cooling solution to the local ambient air. Θ_{SA} values depend on the material, thermal conductivity, and geometry of the thermal cooling solution as well as on the airflow rates.

4.2.3 Thermal Solution Performance

All processor thermal solutions should attach to the processor's heatslug.

The thermal solution must adequately control the processor's case temperatures below the maximum and above the minimum specified in [Table 27](#). The performance of any thermal solution is defined as the thermal resistance between the case temperature and the ambient air around the processor (Θ_{CA}). The lower the thermal resistance between the case and the ambient air, the more efficient the thermal solution is. The required Θ_{CA} is dependent upon the maximum allowed case temperature (T_{CASE}), the local ambient temperature (T_{LA}) and the maximum power dissipation of the processor.

$$\Theta_{CA} = (T_{CASE} - T_{LA}) / P_D$$

The case temperature and device power is listed in [Table 27](#). T_{LA} is a function of the system design. [Table 31](#) provides an example of the resulting thermal solution performance required for a 266 MHz Intel Celeron processor at different ambient air temperatures around the processor.

Table 31. Example Thermal Solution Performance for 266 MHz Intel® Celeron™ Processor at Power of 16.6 Watts

	Local Ambient Temperature (T_{LA})		
	35 °C	40 °C	45 °C
Θ_{CA} (°C/Watt)	3.01	2.71	2.41

A critical but controllable factor to decrease the value of Θ_{CS} is management of the thermal interface between the case and heat sink. The other controllable factor (Θ_{SA}) is determined by the design of the heat sink and airflow around the heat sink.

4.3 Thermal Solution Attach Methods

It is recommended that the Intel Celeron processor be integrated with an Intel designed heat sink and clip. These components are available from major manufacturers.

5.0 Mechanical Specifications

There are two package technologies which Intel® Celeron™ processors use. They are the S.E.P. Package and the PPGA package. The S.E.P. Package contains the processor core and passive components, while the PPGA package does not have passive components.

The processor edge connector defined in this document is referred to as the “SC242 connector.” See the *SC242 Design Guidelines* (Order Number 243397) for further details on the edge connector.

The processor socket connector is defined in this document is referred to as the “370-pin socket.” See the *370-Pin Socket (PGA370) Design Guidelines* (Order Number 244410) for further details on the socket.

5.1 S.E.P. Package

This section defines the mechanical specifications and signal definitions for the Intel® Celeron™ processor in the S.E.P. Package.

5.1.1 Materials Information

The Intel® Celeron™ processor requires a retention mechanism. This retention mechanism may require motherboard hole dimensions to be 0.159" diameter holes if low cost plastic fasteners are used to secure the retention mechanisms in place. The larger diameter holes are necessary to provide a robust structural design that can guarantee stringent shock and vibrate testing. If captive nuts are used in place of the plastic fasteners, then either the 0.159" or the 0.140" diameter holes will suffice as long as the corresponding sized attached mount is used.

Figure 14 with substrate dimensions is provided to aid in the design of a heat sink and clip. In Figure 15 all area on the secondary side of the substrate is zoned “keep out”, except for 25 mils around the tooling holes and the top and side edges of the substrate.

Figure 14. Intel® Celeron™ Processor Substrate Dimensions (S.E.P. Package)

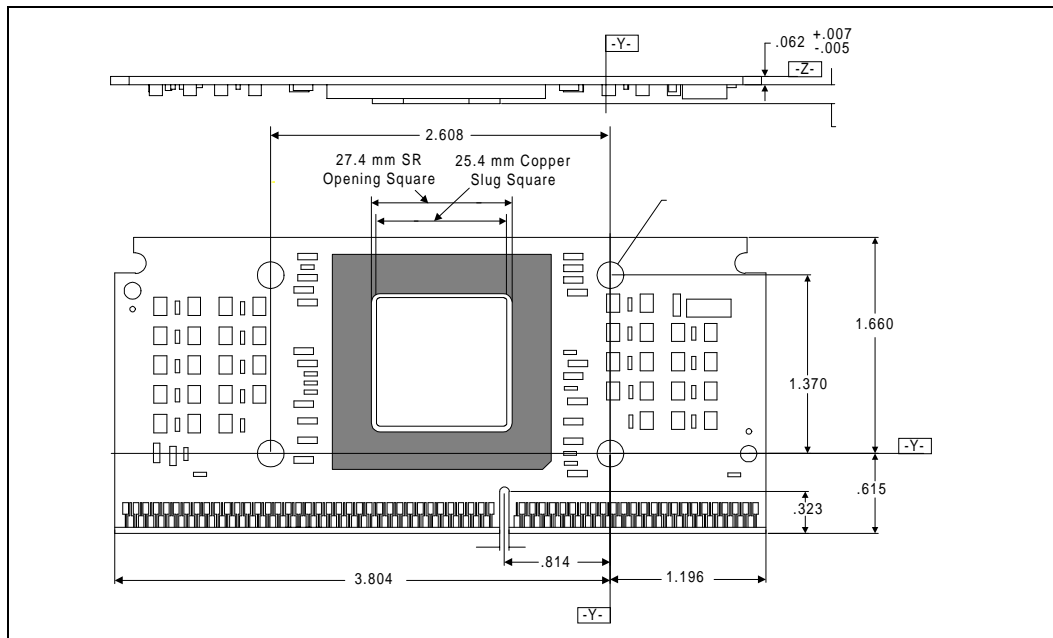
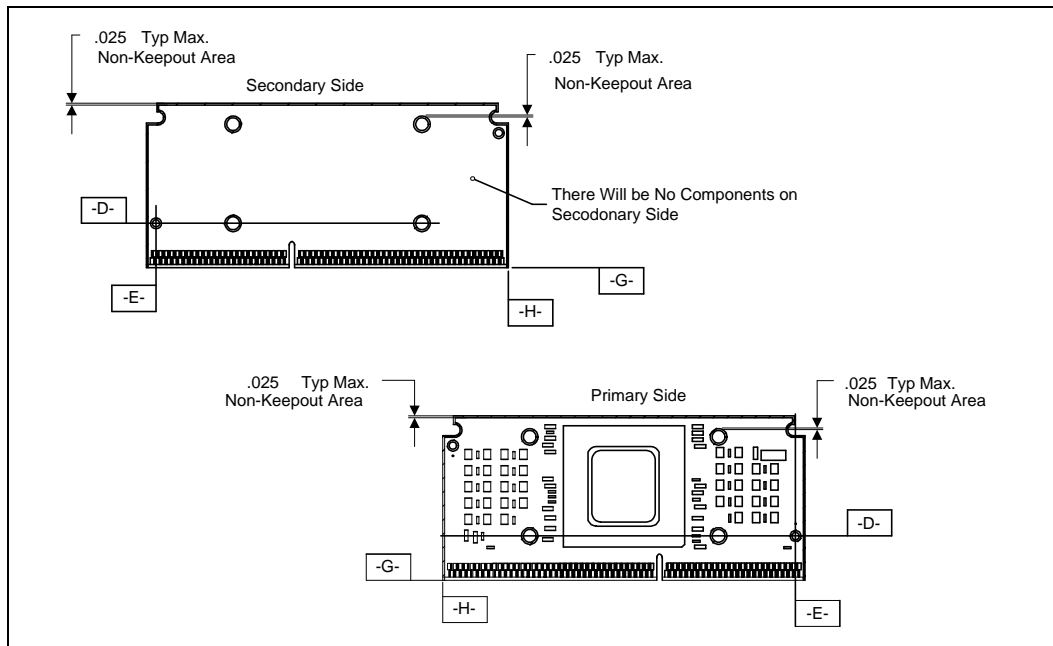


Figure 15. Intel® Celeron™ Processor Substrate Primary/Secondary Side Dimensions (S.E.P. Package)



5.1.2 Signal Listing

Table 32 and Table 33 provide the processor edge finger and SC242 connector signal definitions for Intel® Celeron™ processor. The signal locations on the SC242 edge connector are to be used for signal routing, simulation, and component placement on the motherboard.

Table 32. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
A1	VTT	Power/Other
A2	Vss	Power/Other
A3	VTT	Power/Other
A4	IERR#	CMOS Output
A5	A20M#	CMOS Input
A6	Vss	Power/Other
A7	FERR#	CMOS Output
A8	IGNNE#	CMOS Input
A9	TDI	TAP Input
A10	Vss	Power/Other
A11	TDO	TAP Output
A12	PWRGOOD	CMOS Input
A13	TESTHI	CMOS Test Input
A14	Vss	Power/Other
A15	THERMTRIP#	CMOS Output
A16	Reserved	Reserved for Future Use
A17	LINT0/INTR	CMOS Input
A18	Vss	Power/Other
A19	PICD0	APIC I/O
A20	PREQ#	CMOS Input
A21	BP3#	AGTL+ I/O
A22	Vss	Power/Other
A23	BPM0#	AGTL+ I/O
A24	Reserved	Reserved for Pentium II processor
A25	Reserved	Reserved for Pentium II processor
A26	Vss	Power/Other
A27	Reserved	Reserved for Pentium II processor
A28	Reserved	Reserved for Pentium II processor
A29	Reserved	Reserved for Pentium II processor
A30	Vss	Power/Other
A31	Reserved	Reserved for Pentium II processor
A32	D61#	AGTL+ I/O
A33	D55#	AGTL+ I/O
A34	Vss	Power/Other
A35	D60#	AGTL+ I/O
A36	D53#	AGTL+ I/O

Table 32. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
A37	D57#	AGTL+ I/O
A38	Vss	Power/Other
A39	D46#	AGTL+ I/O
A40	D49#	AGTL+ I/O
A41	D51#	AGTL+ I/O
A42	Vss	Power/Other
A43	D42#	AGTL+ I/O
A44	D45#	AGTL+ I/O
A45	D39#	AGTL+ I/O
A46	Vss	Power/Other
A47	Reserved	Reserved for Future Use
A48	D43#	AGTL+ I/O
A49	D37#	AGTL+ I/O
A50	Vss	Power/Other
A51	D33#	AGTL+ I/O
A52	D35#	AGTL+ I/O
A53	D31#	AGTL+ I/O
A54	Vss	Power/Other
A55	D30#	AGTL+ I/O
A56	D27#	AGTL+ I/O
A57	D24#	AGTL+ I/O
A58	Vss	Power/Other
A59	D23#	AGTL+ I/O
A60	D21#	AGTL+ I/O
A61	D16#	AGTL+ I/O
A62	Vss	Power/Other
A63	D13#	AGTL+ I/O
A64	D11#	AGTL+ I/O
A65	D10#	AGTL+ I/O
A66	Vss	Power/Other
A67	D14#	AGTL+ I/O
A68	D9#	AGTL+ I/O
A69	D8#	AGTL+ I/O
A70	Vss	Power/Other
A71	D5#	AGTL+ I/O
A72	D3#	AGTL+ I/O
A73	D1#	AGTL+ I/O
A74	Vss	Power/Other
A75	BCLK	System Bus Clock Input
A76	Reserved	Reserved for Pentium II processor

Table 32. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
A77	Reserved	Reserved for Pentium II processor
A78	Vss	Power/Other
A79	Reserved	Reserved for Pentium II processor
A80	Reserved	Reserved for Pentium II processor
A81	A30#	AGTL+ I/O
A82	Vss	Power/Other
A83	A31#	AGTL+ I/O
A84	A27#	AGTL+ I/O
A85	A22#	AGTL+ I/O
A86	Vss	Power/Other
A87	A23#	AGTL+ I/O
A88	Reserved	Reserved for Future Use
A89	A19#	AGTL+ I/O
A90	Vss	Power/Other
A91	A18#	AGTL+ I/O
A92	A16#	AGTL+ I/O
A93	A13#	AGTL+ I/O
A94	Vss	Power/Other
A95	A14#	AGTL+ I/O
A96	A10#	AGTL+ I/O
A97	A5#	AGTL+ I/O
A98	Vss	Power/Other
A99	A9#	AGTL+ I/O
A100	A4#	AGTL+ I/O
A101	BNR#	AGTL+ I/O
A102	Vss	Power/Other
A103	BPRI#	AGTL+ Input
A104	TRDY#	AGTL+ Input
A105	DEFER#	AGTL+ Input
A106	Vss	Power/Other
A107	REQ2#	AGTL+ I/O
A108	REQ3#	AGTL+ I/O
A109	HITM#	AGTL+ I/O
A110	Vss	Power/Other
A111	DBSY#	AGTL+ I/O
A112	RS1#	AGTL+ Input
A113	Reserved	Reserved for Future Use
A114	Vss	Power/Other

Table 32. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
A115	ADS#	AGTL+ I/O
A116	Reserved	Reserved for Future Use
A117	Reserved	Reserved for Pentium II processor
A118	Vss	Power/Other
A119	VID2	Power/Other
A120	VID1	Power/Other
A121	VID4	Power/Other
B1	EMI	Power/Other
B2	FLUSH#	CMOS Input
B3	SMI#	CMOS Input
B4	INIT#	CMOS Input
B5	VTT	Power/Other
B6	STPCLK#	CMOS Input
B7	TCK	TAP Input
B8	SLP#	CMOS Input
B9	VTT	Power/Other
B10	TMS	TAP Input
B13	VCC _{CORE}	Power/Other
B14	THERMDP	Power/Other
B15	THERMDN	Power/Other
B16	LINT1/NMI	CMOS Input
B17	VCC _{CORE}	Power/Other
B18	PICCLK	APIC Clock Input
B19	BP2#	AGTL+ I/O
B20	Reserved	Reserved for Future Use
B21	BSEL	Power/Other
B22	PICD1	APIC I/O
B23	PRDY#	AGTL+ Output
B24	BPM1#	AGTL+ I/O
B25	VCC _{CORE}	Power/Other
B26	Reserved	Reserved for Pentium II processor
B27	Reserved	Reserved for Pentium II processor
B28	Reserved	Reserved for Pentium II processor
B29	VCC _{CORE}	Power/Other
B30	D62#	AGTL+ I/O
B31	D58#	AGTL+ I/O
B32	D63#	AGTL+ I/O
B33	VCC _{CORE}	Power/Other

Table 32. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
B34	D56#	AGTL+ I/O
B35	D50#	AGTL+ I/O
B36	D54#	AGTL+ I/O
B37	VCC _{CORE}	Power/Other
B38	D59#	AGTL+ I/O
B39	D48#	AGTL+ I/O
B40	D52#	AGTL+ I/O
B41	EMI	Power/Other
B42	D41#	AGTL+ I/O
B43	D47#	AGTL+ I/O
B44	D44#	AGTL+ I/O
B45	VCC _{CORE}	Power/Other
B46	D36#	AGTL+ I/O
B47	D40#	AGTL+ I/O
B48	D34#	AGTL+ I/O
B49	VCC _{CORE}	Power/Other
B50	D38#	AGTL+ I/O
B51	D32#	AGTL+ I/O
B52	D28#	AGTL+ I/O
B53	VCC _{CORE}	Power/Other
B54	D29#	AGTL+ I/O
B55	D26#	AGTL+ I/O
B56	D25#	AGTL+ I/O
B57	VCC _{CORE}	Power/Other
B58	D22#	AGTL+ I/O
B59	D19#	AGTL+ I/O
B60	D18#	AGTL+ I/O
B61	EMI	Power/Other
B62	D20#	AGTL+ I/O
B63	D17#	AGTL+ I/O
B64	D15#	AGTL+ I/O
B65	VCC _{CORE}	Power/Other
B66	D12#	AGTL+ I/O
B67	D7#	AGTL+ I/O
B68	D6#	AGTL+ I/O
B69	VCC _{CORE}	Power/Other
B70	D4#	AGTL+ I/O
B71	D2#	AGTL+ I/O
B72	D0#	AGTL+ I/O
B73	VCC _{CORE}	Power/Other

Table 32. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
B74	RESET#	AGTL+ Input
B75	Reserved	Reserved for Future Use
B76	Reserved	Reserved for Future Use
B77	VCC _{CORE}	Power/Other
B78	Reserved	Reserved for Pentium II processor
B79	Reserved	Reserved for Pentium II processor
B80	A29#	AGTL+ I/O
B81	EMI	Power/Other
B82	A26#	AGTL+ I/O
B83	A24#	AGTL+ I/O
B84	A28#	AGTL+ I/O
B85	VCC _{CORE}	Power/Other
B86	A20#	AGTL+ I/O
B87	A21#	AGTL+ I/O
B88	A25#	AGTL+ I/O
B89	VCC _{CORE}	Power/Other
B90	A15#	AGTL+ I/O
B91	A17#	AGTL+ I/O
B92	A11#	AGTL+ I/O
B93	VCC _{CORE}	Power/Other
B94	A12#	AGTL+ I/O
B95	A8#	AGTL+ I/O
B96	A7#	AGTL+ I/O
B97	VCC _{CORE}	Power/Other
B98	A3#	AGTL+ I/O
B99	A6#	AGTL+ I/O
B100	EMI	Power/Other
B101	SLOTOCC#	Power/Other
B102	REQ0#	AGTL+ I/O
B103	REQ1#	AGTL+ I/O
B104	REQ4#	AGTL+ I/O
B105	VCC _{CORE}	Power/Other
B106	LOCK#	AGTL+ I/O
B107	DRDY#	AGTL+ I/O
B108	RS0#	AGTL+ Input
B109	VCC ₅	Power/Other
B11	TRST#	TAP Input
B110	HIT#	AGTL+ I/O
B111	RS2#	AGTL+ Input

Table 32. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
B112	Reserved	Reserved for Future Use
B113	VCC _{L2}	Power/Other. Reserved for Pentium II processor
B114	Reserved	Reserved for Pentium II processor
B115	Reserved	Reserved for Pentium II processor
B116	Reserved	Reserved for Pentium II processor

Table 32. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
B117	VCC _{L2}	Power/Other. Reserved for Pentium II processor
B118	Reserved	Reserved for Pentium II processor
B119	VID3	Power/Other
B12	Reserved	Reserved for Future Use
B120	VID0	Power/Other
B121	VCC _{L2}	Power/Other. Reserved for Pentium II processor

Table 33. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
A3#	B98	AGTL+ I/O
A4#	A100	AGTL+ I/O
A5#	A97	AGTL+ I/O
A6#	B99	AGTL+ I/O
A7#	B96	AGTL+ I/O
A8#	B95	AGTL+ I/O
A9#	A99	AGTL+ I/O
A10#	A96	AGTL+ I/O
A11#	B92	AGTL+ I/O
A12#	B94	AGTL+ I/O
A13#	A93	AGTL+ I/O
A14#	A95	AGTL+ I/O
A15#	B90	AGTL+ I/O
A16#	A92	AGTL+ I/O
A17#	B91	AGTL+ I/O
A18#	A91	AGTL+ I/O
A19#	A89	AGTL+ I/O
A20#	B86	AGTL+ I/O
A20M#	A5	CMOS Input
A21#	B87	AGTL+ I/O
A22#	A85	AGTL+ I/O
A23#	A87	AGTL+ I/O
A24#	B83	AGTL+ I/O
A25#	B88	AGTL+ I/O
A26#	B82	AGTL+ I/O
A27#	A84	AGTL+ I/O
A28#	B84	AGTL+ I/O
A29#	B80	AGTL+ I/O
A30#	A81	AGTL+ I/O
A31#	A83	AGTL+ I/O
ADS#	A115	AGTL+ I/O
BCLK	A75	System Bus Clock Input
BNR#	A101	AGTL+ I/O
BP2#	B19	AGTL+ I/O
BP3#	A21	AGTL+ I/O
BPM0#	A23	AGTL+ I/O
BPM1#	B24	AGTL+ I/O

Table 33. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
BPRI#	A103	AGTL+ Input
BSEL	B21	Power/Other
D00#	B72	AGTL+ I/O
D1#	A73	AGTL+ I/O
D2#	B71	AGTL+ I/O
D3#	A72	AGTL+ I/O
D5#	A71	AGTL+ I/O
D6#	B68	AGTL+ I/O
D7#	B67	AGTL+ I/O
D8#	A69	AGTL+ I/O
D9#	A68	AGTL+ I/O
D10#	A65	AGTL+ I/O
D11#	A64	AGTL+ I/O
D12#	B66	AGTL+ I/O
D13#	A63	AGTL+ I/O
D14#	A67	AGTL+ I/O
D15#	B64	AGTL+ I/O
D16#	A61	AGTL+ I/O
D17#	B63	AGTL+ I/O
D18#	B60	AGTL+ I/O
D19#	B59	AGTL+ I/O
D20#	B62	AGTL+ I/O
D21#	A60	AGTL+ I/O
D22#	B58	AGTL+ I/O
D23#	A59	AGTL+ I/O
D24#	A57	AGTL+ I/O
D25#	B56	AGTL+ I/O
D26#	B55	AGTL+ I/O
D27#	A56	AGTL+ I/O
D28#	B52	AGTL+ I/O
D29#	B54	AGTL+ I/O
D30#	A55	AGTL+ I/O
D31#	A53	AGTL+ I/O
D32#	B51	AGTL+ I/O
D33#	A51	AGTL+ I/O
D34#	B48	AGTL+ I/O
D35#	A52	AGTL+ I/O

Table 33. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
D36#	B46	AGTL+ I/O
D37#	A49	AGTL+ I/O
D38#	B50	AGTL+ I/O
D39#	A45	AGTL+ I/O
D4#	B70	AGTL+ I/O
D40#	B47	AGTL+ I/O
D41#	B42	AGTL+ I/O
D42#	A43	AGTL+ I/O
D43#	A48	AGTL+ I/O
D44#	B44	AGTL+ I/O
D45#	A44	AGTL+ I/O
D46#	A39	AGTL+ I/O
D47#	B43	AGTL+ I/O
D48#	B39	AGTL+ I/O
D49#	A40	AGTL+ I/O
D50#	B35	AGTL+ I/O
D51#	A41	AGTL+ I/O
D52#	B40	AGTL+ I/O
D53#	A36	AGTL+ I/O
D54#	B36	AGTL+ I/O
D55#	A33	AGTL+ I/O
D56#	B34	AGTL+ I/O
D57#	A37	AGTL+ I/O
D58#	B31	AGTL+ I/O
D59#	B38	AGTL+ I/O
D60#	A35	AGTL+ I/O
D61#	A32	AGTL+ I/O
D62#	B30	AGTL+ I/O
D63#	B32	AGTL+ I/O
DBSY#	A111	AGTL+ I/O
DEFER#	A105	AGTL+ Input
DRDY#	B107	AGTL+ I/O
EMI	B1	Power/Other
EMI	B41	Power/Other
EMI	B61	Power/Other
EMI	B81	Power/Other
EMI	B100	Power/Other

Table 33. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
FERR#	A7	CMOS Output
FLUSH#	B2	CMOS Input
HIT#	B110	AGTL+ I/O
HITM#	A109	AGTL+ I/O
IERR#	A4	CMOS Output
IGNNE#	A8	CMOS Input
INIT#	B4	CMOS Input
LINT0/INTR	A17	CMOS Input
LINT1/NMI	B16	CMOS Input
LOCK#	B106	AGTL+ I/O
PICCLK	B18	APIC Clock Input
PICD0	A19	APIC I/O
PICD1	B22	APIC I/O
PRDY#	B23	AGTL+ Output
PREQ#	A20	CMOS Input
PWRGOOD	A12	CMOS Input
REQ0#	B102	AGTL+ I/O
REQ1#	B103	AGTL+ I/O
REQ2#	A107	AGTL+ I/O
REQ3#	A108	AGTL+ I/O
REQ4#	B104	AGTL+ I/O
Reserved	A16	Reserved for Future Use
Reserved	A47	Reserved for Future Use
Reserved	A77	Reserved for Pentium II processor
Reserved	A88	Reserved for Future Use
Reserved	A116	Reserved for Future Use
Reserved	B12	Reserved for Future Use
Reserved	A113	Reserved for Future Use
Reserved	B20	Reserved for Future Use
Reserved	B76	Reserved for Future Use
Reserved	B112	Reserved for Future Use
Reserved	B79	Reserved for Pentium II processor
Reserved	B114	Reserved for Pentium II processor
Reserved	B115	Reserved for Pentium II processor

Table 33. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
Reserved	A117	Reserved for Pentium II processor
Reserved	B116	Reserved for Pentium II processor
Reserved	A24	Reserved for Pentium II processor
Reserved	A76	Reserved for Pentium II processor
Reserved	B75	Reserved for Future Use
Reserved	A79	Reserved for Pentium II processor
Reserved	A80	Reserved for Pentium II processor
Reserved	B78	Reserved for Pentium II processor
Reserved	B118	Reserved for Pentium II processor
Reserved	A25	Reserved for Pentium II processor
Reserved	A27	Reserved for Pentium II processor
Reserved	B26	Reserved for Pentium II processor
Reserved	A28	Reserved for Pentium II processor
Reserved	B27	Reserved for Pentium II processor
Reserved	A29	Reserved for Pentium II processor
Reserved	A31	Reserved for Pentium II processor
Reserved	B28	Reserved for Pentium II processor
RESET#	B74	AGTL+ Input
RS0#	B108	AGTL+ Input
RS1#	A112	AGTL+ Input
RS2#	B111	AGTL+ Input
SLOT0CC#	B101	Power/Other
SLP#	B8	CMOS Input
SMI#	B3	CMOS Input
STPCLK#	B6	CMOS Input
TCK	B7	TAP Input
TDI	A9	TAP Input
TDO	A11	TAP Output

Table 33. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
TESTHI	A13	CMOS Test Input
THERMDN	B15	Power/Other
THERMDP	B14	Power/Other
THERMTRIP#	A15	CMOS Output
TMS	B10	TAP Input
TRDY#	A104	AGTL+ Input
TRST#	B11	TAP Input
VCC ₅	B109	Power/Other
VCC _{CORE}	B13	Power/Other
VCC _{CORE}	B17	Power/Other
VCC _{CORE}	B25	Power/Other
VCC _{CORE}	B29	Power/Other
VCC _{CORE}	B33	Power/Other
VCC _{CORE}	B37	Power/Other
VCC _{CORE}	B45	Power/Other
VCC _{CORE}	B49	Power/Other
VCC _{CORE}	B53	Power/Other
VCC _{CORE}	B57	Power/Other
VCC _{CORE}	B65	Power/Other
VCC _{CORE}	B69	Power/Other
VCC _{CORE}	B73	Power/Other
VCC _{CORE}	B77	Power/Other
VCC _{CORE}	B85	Power/Other
VCC _{CORE}	B89	Power/Other
VCC _{CORE}	B93	Power/Other
VCC _{CORE}	B97	Power/Other
VCC _{CORE}	B105	Power/Other
VCC _{L2}	B113	Power/Other. Reserved for Pentium II processor
VCC _{L2}	B117	Power/Other. Reserved for Pentium II processor
VCC _{L2}	B121	Power/Other. Reserved for Pentium II processor
VID0	B120	Power/Other
VID1	A120	Power/Other
VID2	A119	Power/Other
VID3	B119	Power/Other
VID4	A121	Power/Other
Vss	A114	Power/Other

Table 33. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
Vss	A118	Power/Other
Vss	A46	Power/Other
Vss	A38	Power/Other
Vss	A42	Power/Other
Vss	A50	Power/Other
Vss	A54	Power/Other
Vss	A58	Power/Other
Vss	A62	Power/Other
Vss	A66	Power/Other
Vss	A70	Power/Other
Vss	A74	Power/Other
Vss	A78	Power/Other
Vss	A82	Power/Other
Vss	A86	Power/Other
Vss	A2	Power/Other
Vss	A6	Power/Other

Table 33. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
Vss	A10	Power/Other
Vss	A14	Power/Other
Vss	A18	Power/Other
Vss	A22	Power/Other
Vss	A26	Power/Other
Vss	A30	Power/Other
Vss	A34	Power/Other
Vss	A98	Power/Other
Vss	A102	Power/Other
Vss	A106	Power/Other
Vss	A110	Power/Other
VTT	A1	Power/Other
VTT	A3	Power/Other
VTT	B5	Power/Other
VTT	B9	Power/Other

5.2 PPGA Package

This section defines the mechanical specifications and signal definitions for the Intel® Celeron™ processor in the PPGA package.

5.2.1 Materials Information

Figure 16 and Table 34 are provided to aid in the design of a heat sink and clip.

Figure 16. PPGA Package Dimensions

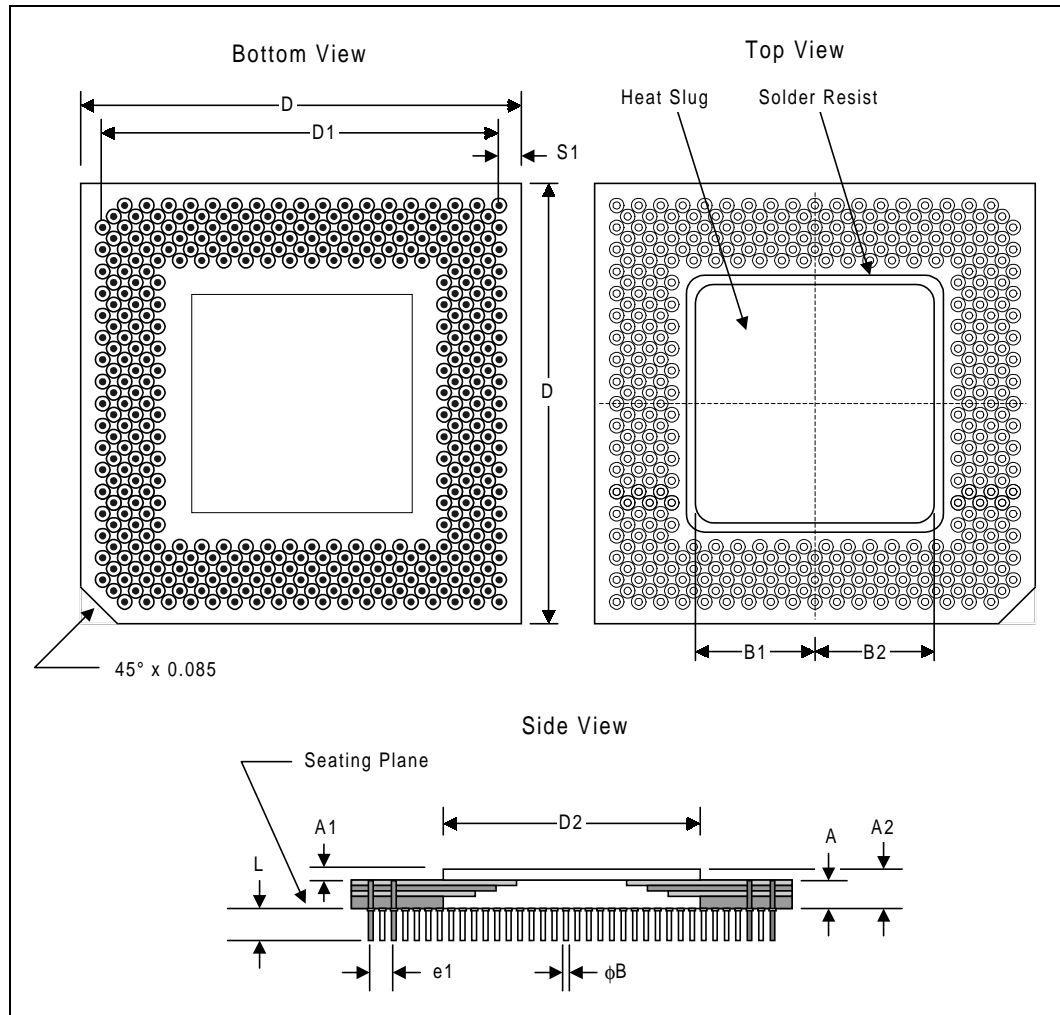


Table 34. PPGA Package Dimensions

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.83	2.23		0.072	0.088	
A ₁	1.00			0.039		
A ₂	2.72	3.33		0.107	0.131	
B	0.40	0.51		0.016	0.020	
D	49.43	49.63		1.946	1.954	
D ₁	45.59	45.85		1.795	1.805	
D ₂	25.15	25.65		0.099	1.010	
e ₁	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	370		Lead Count	370		Lead Count
S ₁	1.52	2.54		0.060	0.100	

Table 35. PPGA Package Information Summary

Package Type	Total Pins	Pin Array	Package Size
Plastic Staggered Pin Grid Array (PPGA)	370	37 x 37	1.95" x 1.95" 4.95 cm x 4.95 cm

5.2.2 Signal Listing

Figure 17. PPGA Package (Pin Side View)

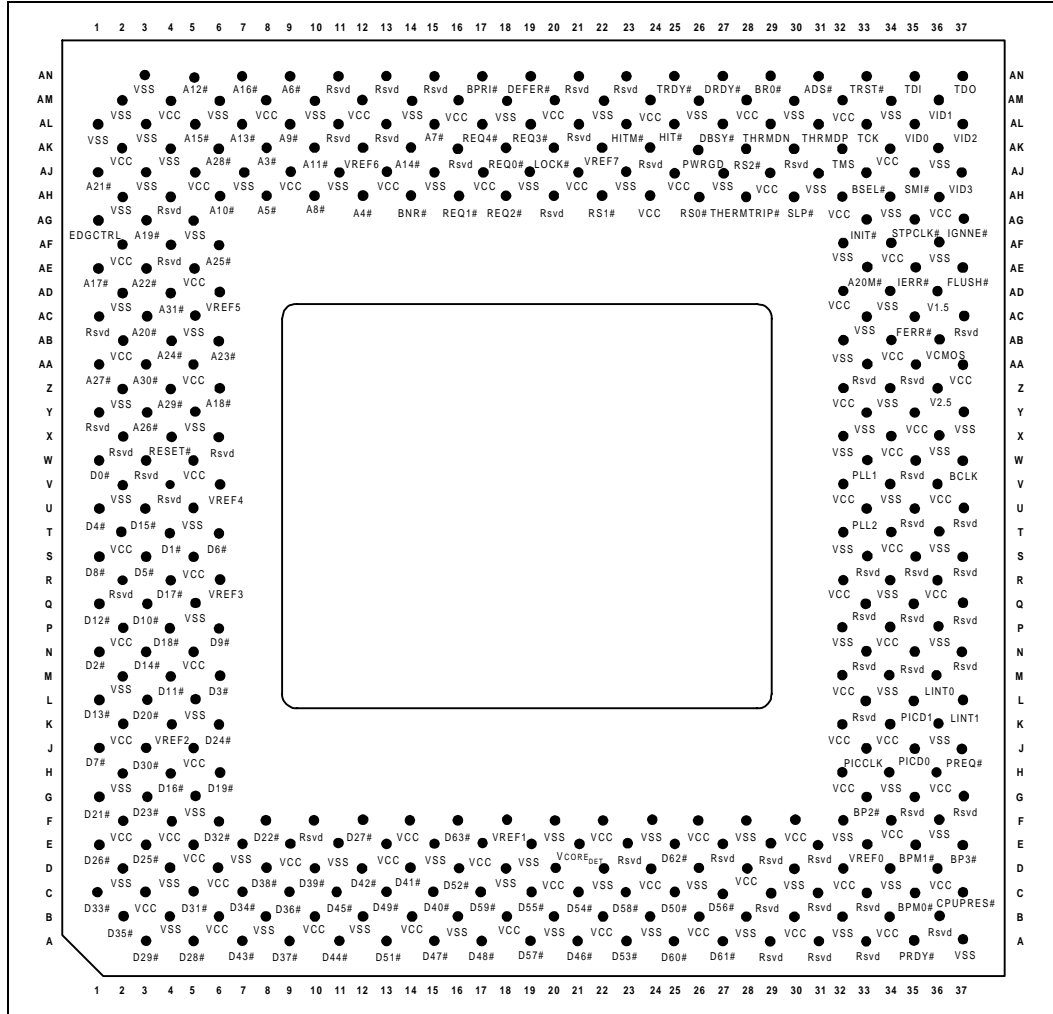


Table 36. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
A3	D29#	AGTL+ I/O
A5	D28#	AGTL+ I/O
A7	D43#	AGTL+ I/O
A9	D37#	AGTL+ I/O
A11	D44#	AGTL+ I/O
A13	D51#	AGTL+ I/O
A15	D47#	AGTL+ I/O
A17	D48#	AGTL+ I/O
A19	D57#	AGTL+ I/O
A21	D46#	AGTL+ I/O
A23	D53#	AGTL+ I/O
A25	D60#	AGTL+ I/O
A27	D61#	AGTL+ I/O
A29	Reserved	Reserved for Future Use
A31	Reserved	Reserved for Future Use
A33	Reserved	Reserved for Future Use
A35	PRDY#	AGTL+ Output
A37	Vss	Power/Other
AA1	A27#	AGTL+ I/O
AA3	A30#	AGTL+ I/O
AA5	VCC _{CORE}	Power/Other
AA33	Reserved	Reserved for Future Use
AA35	Reserved	Reserved for Future Use
AA37	VCC _{CORE}	Power/Other
AB2	VCC _{CORE}	Power/Other
AB4	A24#	AGTL+ I/O
AB6	A23#	AGTL+ I/O
AB32	Vss	Power/Other
AB34	VCC _{CORE}	Power/Other
AB36	VCC _{CMOS}	Power/Other
AC1	Reserved	Reserved for Future Use
AC3	A20#	AGTL+ I/O
AC5	Vss	Power/Other
AC33	Vss	Power/Other
AC35	FERR#	CMOS Output
AC37	Reserved	Reserved for Future Use
AD2	Vss	Power/Other

Table 36. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
AD4	A31#	AGTL+ I/O
AD6	VREF ₅	Power/Other
AD32	VCC _{CORE}	Power/Other
AD34	Vss	Power/Other
AD36	VCC _{1.5}	Power/Other
AE1	A17#	AGTL+ I/O
AE3	A22#	AGTL+ I/O
AE5	VCC _{CORE}	Power/Other
AE33	A20M#	CMOS Input
AE35	IERR#	CMOS Output
AE37	FLUSH#	CMOS Input
AF2	VCC _{CORE}	Power/Other
AF4	Reserved	Reserved for Future Use
AF6	A25#	AGTL+ I/O
AF32	Vss	Power/Other
AF34	VCC _{CORE}	Power/Other
AF36	Vss	Power/Other
AG1	EDGCTRL	Power/Other
AG3	A19#	AGTL+ I/O
AG5	Vss	Power/Other
AG33	INIT#	CMOS Input
AG35	STPCLK#	CMOS Input
AG37	IGNNE#	CMOS Input
AH2	Vss	Power/Other
AH4	Reserved	Reserved for Future Use
AH6	A10#	AGTL+ I/O
AH8	A5#	AGTL+ I/O
AH10	A8#	AGTL+ I/O
AH12	A4#	AGTL+ I/O
AH14	BNR#	AGTL+ I/O
AH16	REQ1#	AGTL+ I/O
AH18	REQ2#	AGTL+ I/O
AH20	Reserved	Reserved for Future Use
AH22	RS1#	AGTL+ Input
AH24	VCC _{CORE}	Power/Other
AH26	RS0#	AGTL+ Input
AH28	THERMTRIP#	CMOS Output

Table 36. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
AH30	SLP#	CMOS Input
AH32	VCC _{CORE}	Power/Other
AH34	Vss	Power/Other
AH36	VCC _{CORE}	Power/Other
AJ01	A21#	AGTL+ I/O
AJ03	Vss	Power/Other
AJ05	VCC _{CORE}	Power/Other
AJ07	Vss	Power/Other
AJ09	VCC _{CORE}	Power/Other
AJ11	Vss	Power/Other
AJ13	VCC _{CORE}	Power/Other
AJ15	Vss	Power/Other
AJ17	VCC _{CORE}	Power/Other
AJ19	Vss	Power/Other
AJ21	VCC _{CORE}	Power/Other
AJ23	Vss	Power/Other
AJ25	VCC _{CORE}	Power/Other
AJ27	Vss	Power/Other
AJ29	VCC _{CORE}	Power/Other
AJ31	Vss	Power/Other
AJ33	BSEL	Power/Other
AJ35	SMI#	CMOS Input
AJ37	VID3	Power/Other
AK02	VCC _{CORE}	Power/Other
AK04	Vss	Power/Other
AK06	A28#	AGTL+ I/O
AK08	A3#	AGTL+ I/O
AK10	A11#	AGTL+ I/O
AK12	VREF ₆	Power/Other
AK14	A14#	AGTL+ I/O
AK16	Reserved	Reserved for Future Use
AK18	REQ0#	AGTL+ I/O
AK20	LOCK#	AGTL+ I/O
AK22	VREF ₇	Power/Other
AK24	Reserved	Reserved for Future Use
AK26	PWRGOOD	CMOS Input
AK28	RS2#	AGTL+ Input
AK30	Reserved	Reserved for Future Use

Table 36. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
AK32	TMS	TAP Input
AK34	VCC _{CORE}	Power/Other
AK36	Vss	Power/Other
AL01	Vss	Power/Other
AL03	Vss	Power/Other
AL05	A15#	AGTL+ I/O
AL07	A13#	AGTL+ I/O
AL09	A9#	AGTL+ I/O
AL11	Reserved	Reserved for Future Use
AL13	Reserved	Reserved for Future Use
AL15	A7#	AGTL+ I/O
AL17	REQ4#	AGTL+ I/O
AL19	REQ3#	AGTL+ I/O
AL21	Reserved	Reserved for Future Use
AL23	HITM#	AGTL+ I/O
AL25	HIT#	AGTL+ I/O
AL27	DBSY#	AGTL+ I/O
AL29	THERMDN	Power/Other
AL31	THERMDP	Power/Other
AL33	TCK	TAP Input
AL35	VID0	Voltage Identification
AL37	VID2	Voltage Identification
AM04	VCC _{CORE}	Power/Other
AM06	Vss	Power/Other
AM08	VCC _{CORE}	Power/Other
AM10	Vss	Power/Other
AM12	VCC _{CORE}	Power/Other
AM14	Vss	Power/Other
AM16	VCC _{CORE}	Power/Other
AM18	Vss	Power/Other
AM2	Vss	Power/Other
AM20	VCC _{CORE}	Power/Other
AM22	Vss	Power/Other
AM24	VCC _{CORE}	Power/Other
AM26	Vss	Power/Other
AM28	VCC _{CORE}	Power/Other
AM30	Vss	Power/Other
AM32	VCC _{CORE}	Power/Other

Table 36. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
AM34	Vss	Power/Other
AM36	VID1	Voltage Identification
AN3	Vss	Power/Other
AN5	A12#	AGTL+ I/O
AN7	A16#	AGTL+ I/O
AN9	A6#	AGTL+ I/O
AN11	Reserved	Reserved for Future Use
AN13	Reserved	Reserved for Future Use
AN15	Reserved	Reserved for Future Use
AN17	BPRI#	AGTL+ Input
AN19	DEFER#	AGTL+ Input
AN21	Reserved	Reserved for Future Use
AN23	Reserved	Reserved for Future Use
AN25	TRDY#	AGTL+ Input
AN27	DRDY#	AGTL+ I/O
AN29	BR0#	AGTL+ I/O
AN31	ADS#	AGTL+ I/O
AN33	TRST#	TAP Input
AN35	TDI	TAP Input
AN37	TDO	TAP Output
B2	D35#	AGTL+ I/O
B4	Vss	Power/Other
B6	VCC _{CORE}	Power/Other
B8	Vss	Power/Other
B10	VCC _{CORE}	Power/Other
B12	Vss	Power/Other
B14	VCC _{CORE}	Power/Other
B16	Vss	Power/Other
B18	VCC _{CORE}	Power/Other
B20	Vss	Power/Other
B22	VCC _{CORE}	Power/Other
B24	Vss	Power/Other
B26	VCC _{CORE}	Power/Other
B28	Vss	Power/Other
B30	VCC _{CORE}	Power/Other
B32	Vss	Power/Other
B34	VCC _{CORE}	Power/Other
B36	Reserved	Reserved for Future Use

Table 36. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
C1	D33#	AGTL+ I/O
C3	VCC _{CORE}	Power/Other
C5	D31#	AGTL+ I/O
C7	D34#	AGTL+ I/O
C9	D36#	AGTL+ I/O
C11	D45#	AGTL+ I/O
C13	D49#	AGTL+ I/O
C15	D40#	AGTL+ I/O
C17	D59#	AGTL+ I/O
C19	D55#	AGTL+ I/O
C21	D54#	AGTL+ I/O
C23	D58#	AGTL+ I/O
C25	D50#	AGTL+ I/O
C27	D56#	AGTL+ I/O
C29	Reserved	Reserved for Future Use
C31	Reserved	Reserved for Future Use
C33	Reserved	Reserved for Future Use
C35	BPM0#	AGTL+ I/O
C37	CPUPRES#	Power/Other
D2	Vss	Power/Other
D4	Vss	Power/Other
D6	VCC _{CORE}	Power/Other
D8	D38#	AGTL+ I/O
D10	D39#	AGTL+ I/O
D12	D42#	AGTL+ I/O
D14	D41#	AGTL+ I/O
D16	D52#	AGTL+ I/O
D18	Vss	Power/Other
D20	VCC _{CORE}	Power/Other
D22	Vss	Power/Other
D24	VCC _{CORE}	Power/Other
D26	Vss	Power/Other
D28	VCC _{CORE}	Power/Other
D30	Vss	Power/Other
D32	VCC _{CORE}	Power/Other
D34	Vss	Power/Other
D36	VCC _{CORE}	Power/Other
E1	D26#	AGTL+ I/O

Table 36. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
E3	D25#	AGTL+ I/O
E5	VCC _{CORE}	Power/Other
E7	Vss	Power/Other
E9	VCC _{CORE}	Power/Other
E11	Vss	Power/Other
E13	VCC _{CORE}	Power/Other
E15	Vss	Power/Other
E17	VCC _{CORE}	Power/Other
E19	Vss	Power/Other
E21	V _{COREDET}	Power/Other
E23	Reserved	Power/Other
E25	D62#	Power/Other
E27	Reserved	Reserved for Future Use
E29	Reserved	Reserved for Future Use
E31	Reserved	Reserved for Future Use
E33	VREF ₀	Power/Other
E35	BPM1#	AGTL+ I/O
E37	BP3#	AGTL+ I/O
F2	VCC _{CORE}	Power/Other
F4	VCC _{CORE}	Power/Other
F6	D32#	AGTL+ I/O
F8	D22#	AGTL+ I/O
F10	Reserved	Reserved for Future Use
F12	D27#	AGTL+ I/O
F14	VCC _{CORE}	Power/Other
F16	D63#	AGTL+ I/O
F18	VREF ₁	Power/Other
F20	Vss	Power/Other
F22	VCC _{CORE}	Power/Other
F24	Vss	Power/Other
F26	VCC _{CORE}	Power/Other
F28	Vss	Power/Other
F30	VCC _{CORE}	Power/Other
F32	Vss	Power/Other
F34	VCC _{CORE}	Power/Other
F36	Vss	Power/Other
G1	D21#	AGTL+ I/O
G3	D23#	AGTL+ I/O

Table 36. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
G5	Vss	Power/Other
G33	BP2#	AGTL+ I/O
G35	Reserved	Reserved for Future Use
G37	Reserved	Reserved for Future Use
H2	Vss	Power/Other
H4	D16#	AGTL+ I/O
H6	D19#	AGTL+ I/O
H32	VCC _{CORE}	Power/Other
H34	Vss	Power/Other
H36	VCC _{CORE}	Power/Other
J1	D7#	AGTL+ I/O
J3	D30#	AGTL+ I/O
J5	VCC _{CORE}	Power/Other
J33	PICCLK	APIC Clock Input
J35	PICD0	APIC I/O
J37	PREQ#	CMOS Input
K2	VCC _{CORE}	Power/Other
K4	VREF ₂	Power/Other
K6	D24#	AGTL+ I/O
K32	VCC _{CORE}	Power/Other
K34	VCC _{CORE}	Power/Other
K36	Vss	Power/Other
L1	D13#	AGTL+ I/O
L3	D20#	AGTL+ I/O
L5	Vss	Power/Other
L33	Reserved	Reserved for Future Use
L35	PICD1	APIC I/O
L37	LINT1/NMI	CMOS Input
M2	Vss	Power/Other
M4	D11#	AGTL+ I/O
M6	D3#	AGTL+ I/O
M32	VCC _{CORE}	Power/Other
M34	Vss	Power/Other
M36	LINT0/INTR	CMOS Input
N1	D2#	AGTL+ I/O
N3	D14#	AGTL+ I/O
N5	VCC _{CORE}	Power/Other
N33	Reserved	Reserved for Future Use

Table 36. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
N35	Reserved	Reserved for Future Use
N37	Reserved	Reserved for Future Use
P2	VCC _{CORE}	Power/Other
P4	D18#	AGTL+ I/O
P6	D9#	AGTL+ I/O
P32	Vss	Power/Other
P34	VCC _{CORE}	Power/Other
P36	Vss	Power/Other
Q1	D12#	AGTL+ I/O
Q3	D10#	AGTL+ I/O
Q5	Vss	Power/Other
Q33	Reserved	Reserved for Future Use
Q35	Reserved	Reserved for Future Use
Q37	Reserved	Reserved for Future Use
R2	Reserved	Reserved for Future Use
R4	D17#	AGTL+ I/O
R6	VREF ₃	Power/Other
R32	VCC _{CORE}	Power/Other
R34	Vss	Power/Other
R36	VCC _{CORE}	Power/Other
S1	D8#	AGTL+ I/O
S3	D5#	AGTL+ I/O
S5	VCC _{CORE}	Power/Other
S33	Reserved	Reserved for Future Use
S35	Reserved	Reserved for Future Use
S37	Reserved	Reserved for Future Use
T2	VCC _{CORE}	Power/Other
T4	D1#	AGTL+ I/O
T6	D6#	AGTL+ I/O
T32	Vss	Power/Other
T34	VCC _{CORE}	Power/Other
T36	Vss	Power/Other
U1	D4#	AGTL+ I/O
U3	D15#	AGTL+ I/O

Table 36. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
U5	Vss	Power/Other
U33	PLL2	Power/Other
U35	Reserved	Reserved for Future Use
U37	Reserved	Reserved for Future Use
V2	Vss	Power/Other
V4	Reserved	Reserved for Future Use
V6	VREF ₄	Power/Other
V32	VCC _{CORE}	Power/Other
V34	Vss	Power/Other
V36	VCC _{CORE}	Power/Other
W1	D0#	AGTL+ I/O
W3	Reserved	Reserved for Future Use
W5	VCC _{CORE}	Power/Other
W33	PLL1	Power/Other
W35	Reserved	Reserved for Future Use
W37	BCLK	System Bus Clock Input
X2	Reserved	Reserved for Future Use
X4	RESET#	AGTL+ Input
X6	Reserved	Reserved for Future Use
X32	Vss	Power/Other
X34	VCC _{CORE}	Power/Other
X36	Vss	Power/Other
Y1	Reserved	Reserved for Future Use
Y3	A26#	AGTL+ I/O
Y5	Vss	Power/Other
Y33	Vss	Power/Other
Y35	VCC _{CORE}	Power/Other
Y37	Vss	Power/Other
Z2	Vss	Power/Other
Z4	A29#	AGTL+ I/O
Z6	A18#	AGTL+ I/O
Z32	VCC _{CORE}	Power/Other
Z34	Vss	Power/Other
Z36	VCC _{2.5}	Power/Other

Table 37. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
A3#	AK8	AGTL+ I/O
A4#	AH12	AGTL+ I/O
A5#	AH8	AGTL+ I/O
A6#	AN9	AGTL+ I/O
A7#	AL15	AGTL+ I/O
A8#	AH10	AGTL+ I/O
A9#	AL9	AGTL+ I/O
A10#	AH6	AGTL+ I/O
A11#	AK10	AGTL+ I/O
A12#	AN5	AGTL+ I/O
A13#	AL7	AGTL+ I/O
A14#	AK14	AGTL+ I/O
A15#	AL5	AGTL+ I/O
A16#	AN7	AGTL+ I/O
A17#	AE1	AGTL+ I/O
A18#	Z6	AGTL+ I/O
A19#	AG3	AGTL+ I/O
A20#	AC3	AGTL+ I/O
A21#	AJ1	AGTL+ I/O
A22#	AE3	AGTL+ I/O
A23#	AB6	AGTL+ I/O
A24#	AB4	AGTL+ I/O
A25#	AF6	AGTL+ I/O
A26#	Y3	AGTL+ I/O
A27#	AA1	AGTL+ I/O
A28#	AK6	AGTL+ I/O
A29#	Z4	AGTL+ I/O
A30#	AA3	AGTL+ I/O
A31#	AD4	AGTL+ I/O
A20M#	AE33	CMOS Input
ADS#	AN31	AGTL+ I/O
BCLK	W37	System Bus Clock Input
BNR#	AH14	AGTL+ I/O
BP2#	G33	AGTL+ I/O
BP3#	E37	AGTL+ I/O
BPM0#	C35	AGTL+ I/O
BPM1#	E35	AGTL+ I/O
BPRI#	AN17	AGTL+ Input
BR0#	AN29	AGTL+ I/O
BSEL	AJ33	Power/Other

Table 37. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
CPUPRES#	C37	Power/Other
D0#	W1	AGTL+ I/O
D1#	T4	AGTL+ I/O
D2#	N1	AGTL+ I/O
D3#	M6	AGTL+ I/O
D4#	U1	AGTL+ I/O
D5#	S3	AGTL+ I/O
D6#	T6	AGTL+ I/O
D7#	J1	AGTL+ I/O
D8#	S1	AGTL+ I/O
D9#	P6	AGTL+ I/O
D10#	Q3	AGTL+ I/O
D11#	M4	AGTL+ I/O
D12#	Q1	AGTL+ I/O
D13#	L1	AGTL+ I/O
D14#	N3	AGTL+ I/O
D15#	U3	AGTL+ I/O
D16#	H4	AGTL+ I/O
D17#	R4	AGTL+ I/O
D18#	P4	AGTL+ I/O
D19#	H6	AGTL+ I/O
D20#	L3	AGTL+ I/O
D21#	G1	AGTL+ I/O
D22#	F8	AGTL+ I/O
D23#	G3	AGTL+ I/O
D24#	K6	AGTL+ I/O
D25#	E3	AGTL+ I/O
D26#	E1	AGTL+ I/O
D27#	F12	AGTL+ I/O
D28#	A5	AGTL+ I/O
D29#	A3	AGTL+ I/O
D30#	J3	AGTL+ I/O
D31#	C5	AGTL+ I/O
D32#	F6	AGTL+ I/O
D33#	C1	AGTL+ I/O
D34#	C7	AGTL+ I/O
D35#	B2	AGTL+ I/O
D36#	C9	AGTL+ I/O
D37#	A9	AGTL+ I/O
D38#	D8	AGTL+ I/O

**Table 37. PPGA Package Signal Listing
in Order by Signal Name**

Pin Name	Pin No.	Signal Buffer Type
D39#	D10	AGTL+ I/O
D40#	C15	AGTL+ I/O
D41#	D14	AGTL+ I/O
D42#	D12	AGTL+ I/O
D43#	A7	AGTL+ I/O
D44#	A11	AGTL+ I/O
D45#	C11	AGTL+ I/O
D46#	A21	AGTL+ I/O
D47#	A15	AGTL+ I/O
D48#	A17	AGTL+ I/O
D49#	C13	AGTL+ I/O
D50#	C25	AGTL+ I/O
D51#	A13	AGTL+ I/O
D52#	D16	AGTL+ I/O
D53#	A23	AGTL+ I/O
D54#	C21	AGTL+ I/O
D55#	C19	AGTL+ I/O
D56#	C27	AGTL+ I/O
D57#	A19	AGTL+ I/O
D58#	C23	AGTL+ I/O
D59#	C17	AGTL+ I/O
D60#	A25	AGTL+ I/O
D61#	A27	AGTL+ I/O
D62#	E25	AGTL+ I/O
D63#	F16	AGTL+ I/O
DBSY#	AL27	AGTL+ I/O
DEFER#	AN19	AGTL+ Input
DRDY#	AN27	AGTL+ I/O
EDGCTRL	AG1	Power/Other
FERR#	AC35	CMOS Output
FLUSH#	AE37	CMOS Input
HIT#	AL25	AGTL+ I/O
HITM#	AL23	AGTL+ I/O
IERR#	AE35	CMOS Output
IGNNE#	AG37	CMOS Input
INIT#	AG33	CMOS Input
LINT0/INTR	M36	CMOS Input
LINT1/NMI	L37	CMOS Input
LOCK#	AK20	AGTL+ I/O
PICCLK	J33	APIC Clock Input

**Table 37. PPGA Package Signal Listing
in Order by Signal Name**

Pin Name	Pin No.	Signal Buffer Type
PICD0	J35	APIC I/O
PICD1	L35	APIC I/O
PLL1	W33	Power/Other
PLL2	U33	Power/Other
PRDY#	A35	AGTL+ Output
PREQ#	J37	CMOS Input
PWRGOOD	AK26	CMOS Input
REQ0#	AK18	AGTL+ I/O
REQ1#	AH16	AGTL+ I/O
REQ2#	AH18	AGTL+ I/O
REQ3#	AL19	AGTL+ I/O
REQ4#	AL17	AGTL+ I/O
Reserved	AC1	Reserved for Future Use
Reserved	AC37	Reserved for Future Use
Reserved	AF4	Reserved for Future Use
Reserved	AK16	Reserved for Future Use
Reserved	AK24	Reserved for Future Use
Reserved	AK30	Reserved for Future Use
Reserved	AL11	Reserved for Future Use
Reserved	AL13	Reserved for Future Use
Reserved	AL21	Reserved for Future Use
Reserved	AN11	Reserved for Future Use
Reserved	AN13	Reserved for Future Use
Reserved	AN15	Reserved for Future Use
Reserved	AN21	Reserved for Future Use
Reserved	AN23	Reserved for Future Use
Reserved	B36	Reserved for Future Use
Reserved	C29	Reserved for Future Use
Reserved	C31	Reserved for Future Use
Reserved	C33	Reserved for Future Use
Reserved	E23	Reserved for Future Use
Reserved	E29	Reserved for Future Use
Reserved	E31	Reserved for Future Use
Reserved	F10	Reserved for Future Use
Reserved	G35	Reserved for Future Use
Reserved	G37	Reserved for Future Use
Reserved	L33	Reserved for Future Use
Reserved	N33	Reserved for Future Use
Reserved	N35	Reserved for Future Use
Reserved	N37	Reserved for Future Use

Table 37. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
Reserved	Q33	Reserved for Future Use
Reserved	Q35	Reserved for Future Use
Reserved	Q37	Reserved for Future Use
Reserved	S33	Reserved for Future Use
Reserved	S37	Reserved for Future Use
Reserved	U35	Reserved for Future Use
Reserved	U37	Reserved for Future Use
Reserved	V4	Reserved for Future Use
Reserved	W3	Reserved for Future Use
Reserved	W35	Reserved for Future Use
Reserved	AH20	Reserved for Future Use
Reserved	AH4	Reserved for Future Use
Reserved	A29	Reserved for Future Use
Reserved	A31	Reserved for Future Use
Reserved	A33	Reserved for Future Use
Reserved	AA33	Reserved for Future Use
Reserved	AA35	Reserved for Future Use
Reserved	X6	Reserved for Future Use
Reserved	Y1	Reserved for Future Use
Reserved	E27	Reserved for Future Use
Reserved	R2	Reserved for Future Use
Reserved	S35	Reserved for Future Use
Reserved	X2	Reserved for Future Use
RESET#	X4	AGTL+ Input
RS0#	AH26	AGTL+ Input
RS1#	AH22	AGTL+ Input
RS2#	AK28	AGTL+ Input
SLP#	AH30	CMOS Input
SMI#	AJ35	CMOS Input
STPCLK#	AG35	CMOS Input
TCK	AL33	TAP Input
TDI	AN35	TAP Input
TDO	AN37	TAP Output
THERMDN	AL29	Power/Other
THERMDP	AL31	Power/Other
THERMTRIP#	AH28	CMOS Output
TMS	AK32	TAP Input
TRDY#	AN25	AGTL+ Input
TRST#	AN33	TAP Input
VCC _{1.5}	AD36	Power/Other

Table 37. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
VCC _{2.5}	Z36	Power/Other
VCC _{CMOS}	AB36	Power/Other
VCC _{CORE}	AJ25	Power/Other
VCC _{CORE}	AJ29	Power/Other
VCC _{CORE}	AJ5	Power/Other
VCC _{CORE}	AJ9	Power/Other
VCC _{CORE}	AK2	Power/Other
VCC _{CORE}	AK34	Power/Other
VCC _{CORE}	AM12	Power/Other
VCC _{CORE}	AM16	Power/Other
VCC _{CORE}	AM20	Power/Other
VCC _{CORE}	AM24	Power/Other
VCC _{CORE}	AM28	Power/Other
VCC _{CORE}	AM32	Power/Other
VCC _{CORE}	AM4	Power/Other
VCC _{CORE}	AM8	Power/Other
VCC _{CORE}	B10	Power/Other
VCC _{CORE}	B14	Power/Other
VCC _{CORE}	B18	Power/Other
VCC _{CORE}	B22	Power/Other
VCC _{CORE}	B26	Power/Other
VCC _{CORE}	B30	Power/Other
VCC _{CORE}	B34	Power/Other
VCC _{CORE}	B6	Power/Other
VCC _{CORE}	C3	Power/Other
VCC _{CORE}	D20	Power/Other
VCC _{CORE}	D24	Power/Other
VCC _{CORE}	D28	Power/Other
VCC _{CORE}	D32	Power/Other
VCC _{CORE}	D36	Power/Other
VCC _{CORE}	D6	Power/Other
VCC _{CORE}	E13	Power/Other
VCC _{CORE}	E17	Power/Other
VCC _{CORE}	E5	Power/Other
VCC _{CORE}	E9	Power/Other
VCC _{CORE}	F14	Power/Other
VCC _{CORE}	F2	Power/Other
VCC _{CORE}	F22	Power/Other
VCC _{CORE}	F26	Power/Other
VCC _{CORE}	AA37	Power/Other

**Table 37. PPGA Package Signal Listing
in Order by Signal Name**

Pin Name	Pin No.	Signal Buffer Type
VCC _{CORE}	AA5	Power/Other
VCC _{CORE}	AB2	Power/Other
VCC _{CORE}	AB34	Power/Other
VCC _{CORE}	AD32	Power/Other
VCC _{CORE}	AE5	Power/Other
VCC _{CORE}	AF2	Power/Other
VCC _{CORE}	AF34	Power/Other
VCC _{CORE}	AH24	Power/Other
VCC _{CORE}	AH32	Power/Other
VCC _{CORE}	AH36	Power/Other
VCC _{CORE}	AJ13	Power/Other
VCC _{CORE}	AJ17	Power/Other
VCC _{CORE}	AJ21	Power/Other
VCC _{CORE}	F30	Power/Other
VCC _{CORE}	F34	Power/Other
VCC _{CORE}	F4	Power/Other
VCC _{CORE}	H32	Power/Other
VCC _{CORE}	H36	Power/Other
VCC _{CORE}	J5	Power/Other
VCC _{CORE}	K2	Power/Other
VCC _{CORE}	K32	Power/Other
VCC _{CORE}	K34	Power/Other
VCC _{CORE}	M32	Power/Other
VCC _{CORE}	N5	Power/Other
VCC _{CORE}	P2	Power/Other
VCC _{CORE}	P34	Power/Other
VCC _{CORE}	R32	Power/Other
VCC _{CORE}	R36	Power/Other
VCC _{CORE}	S5	Power/Other
VCC _{CORE}	T2	Power/Other
VCC _{CORE}	T34	Power/Other
VCC _{CORE}	V32	Power/Other
VCC _{CORE}	V36	Power/Other
VCC _{CORE}	W5	Power/Other
VCC _{CORE}	X34	Power/Other
VCC _{CORE}	Y35	Power/Other
VCC _{CORE}	Z32	Power/Other
V _{CORE_DET}	E21	Power/Other
VID0	AL35	Power/Other
VID1	AM36	Power/Other

**Table 37. PPGA Package Signal Listing
in Order by Signal Name**

Pin Name	Pin No.	Signal Buffer Type
VID2	AL37	Power/Other
VID3	AJ37	Power/Other
VREF ₀	E33	Power/Other
VREF ₁	F18	Power/Other
VREF ₂	K4	Power/Other
VREF ₃	R6	Power/Other
VREF ₄	V6	Power/Other
VREF ₅	AD6	Power/Other
VREF ₆	AK12	Power/Other
VREF ₇	AK22	Power/Other
Vss	B16	Power/Other
Vss	B20	Power/Other
Vss	B24	Power/Other
Vss	B28	Power/Other
Vss	B32	Power/Other
Vss	B4	Power/Other
Vss	B8	Power/Other
Vss	D18	Power/Other
Vss	D2	Power/Other
Vss	D22	Power/Other
Vss	D26	Power/Other
Vss	D30	Power/Other
Vss	D34	Power/Other
Vss	D4	Power/Other
Vss	E11	Power/Other
Vss	E15	Power/Other
Vss	E19	Power/Other
Vss	E7	Power/Other
Vss	F20	Power/Other
Vss	F24	Power/Other
Vss	F28	Power/Other
Vss	F32	Power/Other
Vss	F36	Power/Other
Vss	G5	Power/Other
Vss	H2	Power/Other
Vss	H34	Power/Other
Vss	K36	Power/Other
Vss	L5	Power/Other
Vss	M2	Power/Other
Vss	M34	Power/Other

Table 37. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
Vss	P32	Power/Other
Vss	P36	Power/Other
Vss	Q5	Power/Other
Vss	R34	Power/Other
Vss	T32	Power/Other
Vss	T36	Power/Other
Vss	U5	Power/Other
Vss	V2	Power/Other
Vss	A37	Power/Other
Vss	AB32	Power/Other
Vss	AC33	Power/Other
Vss	AC5	Power/Other
Vss	AD2	Power/Other
Vss	AD34	Power/Other
Vss	AF32	Power/Other
Vss	AF36	Power/Other
Vss	AG5	Power/Other
Vss	AH2	Power/Other
Vss	AH34	Power/Other
Vss	AJ11	Power/Other
Vss	AJ15	Power/Other
Vss	AJ19	Power/Other
Vss	AJ23	Power/Other
Vss	AJ27	Power/Other
Vss	AJ3	Power/Other

Table 37. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
Vss	AJ7	Power/Other
Vss	AK36	Power/Other
Vss	AK4	Power/Other
Vss	AL1	Power/Other
Vss	AL3	Power/Other
Vss	AM10	Power/Other
Vss	AM14	Power/Other
Vss	AM18	Power/Other
Vss	AM2	Power/Other
Vss	AM22	Power/Other
Vss	AM26	Power/Other
Vss	AM30	Power/Other
Vss	AM34	Power/Other
Vss	AM6	Power/Other
Vss	AN3	Power/Other
Vss	B12	Power/Other
Vss	V34	Power/Other
Vss	X32	Power/Other
Vss	X36	Power/Other
Vss	Y37	Power/Other
Vss	Y5	Power/Other
Vss	Z2	Power/Other
Vss	Z34	Power/Other
Vss	AJ31	Power/Other
Vss	Y33	Power/Other

5.3 Heat Sink Volumetric Keepout Zone Guidelines

When designing a system platform it is necessary to ensure sufficient space is left for a heat sink to be installed without mechanical interference. Due to the large number of proprietary heat sink designs, Intel cannot specify a keepout zone that covers all passive and active-fan heat sinks. It is the system designer's responsibility to consider their own proprietary solution when designing the desired keepout zone in their system platform. Please refer to the *Intel® Celeron™ processor (PPGA) at 466 MHz Thermal Solutions Guidelines* (Order Number 245156) for further guidance.

Note: The heat sink keepout zones found in [Section 6.0, “Boxed Processor Specifications” on page 68](#) refer specifically to the Boxed Processor's active-fan heat sink. This does not reflect the worst-case dimensions that may exist with other third party passive or active-fan heat sinks. Contact your vendor of choice for their passive or active-fan heat sink dimensions to ensure that mechanical interference with system platform components does not occur.

6.0 Boxed Processor Specifications

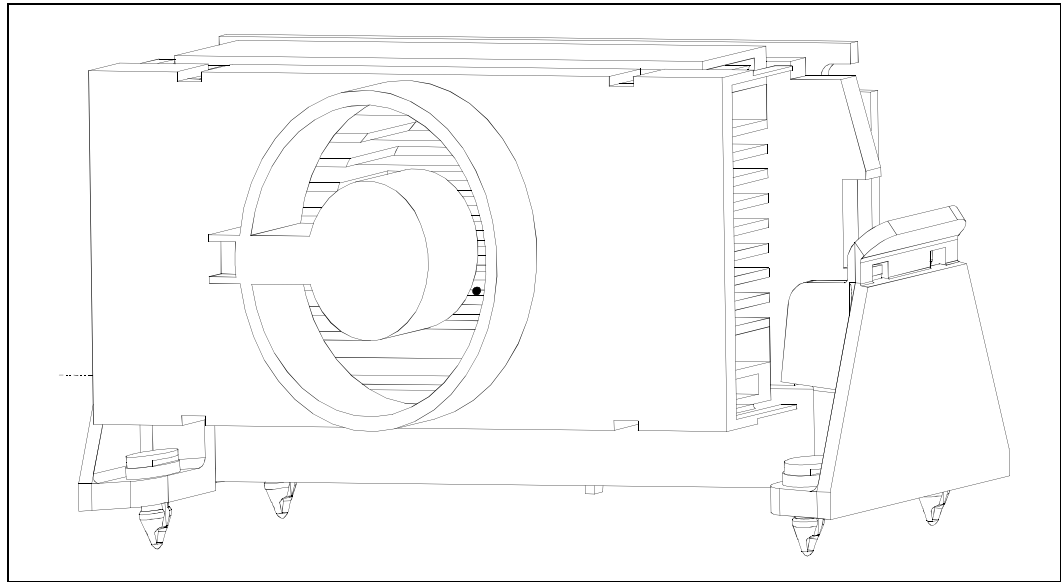
6.1 S.E.P. Package

6.1.1 Introduction

The Intel® Celeron™ processor is also offered as an Intel boxed processor in the S.E.P. Package at the following processor speeds: 400 MHz, 366 MHz, 333 MHz, 300A MHz, 300 MHz, and 266 MHz. Intel boxed processors are intended for system integrators who build systems from motherboards and standard components. The boxed Intel Celeron processor in the S.E.P. Package will be supplied with an attached fan heat sink. This section documents motherboard and system requirements for the fan heat sink that will be supplied with the boxed Intel Celeron processor. This section is particularly important for OEMs that manufacture motherboards for system integrators. Unless otherwise noted, all figures in this section are dimensioned in inches. [Figure 18](#) shows a mechanical representation of the boxed Intel Celeron processor in a S.E.P. Package in the retention mechanism, which is not shipped with the boxed Intel Celeron processor. Note that the airflow of the fan heat sink is into the center and out of the sides of the fan heat sink.

Note: The heat sink keepout zones found in this section refer specifically to the Boxed Processor's active-fan heat sink. This does not reflect the worst-case dimensions that may exist with other third party passive or active-fan heat sinks. Contact your vendor of choice for their passive or active-fan heat sink dimensions to ensure that mechanical interference with system platform components does not occur.

Figure 18. Boxed Intel® Celeron™ Processor in S.E.P. Package in the Retention Mechanism



6.1.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed Intel® Celeron™ processor fan heat sink.

The boxed processor ships with an attached fan heat sink. Clearance is required around the fan heat sink to ensure unimpeded airflow for proper cooling. The space requirements and dimensions for the boxed Processor with integrated fan heat sink are shown in [Figure 19](#), [Figure 20](#), and [Figure 21](#). All dimensions are in inches. Note that these drawings show a conceptual attachment interface to a S.E.P. Package low profile retention mechanism.

Figure 19. Side View Space Requirements for the Boxed Processor

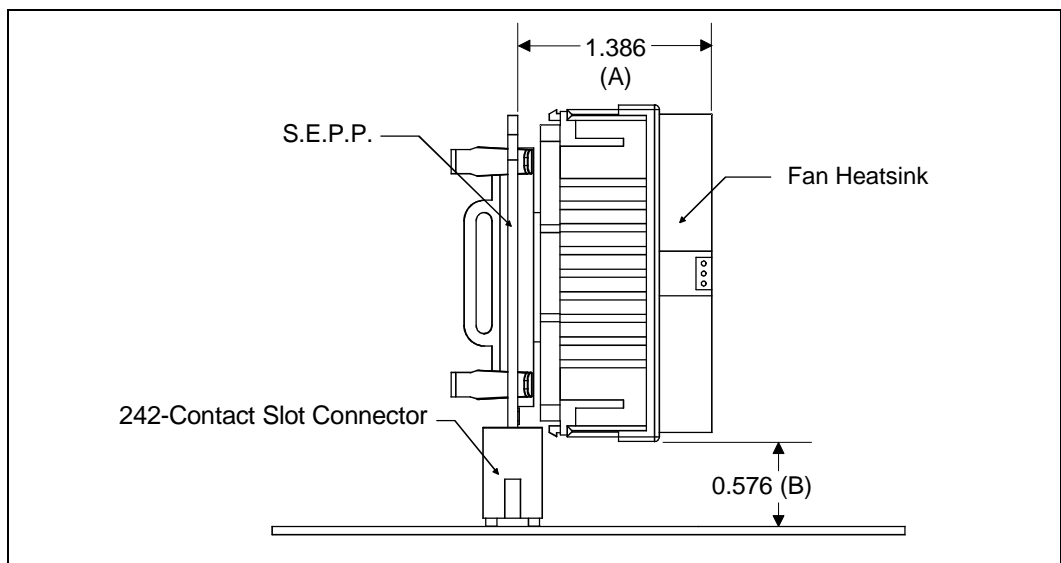


Figure 20. Front View Space Requirements for the Boxed Processor

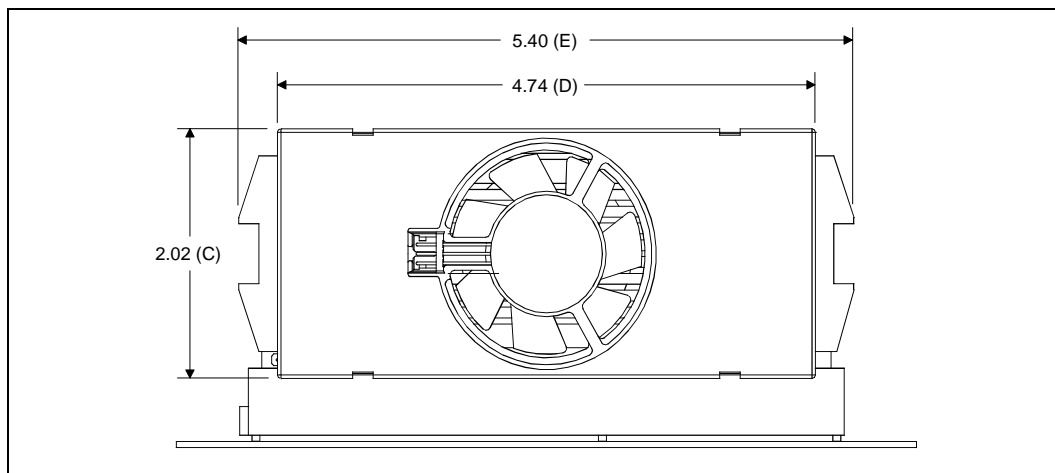
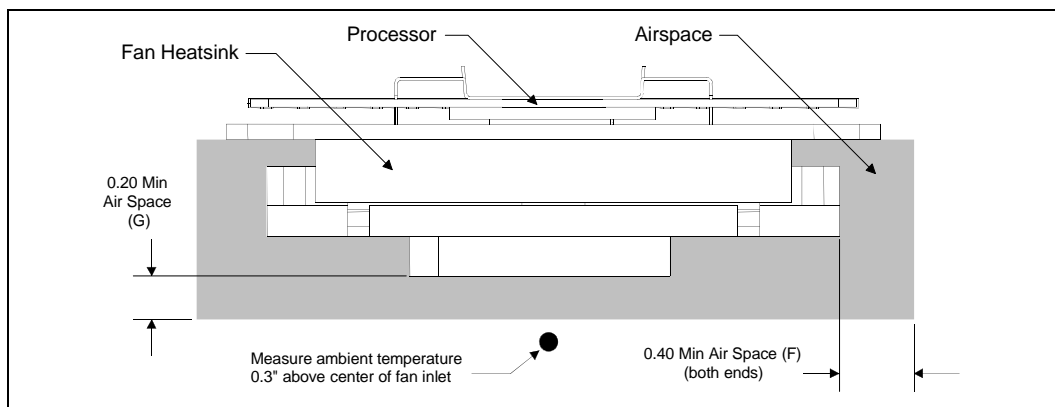


Figure 21. Top View Airspace Requirements for the Boxed Processor



6.1.2.1 Boxed Processor Heat Sink Dimensions

Table 38. Boxed Processor Fan Heat Sink Spatial Dimensions

Fig. Ref. Label	Dimensions (Inches)	Min	Typ	Max
A	Fan Heat Sink Depth (see Figure 19)			1.386
B	Fan Heat Sink Height from Motherboard (see Figure 19)		0.576	
C	Fan Heat Sink Height (see Figure 20)			2.02
D	Fan Heat Sink Width (see Figure 20)			4.74
E	Fan Heat Sink Base Width (see Figure 20)		5.40	
F	Airflow Keepout Zones from end of Fan Heat Sink	0.40		
G	Airflow Keepout Zones from face of Fan Heat Sink	0.20		

NOTE: Drawings reflect only the specifications of the Intel Boxed Processor product. These dimensions should not be used as a universal keepout zone that covers all heat sinks. It is the system designer's responsibility to consider their own proprietary solution when designing the desired keepout zone in their system platform.

6.1.2.2 Boxed Processor Heat Sink Weight

The boxed processor heat sink will not weigh more than 225 grams.

6.1.2.3 Boxed Processor Retention Mechanism

The boxed Intel® Celeron™ processor requires a S.E.P. Package retention mechanism to secure the processor in the SC242 connector. A S.E.P. Package retention mechanism will not be provided with the boxed processor. Motherboards designed for use by system integrators should include a retention mechanism and appropriate installation instructions.

The boxed Intel Celeron processor does not require additional fan heat sink supports. Fan heat sink supports will not be shipped with the boxed Intel Celeron processor.

Motherboards designed for flexible use by system integrators must still recognize the boxed Pentium® II processor's fan heat sink clearance requirements, which are described in the *Pentium® II Processor at 233, 266, 300, and 333 MHz Datasheet* (Order Number 243335).

6.1.3 Boxed Processor Requirements

The boxed processor's fan heat sink requires a +12 V power supply. A fan power cable is shipped with the boxed processor to draw power from a power header on the motherboard. The power cable connector and pin-out are shown in Figure 22. Motherboards must provide a matched power header to support the boxed processor. Table 39 contains specifications for the input and output signals at the fan heat sink connector. The cable length is 7.0 inches (± 0.25"). The fan heat sink outputs a SENSE signal, which is an open-collector output, that pulses at a rate of two pulses per fan revolution. A motherboard pull-up resistor provides VOH to match the motherboard-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The power header on the baseboard must be positioned to allow the fan heat sink power cable to reach it. The power header identification and location should be documented in the motherboard documentation or on the motherboard. Figure 23 shows the recommended location of the fan power connector relative to the SC242 connector. The motherboard power header should be positioned within 4.75 inches (lateral) of the fan power connector.

Figure 22. Boxed Processor Fan Heat Sink Power Cable Connector Description

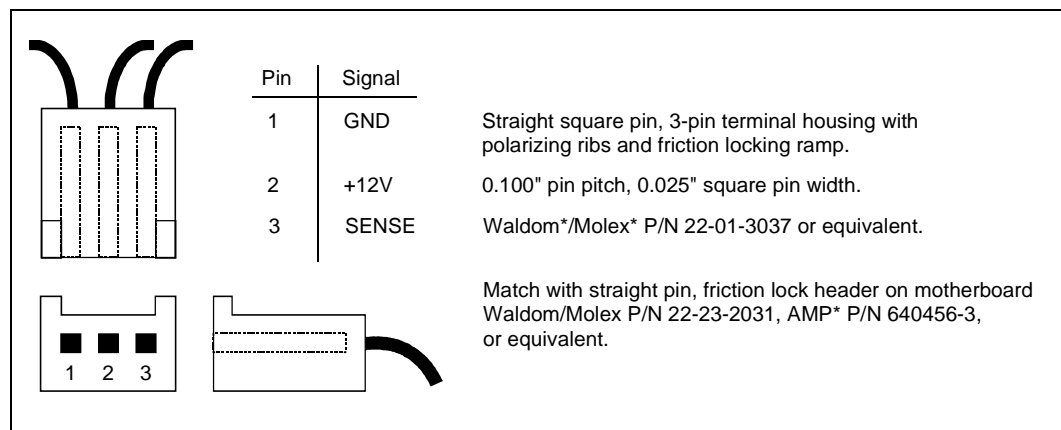
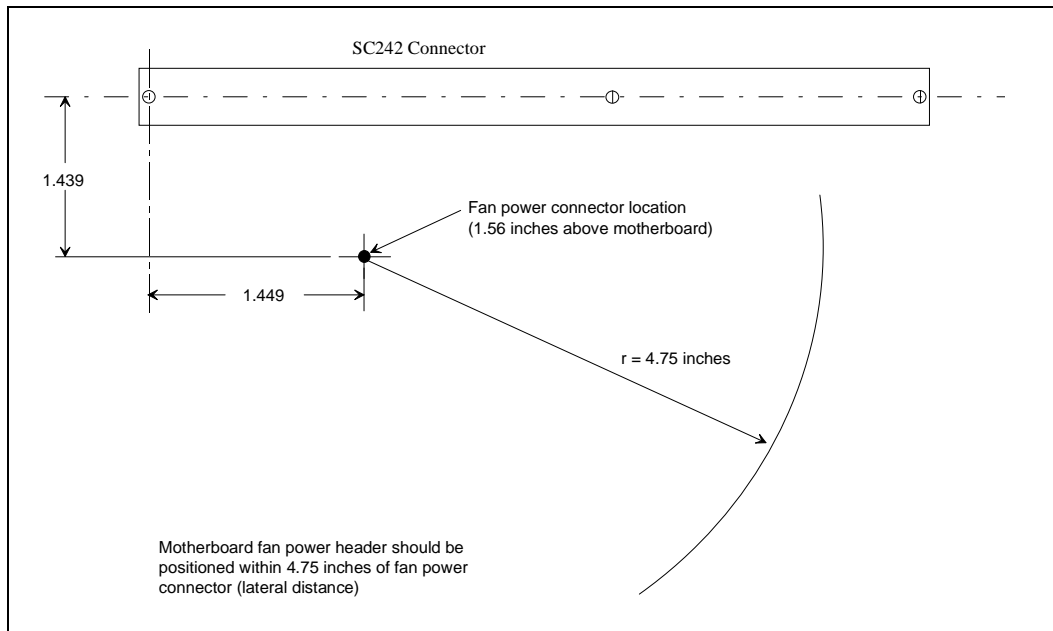


Table 39. Fan Heat Sink Power and Signal Specifications

Description	Min	Typ	Max
+12 V: 12 volt fan power supply	7 V	12 V	13.8 V
IC: Fan current draw			100 mA
SENSE: SENSE frequency (motherboard should pull this pin up to appropriate Vcc with resistor)		2 pulses per fan revolution	

Figure 23. Motherboard Power Header Placement Relative to Fan Power Connector and SC242



6.1.4 Thermal Specifications

This section describes the cooling requirements of the fan heat sink solution utilized by the boxed processor.

6.1.4.1 Boxed Processor Cooling Requirements

The boxed processor is cooled with a fan heat sink. The boxed processor fan heat sink will keep the processor core case temperature, T_{CASE} , within the specifications (see [Table 27](#)), provided airflow through the fan heat sink is unimpeded and the air temperature entering the fan is below 45 °C (see [Figure 21](#) for measurement location).

Airspace is required around the fan to ensure that the airflow through the fan heat sink is not blocked. Blocking the airflow to the fan heat sink reduces the cooling efficiency and decreases fan life. [Figure 21](#) illustrates an acceptable airspace clearance for the fan heat sink.

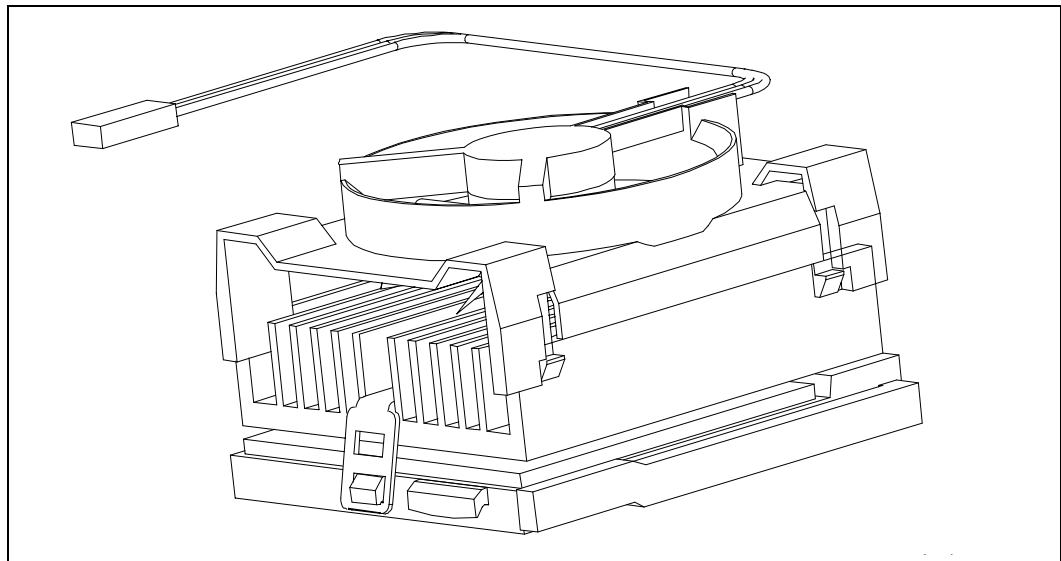
6.2 PPGA Package

6.2.1 Introduction

The Intel® Celeron™ processor is also offered as an Intel boxed processor in the PPGA package at the following processor speeds: 500 MHz, 466 MHz, 433 MHz, 400 MHz, 366 MHz, 333 MHz, and 300A MHz. Intel boxed processors are intended for system integrators who build systems from motherboards and standard components. The boxed Intel Celeron processor in the PPGA package will be supplied with an unattached fan heat sink. This section documents motherboard and system requirements for the fan heat sink that will be supplied with the boxed Intel Celeron processor. This section is particularly important for OEMs that manufacture motherboards for system integrators. Unless otherwise noted, all figures in this section are dimensioned in inches. [Figure 24](#) shows a mechanical representation of the boxed Intel Celeron processor in the PPGA package. Note that the airflow of the fan heat sink is into the center and out of the sides of the fan heat sink.

Note: The heat sink keepout zones found in this section refer specifically to the Boxed Processor's active-fan heat sink. This does not reflect the worst-case dimensions that may exist with other third party passive or active-fan heat sinks. Contact your vendor of choice for their passive or active-fan heat sink dimensions to ensure that mechanical interference with system platform components does not occur.

Figure 24. Boxed Intel® Celeron™ Processor in PPGA Package



6.2.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed Intel® Celeron™ processor fan heat sink.

The boxed processor in the PPGA package ships with an unattached fan heat sink which has an attached integrated clip. Clearance is required around the fan heat sink to ensure unimpeded airflow for proper cooling. The space requirements and dimensions for the boxed Processor with integrated fan heat sink are shown in [Figure 25](#) and [Figure 26](#). All dimensions are in inches.

Figure 25. Side View Space Requirements for the Boxed Processor

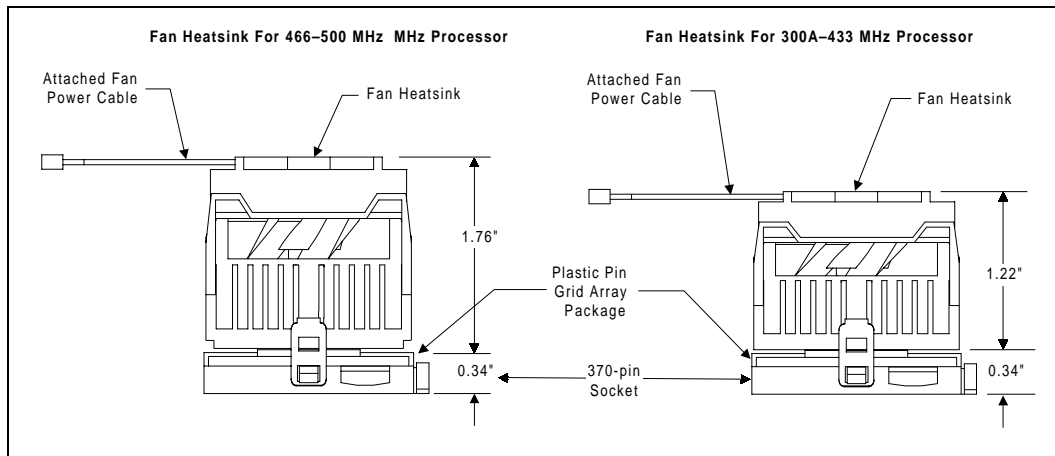


Figure 26. Top View Space Requirements for the Boxed Processor

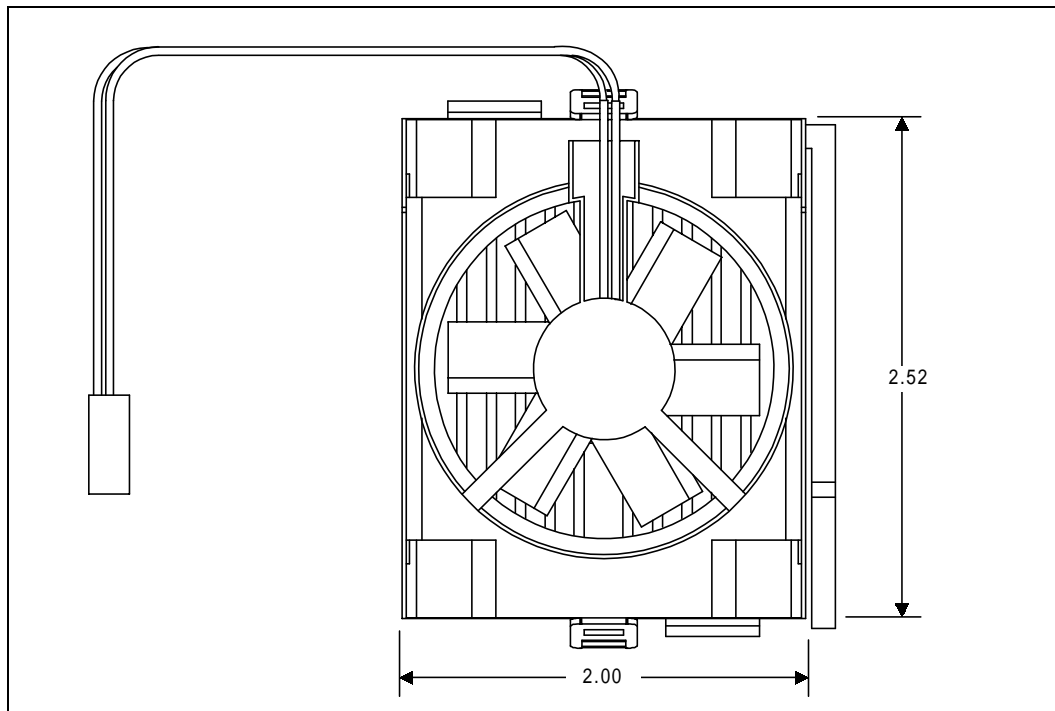
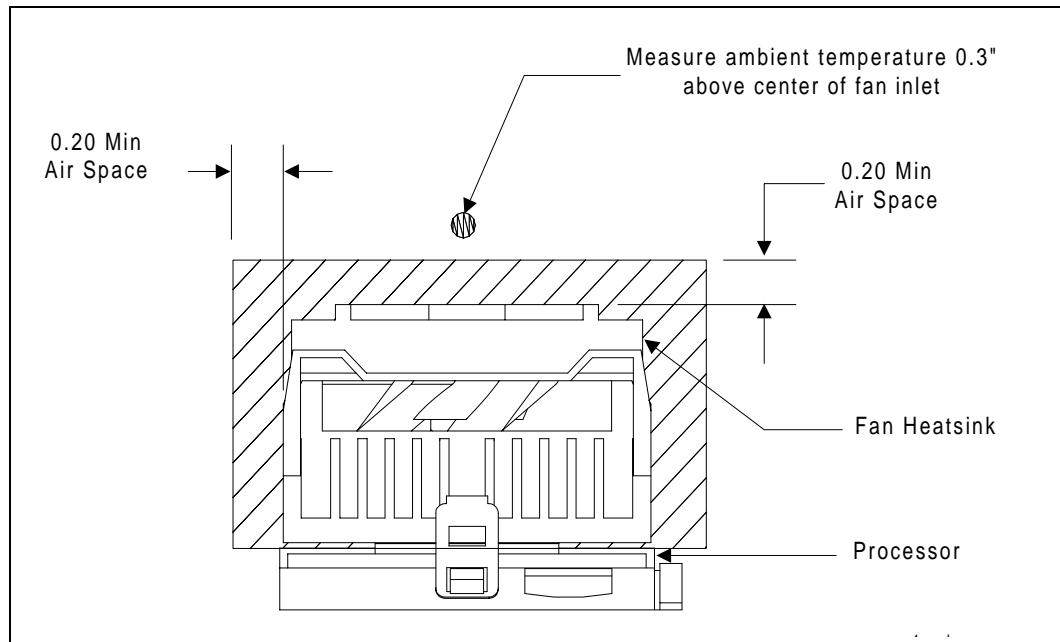


Figure 27. Side View Airspace Requirements for the Boxed Processor



6.2.2.1 Boxed Processor Heat Sink Dimensions

Table 40. Boxed Processor Fan Heat Sink Spatial Dimensions ¹

Dimensions (Inches)	Min	Typ	Max	Notes
Fan Heat Sink Length (see Figure 26)			2.52	
Fan Heat Sink Height from Motherboard (see Figure 25)		0.34		
Fan Heat Sink Height (see Figure 25)			1.22 1.76	2 3
Fan Heat Sink Width (see Figure 26)			2.00	
Airflow Keepout Zones from end of Fan Heat Sink	0.20			
Airflow Keepout Zones from face of Fan Heat Sink	0.20			

NOTES:

1. Drawings reflect only the specifications of the Intel Boxed Processor product. These dimensions should not be used as a universal keepout zone that covers all heat sinks. It is the system designer's responsibility to consider their own proprietary solution when designing the desired keepout zone in their system platform. Please refer to the *Intel® Celeron™ processor (PPGA) at 466 MHz Thermal Solution Guidelines* (Order Number 245156) for further guidance.
2. Specifically applies to the 300A–433 MHz heat sink.
3. Specifically applies to the 466–500 MHz heat sink.

6.2.2.2 Boxed Processor Heat Sink Weight

The boxed processor heat sink will not weigh more than 180 grams.

6.2.2.3 Boxed Processor Thermal Cooling Solution Clip

The boxed processor thermal solution requires installation by a system integrator to secure the thermal cooling solution to the processor after it is installed in the 370-pin socket ZIF socket. Motherboards designed for use by system integrators should take care to consider the implications of clip installation and potential scraping of the motherboard PCB underneath the 370-pin socket attach tabs. Motherboard components should not be placed too close to the 370-pin socket attach tabs in a way that interferes with the installation of the boxed processor thermal cooling solution (see Figure 30 for specification).

6.2.3 Boxed Processor Requirements

The boxed processor's fan heat sink requires a +12 V power supply. A fan power cable is attached to the fan and will draw power from a power header on the motherboard. The power cable connector and pin-out are shown in Figure 28. Motherboards must provide a matched power header to support the boxed processor. Table 41 contains specifications for the input and output signals at the fan heat sink connector. The cable length is 7.0 inches (± 0.25 ”).

The power header on the baseboard must be positioned to allow the fan heat sink power cable to reach it. The power header identification and location should be documented in the motherboard documentation or on the motherboard. Figure 29 shows the recommended location of the fan power connector relative to the 370-pin socket. The motherboard power header should be positioned within 4.00 inches from the center of the 370-pin socket.

Figure 28. Boxed Processor Fan Heat Sink Power Cable Connector Description

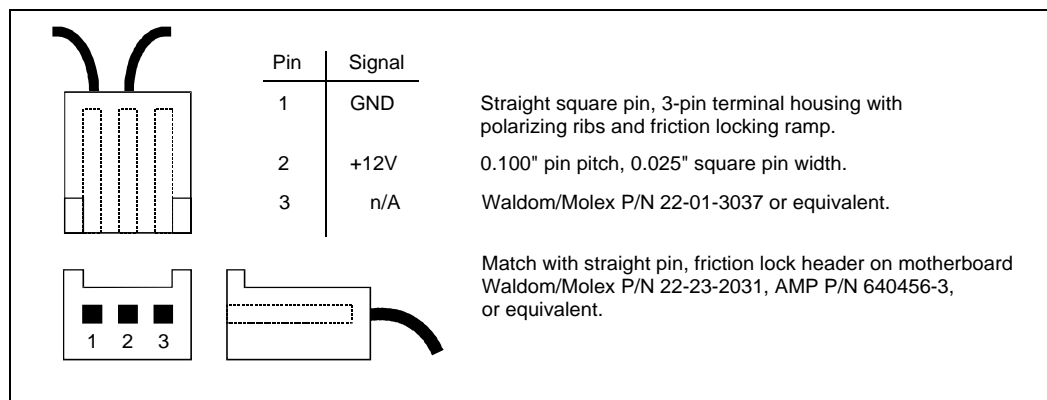


Table 41. Fan Heat Sink Power and Signal Specifications

Description	Min	Typ	Max
+12 V: 12 volt fan power supply	7 V	12 V	13.8 V
IC: Fan current draw			100 mA

Figure 29. Motherboard Power Header Placement Relative to the Intel® Celeron™ Processor in the PPGA Package

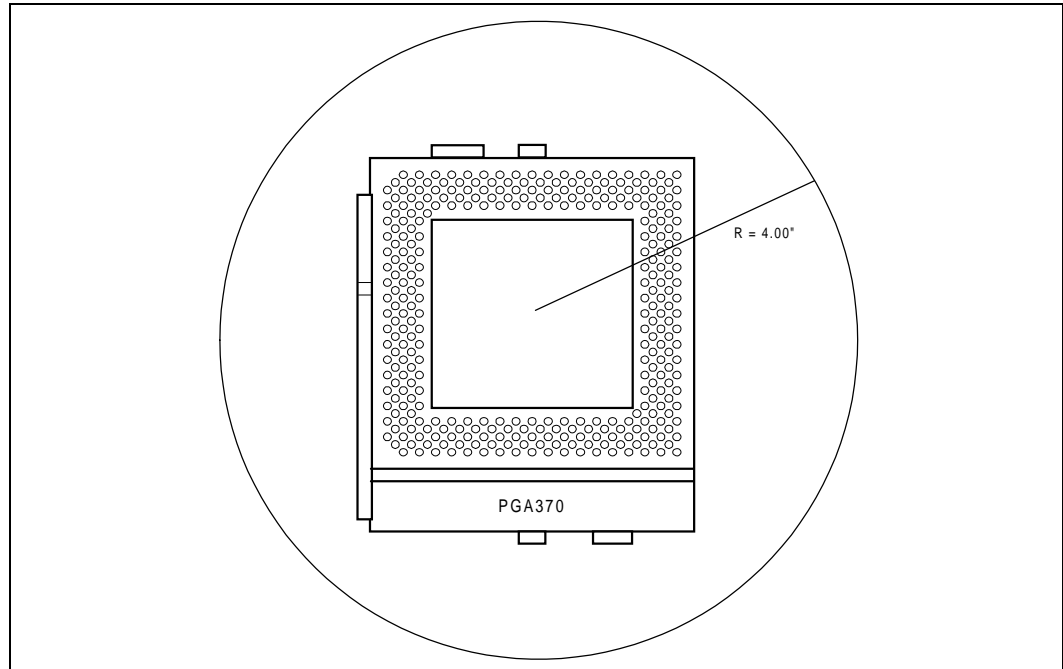


Figure 30. Top View of Motherboard Keepout Requirements

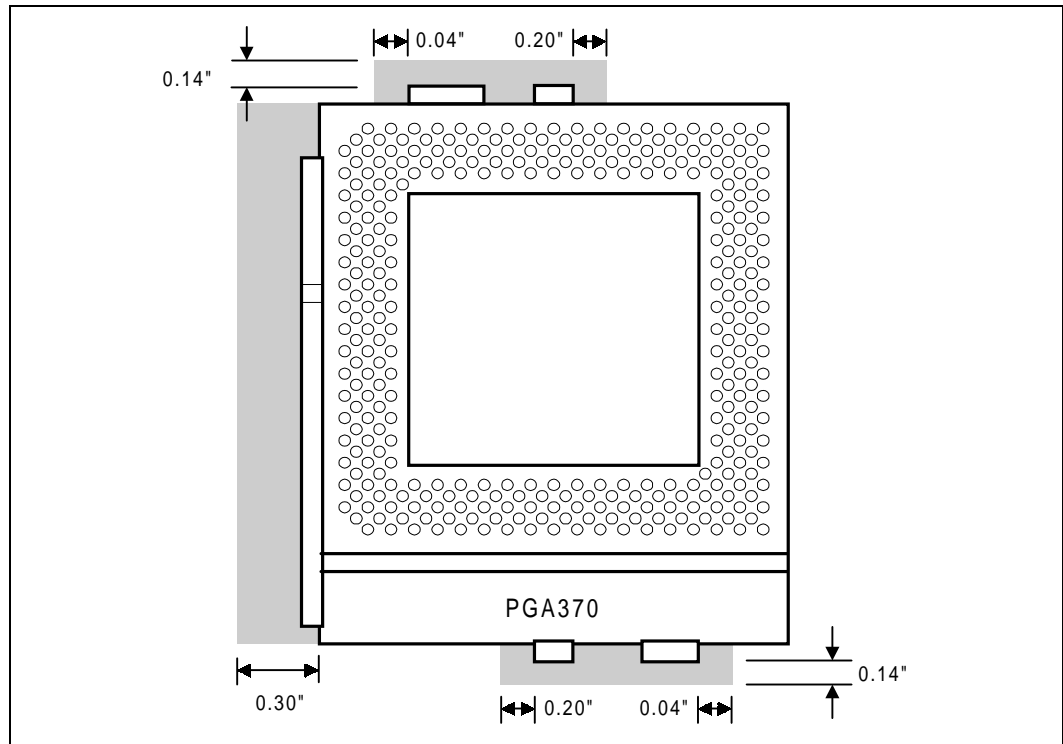
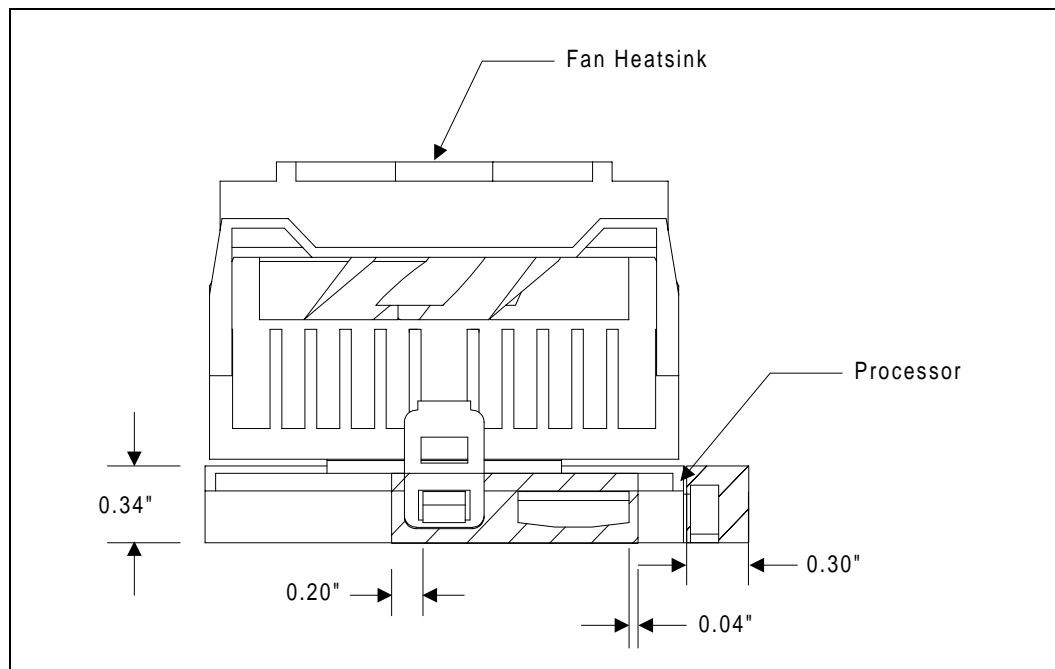


Figure 31. Side View of Motherboard Keepout Requirements



6.2.4 Thermal Specifications

This section describes the cooling requirements of the fan heat sink solution utilized by the boxed processor.

6.2.4.1 Boxed Processor Cooling Requirements

The boxed Intel® Celeron™ processor fan heat sink is designed to keep the processor within thermal specifications under the following conditions: the temperature entering the fan inlet remains below 45°C (see Figure 27 for measurement location), the provided airflow through the fan heat sink is unimpeded (see Figure 27), the processor power is generated by commercially available software (applications and operating system) rather than synthetic testing hardware (silicon testers)

Refer to Section 4.0 for Intel® Celeron™ processor thermal and power specifications.

Airspace is required around the fan to ensure that the airflow through the fan heat sink is not blocked. Blocking the airflow to the fan heat sink reduces the cooling efficiency and decreases fan life. Figure 27 illustrates an acceptable airspace clearance for the fan heat sink.

7.0 Intel® Celeron™ Processor Signal Description

Table 42 provides an alphabetical listing of all Intel® Celeron™ processor signals. The tables at the end of this section summarize the signals by direction: output, input, and I/O.

Note: Unless otherwise noted, the signals apply to both S.E.P. and PPGA Packages

Table 42. Alphabetical Signal Reference (Sheet 1 of 6)

Signal	Type	Description
A[31:3]#	I/O	<p>The A[31:3]# (Address) signals define a 2³²-byte physical memory address space. When ADS# is active, these pins transmit the address of a transaction; when ADS# is inactive, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Intel® Celeron™ processor system bus. The A[31:24]# signals are parity-protected by the AP1# parity signal, and the A[23:3]# signals are parity-protected by the AP0# parity signal.</p> <p>On the active-to-inactive transition of RESET#, the processors sample the A[31:3]# pins to determine their power-on configuration. See the <i>Pentium® II Processor Developer's Manual</i> (Order Number 243502) for details.</p>
A20M#	I	<p>If the A20M# (Address-20 Mask) input signal is asserted, the Intel Celeron processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1 MB boundary. Assertion of A20M# is only supported in real mode.</p> <p>A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.</p>
ADS#	I/O	<p>The ADS# (Address Strobe) signal is asserted to indicate the validity of the transaction address on the A[31:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all Intel Celeron processor system bus agents.</p>
BCLK	I	<p>The BCLK (Bus Clock) signal determines the bus frequency. All Intel Celeron processor system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge.</p> <p>All external timing parameters are specified with respect to the BCLK signal.</p>
BNR#	I/O	<p>The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.</p> <p>Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all Intel Celeron processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.</p>
BP[3:2]#	I/O	<p>The BP[3:2]# (Breakpoint) signals are outputs from the processor that indicate the status of breakpoints.</p>
BPM[1:0]#	I/O	<p>The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance.</p>
BPRI#	I	<p>The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the Intel Celeron processor system bus. It must connect the appropriate pins of all Intel Celeron processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.</p>

Table 42. Alphabetical Signal Reference (Sheet 2 of 6)

Signal	Type	Description
BSEL	I/O	This signal indicates the system bus frequency supported by the processor. A logic low indicates a host bus frequency of 66 MHz.
BR0#	I/O	The BR0# (Bus Request) pin drives the BREQ[0]# signal in the system. During power-up configuration, the central agent asserts the BREQ0# bus signal in the system to assign the symmetric agent ID to the processor. The processor samples its BR0# pin on the active-to-inactive transition of RESET# to obtain its symmetric agent ID. The processor asserts BR0# to request the system bus.
CPUPRES# (PPGA only)	O	The CPUPRES# signal provides the ability for a system board to detect the presence of a processor. This pin is a ground on the processor indicating to the system that a processor is installed.
D[63:0]#	I/O	The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between the Intel Celeron processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.
DBSY#	I/O	The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the Intel Celeron processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all Intel Celeron processor system bus agents.
DEFER#	I	The DEFER# signal is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all Intel Celeron processor system bus agents.
DRDY#	I/O	The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multicycle data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all Intel Celeron processor system bus agents.
EDGCTRL	I	The EDGCTRL input provides AGTL+ edge control and should be pulled up to VCC _{CORE} with a 51 Ω ± 5% resistor.
EMI (S.E.P.P. only)	I	EMI pins should be connected to motherboard ground and/or to chassis ground through zero ohm (0Ω) resistors. The zero ohm resistors should be placed in close proximity to the Intel Celeron processor connector. The path to chassis ground should be short in length and have a low impedance. These pins are used for EMI management purposes.
FERR#	O	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.
FLUSH#	I	When the FLUSH# input signal is asserted, the processor writes back all data in the Modified state from the internal cache and invalidates all internal cache lines. At the completion of this operation, the processor issues a Flush Acknowledge transaction. The processor does not cache any new data while the FLUSH# signal remains asserted. FLUSH# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. On the active-to-inactive transition of RESET#, the processor samples FLUSH# to determine its power-on configuration. See <i>Pentium® Pro Family Developer's Manual, Volume 1: Specifications</i> (Order Number 242690) for details.
HIT#, HITM#	I/O	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must connect the appropriate pins of all Intel Celeron processor system bus agents. Any such agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.

Table 42. Alphabetical Signal Reference (Sheet 3 of 6)

Signal	Type	Description
IERR#	O	The IERR# (Internal Error) signal is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the Intel Celeron processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
INIT#	I	The INIT# (Initialization) signal, when asserted, resets integer registers inside all processors without affecting their internal (L1) caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
LINT[1:0]	I	The LINT[1:0] (Local APIC Interrupt) signals must connect the appropriate pins of all APIC Bus agents, including all processors and the core logic or I/O APIC component. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium® processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	The LOCK# signal indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the system bus throughout the bus locked operation and ensure the atomicity of lock.
PICCLK	I	The PICCLK (APIC Clock) signal is an input clock to the processor and core logic or I/O APIC which is required for operation of all processors, core logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O	The PICD[1:0] (APIC Data) signals are used for bidirectional serial message passing on the APIC bus, and must connect the appropriate pins of the Intel Celeron processor for proper initialization.
PLL1, PLL2 (PPGA only)	I	All Intel Celeron processors have internal analog PLL clock generators that require quiet power supplies. PLL1 and PLL2 are inputs to the internal PLL and should be connected to V _{CC} CORE through a low-pass filter that minimizes jitter.
PRDY#	O	The PRDY (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processors.

Table 42. Alphabetical Signal Reference (Sheet 4 of 6)

Signal	Type	Description
PWRGOOD	I	<p>The PWRGOOD (Power Good) signal is a 2.5 V tolerant processor input. The processor requires this signal to be a clean indication that the clocks and power supplies ($V_{CC_{CORE}}$, etc.) are stable and within their specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high (2.5 V) state. Figure 23 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 14 and Table 15, and be followed by a 1 ms RESET# pulse.</p> <p>The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.</p> <p>PWRGOOD Relationship at Power-On</p>
REQ[4:0]#	I/O	<p>The REQ[4:0]# (Request Command) signals must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner over two clock cycles to define the currently active transaction type.</p>
RESET#	I	<p>Asserting the RESET# signal resets the processor to a known state and invalidates the L1 cache without writing back any of the contents. RESET# must stay active for at least one millisecond after $V_{CC_{CORE}}$ and CLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks.</p> <p>A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the <i>Pentium® Pro Family Developer's Manual, Volume 1: Specifications</i> (Order Number 242690).</p> <p>The processor may have its outputs tristated via power-on configuration. Otherwise, if INIT# is sampled active during the active-to-inactive transition of RESET#, the processor will execute its Built-in Self-Test (BIST). Whether or not BIST is executed, the processor will begin program execution at the power on Reset vector (default 0_FFFF_FFF0h). RESET# must connect the appropriate pins of all processor system bus agents.</p>
RS[2:0]#	I	<p>The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.</p>

Table 42. Alphabetical Signal Reference (Sheet 5 of 6)

Signal	Type	Description												
SLOTOCC# (S.E.P.P. only)	O	<p>SLOTOCC# is defined to allow a system design to detect the presence of a terminator card or processor in a SC242 connector. This pin is not a signal; rather, it is a short to VSS. Combined with the VID combination of VID[4:0]= 11111 (see Section 2.5), a system can determine if a SC242 connector is occupied, and whether a processor core is present. The states and values for determining the type of cartridge in the SC242 connector is shown below.</p> <p style="text-align: center;">SC242 Occupation Truth Table</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Signal</th> <th>Value</th> <th>Status</th> </tr> </thead> <tbody> <tr> <td>SLOTOCC# VID[4:0]</td> <td>0 Anything other than '11111'</td> <td>Processor with core in SC242 connector.</td> </tr> <tr> <td>SLOTOCC# VID[4:0]</td> <td>0 11111</td> <td>Terminator cartridge in SC242 connector (i.e., no core present).</td> </tr> <tr> <td>SLOTOCC# VID[4:0]</td> <td>1 Any value</td> <td>SC242 connector not occupied.</td> </tr> </tbody> </table>	Signal	Value	Status	SLOTOCC# VID[4:0]	0 Anything other than '11111'	Processor with core in SC242 connector.	SLOTOCC# VID[4:0]	0 11111	Terminator cartridge in SC242 connector (i.e., no core present).	SLOTOCC# VID[4:0]	1 Any value	SC242 connector not occupied.
Signal	Value	Status												
SLOTOCC# VID[4:0]	0 Anything other than '11111'	Processor with core in SC242 connector.												
SLOTOCC# VID[4:0]	0 11111	Terminator cartridge in SC242 connector (i.e., no core present).												
SLOTOCC# VID[4:0]	1 Any value	SC242 connector not occupied.												
SLP#	I	The SLP# (Sleep) signal, when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertions of the SLP#, STPCLK#, and RESET# signals while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and APIC processor core units.												
SMI#	I	The SMI# (System Management Interrupt) signal is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.												
STPCLK#	I	The STPCLK# (Stop Clock) signal, when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the bus and APIC units. The processor continues to snoop bus transactions and may latch interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units, resumes execution, and services any pending interrupt. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.												
TCK	I	The TCK (Test Clock) signal provides the clock input for the Intel Celeron processor Test Access Port.												
TDI	I	The TDI (Test Data In) signal transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.												
TDO	O	The TDO (Test Data Out) signal transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.												
TESTHI (S.E.P.P. only)	I	Refer to Section 2.6 for implementation details.												
THERMDN	O	Thermal Diode p-n junction. Used to calculate core temperature. See Section 4.1 .												
THERMDP	I	Thermal Diode p-n junction. Used to calculate core temperature. See Section 4.1 .												
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 135 °C. This is signaled to the system by the THERMTRIP# (Thermal Trip) pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will reassert THERMTRIP# and remain stopped.												

Table 42. Alphabetical Signal Reference (Sheet 6 of 6)

Signal	Type	Description
TMS	I	The TMS (Test Mode Select) signal is a JTAG specification support signal used by debug tools.
TRDY#	I	The TRDY# (Target Ready) signal is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	I	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. Intel Celeron processors require this signal to be driven low during power on Reset. A 680 ohm resistor is the suggested value for a pull down resistor on TRST#.
VCC _{1.5} (PPGA only)	I	The VCC _{CMOS} pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the VCC _{2.5} input and 1.5 V must be provided to the VCC _{1.5} input. The processor re-routes the 2.5 V input to the VCC _{CMOS} output via the package. Future processors requiring 1.5 V CMOS voltage levels will route the 1.5 V at the VCC _{1.5} input to the VCC _{CMOS} output.
VCC _{2.5} (PPGA only)	I	The VCC _{CMOS} pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the VCC _{2.5} input and 1.5 V must be provided to the VCC _{1.5} input. The processor re-routes the 2.5 V input to the VCC _{CMOS} output via the package. Future processors requiring 1.5 V CMOS voltage levels will route the 1.5 V at the VCC _{1.5} input to the VCC _{CMOS} output.
VCC _{CMOS} (PPGA only)	O	The VCC _{CMOS} pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the VCC _{2.5} input and 1.5 V must be provided to the VCC _{1.5} input. The processor re-routes the 2.5 V input to the VCC _{CMOS} output via the package. Future processors requiring 1.5 V CMOS voltage levels will route the 1.5 V at the VCC _{1.5} input to the VCC _{CMOS} output.
VCORE _{DET} (PPGA only)	O	The VCORE _{DET} signal will float for 2.0 V core processors and will be grounded for future processors with a lower core voltage.
VID[4:0] (S.E.P.P.) VID[3:0] (PPGA)	O	The VID (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support voltage specification variations on Intel Celeron processors. See Table 1 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
VREF[7:0] (PPGA only)	I	These input signals are used by the AGTL+ inputs as a reference voltage. AGTL+ inputs are differential receivers and will use this voltage to determine whether the signal is a logic high or logic low.

7.1 Signal Summaries

Table 43 through Table 46 list attributes of the Intel® Celeron™ processor output, input, and I/O signals.

Table 43. Output Signals

Name	Active Level	Clock	Signal Group
CPUPRES# (PPGA only)	Low	Asynch	Power/Other
FERR#	Low	Asynch	CMOS Output
IERR#	Low	Asynch	CMOS Output
PRDY#	Low	BCLK	AGTL+ Output
SLOTICC# (S.E.P.P. only)	Low	Asynch	Power/Other
TDO	High	TCK	TAP Output
THERMDN	N/A	Asynch	Power/Other
THERMTRIP#	Low	Asynch	CMOS Output
V _{COREDET} (PPGA only)	High	Asynch	Power/Other
VID[4:0] (S.E.P.P.) VID[3:0] (PPGA)	High	Asynch	Power/Other

Table 44. Input Signals (Sheet 1 of 2)

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	CMOS Input	Always ¹
BPRI#	Low	BCLK	AGTL+ Input	Always
BCLK	High	—	System Bus Clock	Always
DEFER#	Low	BCLK	AGTL+ Input	Always
FLUSH#	Low	Asynch	CMOS Input	Always ¹
IGNNE#	Low	Asynch	CMOS Input	Always ¹
INIT#	Low	Asynch	CMOS Input	Always ¹
INTR	High	Asynch	CMOS Input	APIC disabled mode
LINT[1:0]	High	Asynch	CMOS Input	APIC enabled mode
NMI	High	Asynch	CMOS Input	APIC disabled mode
PICCLK	High	—	APIC Clock	Always
PREQ#	Low	Asynch	CMOS Input	Always
PWRGOOD	High	Asynch	CMOS Input	Always
RESET#	Low	BCLK	AGTL+ Input	Always
RS[2:0]#	Low	BCLK	AGTL+ Input	Always
SLP#	Low	Asynch	CMOS Input	During Stop-Grant state
SMI#	Low	Asynch	CMOS Input	
STPCLK#	Low	Asynch	CMOS Input	
TCK	High	—	TAP Input	

Table 44. Input Signals (Sheet 2 of 2)

Name	Active Level	Clock	Signal Group	Qualified
TDI	High	TCK	TAP Input	
TESTHI (S.E.P.P. only)	High	Asynch	Power/Other	Always
THERMDP	N/A	Asynch	Power/Other	
TMS	High	TCK	TAP Input	
TRST#	Low	Asynch	TAP Input	
TRDY#	Low	BCLK	AGTL+ Input	

NOTE:

1. Synchronous assertion with active TRDY# ensures synchronization.

Table 45. Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
BSEL	Low	Asynch	Power/Other	Always
BP[3:2]	Low	BCLK	AGTL+ I/O	Always
A[31:3]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
ADS#	Low	BCLK	AGTL+ I/O	Always
BPM[1:0]#	Low	BCLK	AGTL+ I/O	Always
D[63:0]#	Low	BCLK	AGTL+ I/O	DRDY#
DBSY#	Low	BCLK	AGTL+ I/O	Always
DRDY#	Low	BCLK	AGTL+ I/O	Always
LOCK#	Low	BCLK	AGTL+ I/O	Always
REQ[4:0]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1

Table 46. Input/Output Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
BNR#	Low	BCLK	AGTL+ I/O	Always
HIT#	Low	BCLK	AGTL+ I/O	Always
HITM#	Low	BCLK	AGTL+ I/O	Always
PICD[1:0]	High	PICCLK	APIC I/O	Always