



# 128Kx64 3.3V SRAM MODULE

ADVANCED\*

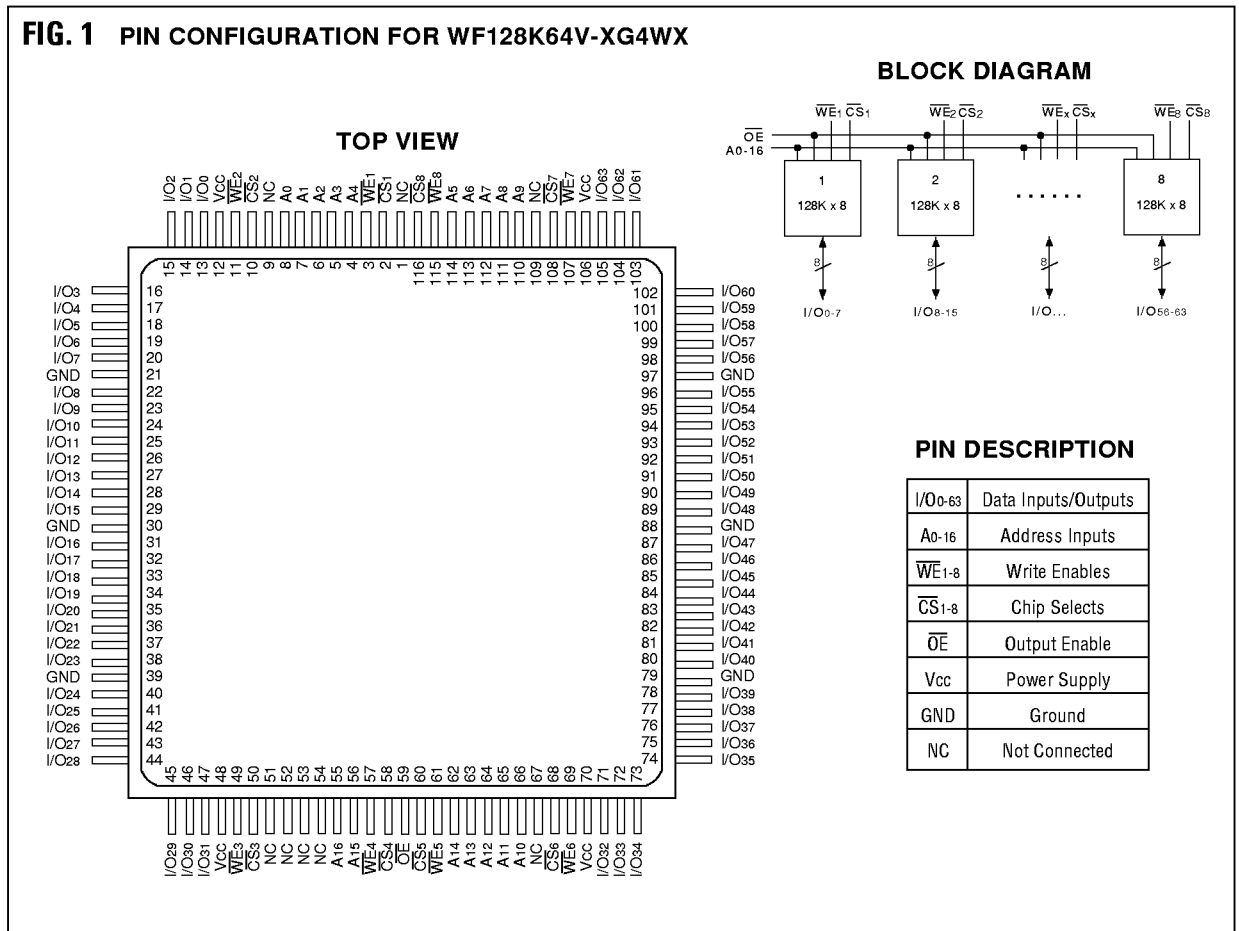
## FEATURES

- Access Times of 15, 17, 20, 25ns
- Packaging
  - 116 lead, 40mm square, Hermetic CQFP (Package 504)
- Organized as 128Kx64, User Configurable as 256Kx32, 512Kx16 or 1Mx8.
- Commercial, Industrial and Military Temperature Ranges
- 3 Volt Power Supply
- Low Power CMOS
- 2V Data Retention Devices Available (Low Power Version)
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight  
WF128K64V-XG4WX - 20 grams typical

\* This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.

Note: Programming information available upon request.

### FIG. 1 PIN CONFIGURATION FOR WF128K64V-XG4WX





### ABSOLUTE MAXIMUM RATINGS

| Parameter                      | Symbol           | Min  | Max  | Unit |
|--------------------------------|------------------|------|------|------|
| Operating Temperature          | T <sub>A</sub>   | -55  | +125 | °C   |
| Storage Temperature            | T <sub>STG</sub> | -65  | +150 | °C   |
| Signal Voltage Relative to GND | V <sub>G</sub>   | -0.5 | 4.6  | V    |
| Junction Temperature           | T <sub>J</sub>   |      | 150  | °C   |
| Supply Voltage                 | V <sub>CC</sub>  | -0.5 | 4.6  | V    |

### RECOMMENDED OPERATING CONDITIONS

| Parameter              | Symbol          | Min  | Max                   | Unit |
|------------------------|-----------------|------|-----------------------|------|
| Supply Voltage         | V <sub>CC</sub> | 3.0  | 3.6                   | V    |
| Input High Voltage     | V <sub>IH</sub> | 2.2  | V <sub>CC</sub> + 0.3 | V    |
| Input Low Voltage      | V <sub>IL</sub> | -0.3 | +0.8                  | V    |
| Operating Temp. (Mil.) | T <sub>A</sub>  | -55  | +125                  | °C   |

### TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode        | Data I/O | Power   |
|-----------------|-----------------|-----------------|-------------|----------|---------|
| H               | X               | X               | Standby     | High Z   | Standby |
| L               | L               | H               | Read        | Data Out | Active  |
| L               | X               | L               | Write       | Data In  | Active  |
| L               | H               | H               | Out Disable | High Z   | Active  |

### CAPACITANCE

(T<sub>A</sub> = +25°C)

| Parameter                   | Symbol           | Conditions                          | Max | Unit |
|-----------------------------|------------------|-------------------------------------|-----|------|
| $\overline{OE}$ capacitance | C <sub>OE</sub>  | V <sub>IN</sub> = 0 V, f = 1.0 MHz  | 100 | pF   |
| $\overline{WE}$ capacitance | C <sub>WE</sub>  | V <sub>IN</sub> = 0 V, f = 1.0 MHz  | 20  | pF   |
| $\overline{CS}$ capacitance | C <sub>CS</sub>  | V <sub>IN</sub> = 0 V, f = 1.0 MHz  | 20  | pF   |
| Data I/O capacitance        | C <sub>I/O</sub> | V <sub>I/O</sub> = 0 V, f = 1.0 MHz | 20  | pF   |
| Address input capacitance   | C <sub>AD</sub>  | V <sub>IN</sub> = 0 V, f = 1.0 MHz  | 100 | pF   |

This parameter is guaranteed by design but not tested.

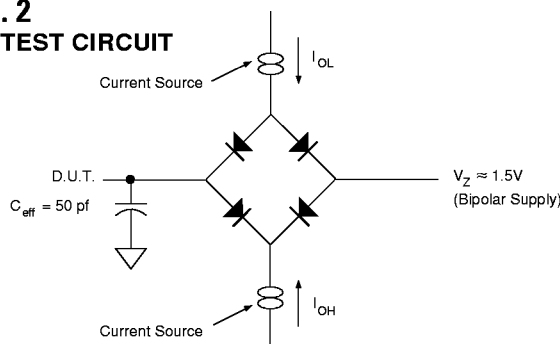
### DC CHARACTERISTICS

(V<sub>CC</sub> = 3.3V ± 0.3V, T<sub>A</sub> = -55°C to +125°C)

| Parameter                | Sym             | Conditions   |     |     | Units |
|--------------------------|-----------------|--|-----|-----|-------|
|                          |                 |  | Min | Max |       |
| Input Leakage Current    | I <sub>LI</sub> | V <sub>IN</sub> = GND to V <sub>CC</sub>   |     | 10  | µA    |
| Output Leakage Current   | I <sub>LO</sub> | $\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, V_{OUT} = GND \text{ to } V_{CC}$ |     | 10  | µA    |
| Operating Supply Current | I <sub>CC</sub> | $\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 3.6$    |     | 1   | A     |
| Standby Current          | I <sub>SB</sub> | $\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 3.6$    |     | 64  | mA    |
| Output Low Voltage       | V <sub>OL</sub> | I <sub>OL</sub> = 8mA  |     | 0.4 | V     |
| Output High Voltage      | V <sub>OH</sub> | I <sub>OH</sub> = -4.0mA   | 2.4 |     | V     |

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V

### FIG. 2 AC TEST CIRCUIT



### AC TEST CONDITIONS

| Parameter                        | Typ  | Unit |
|----------------------------------|--|------|
| Input Pulse Levels               | V <sub>IL</sub> = 0, V <sub>IH</sub> = 2.5 | V    |
| Input Rise and Fall              | 5  | ns   |
| Input and Output Reference Level | 1.5  | V    |
| Output Timing Reference Level    | 1.5  | V    |

#### NOTES:

V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75 Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.

**AC CHARACTERISTICS** $(V_{CC} = 3.3V \pm 0.3V, T_A = -55^{\circ}C \text{ To } +125^{\circ}C)$ 

| Parameter                          | Symbol                        | <u>-15</u> |     | <u>-17</u> |     | <u>-20</u> |     | <u>-25</u> |     | Units |
|------------------------------------|-------------------------------|------------|-----|------------|-----|------------|-----|------------|-----|-------|
|                                    |                               | Min        | Max | Min        | Max | Min        | Max | Min        | Max |       |
| <b>Read Cycle</b>                  |                               |            |     |            |     |            |     |            |     |       |
| Read Cycle Time                    | t <sub>RC</sub>               | 15         |     | 17         |     | 20         |     | 25         |     | ns    |
| Address Access Time                | t <sub>AA</sub>               |            | 15  |            | 17  |            | 20  |            | 25  | ns    |
| Output Hold from Address Change    | t <sub>OH</sub>               | 0          |     | 0          |     | 0          |     | 0          |     | ns    |
| Chip Select Access Time            | t <sub>ACS</sub>              |            | 15  |            | 17  |            | 20  |            | 25  | ns    |
| Output Enable to Output Valid      | t <sub>OE</sub>               |            | 10  |            | 10  |            | 12  |            | 15  | ns    |
| Chip Select to Output in Low Z     | t <sub>CLZ</sub> <sup>1</sup> | 3          |     | 3          |     | 3          |     | 3          |     | ns    |
| Output Enable to Output in Low Z   | t <sub>OLZ</sub> <sup>1</sup> | 0          |     | 0          |     | 0          |     | 0          |     | ns    |
| Chip Disable to Output in High Z   | t <sub>CHZ</sub> <sup>1</sup> |            | 10  |            | 10  |            | 12  |            | 12  | ns    |
| Output Disable to Output in High Z | t <sub>OHZ</sub> <sup>1</sup> |            | 10  |            | 10  |            | 12  |            | 12  | ns    |

1. This parameter is guaranteed by design but not tested.

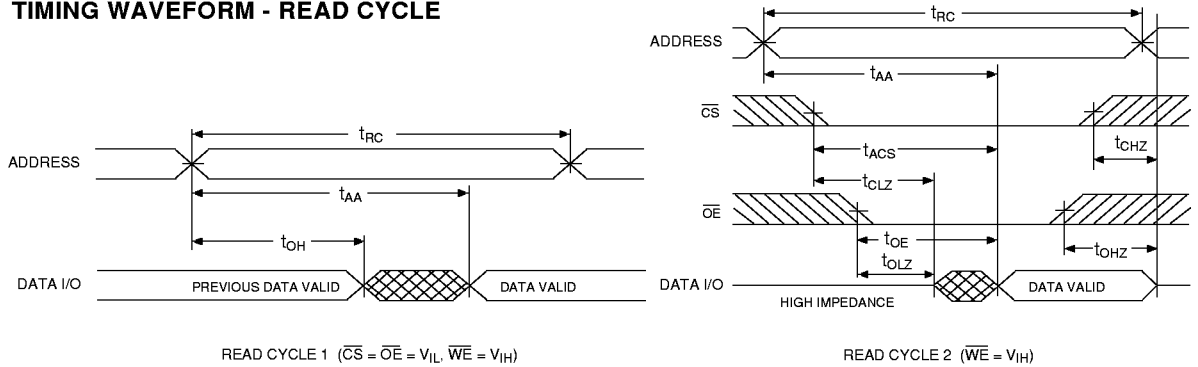
**AC CHARACTERISTICS** $(V_{CC} = 3.3V \pm 0.3V, T_A = -55^{\circ}C \text{ To } +125^{\circ}C)$ 

| Parameter                        | Symbol                        | <u>-15</u> |     | <u>-17</u> |     | <u>-20</u> |     | <u>-25</u> |     | Units |
|----------------------------------|-------------------------------|------------|-----|------------|-----|------------|-----|------------|-----|-------|
|                                  |                               | Min        | Max | Min        | Max | Min        | Max | Min        | Max |       |
| <b>Write Cycle</b>               |                               |            |     |            |     |            |     |            |     |       |
| Write Cycle Time                 | t <sub>WC</sub>               | 15         |     | 17         |     | 20         |     | 25         |     | ns    |
| Chip Select to End of Write      | t <sub>CW</sub>               | 14         |     | 14         |     | 15         |     | 20         |     | ns    |
| Address Valid to End of Write    | t <sub>AW</sub>               | 14         |     | 14         |     | 15         |     | 20         |     | ns    |
| Data Valid to End of Write       | t <sub>DW</sub>               | 10         |     | 10         |     | 12         |     | 15         |     | ns    |
| Write Pulse Width                | t <sub>WP</sub>               | 14         |     | 14         |     | 15         |     | 20         |     | ns    |
| Address Setup Time               | t <sub>AS</sub>               | 0          |     | 0          |     | 0          |     | 0          |     | ns    |
| Address Hold Time                | t <sub>AH</sub>               | 0          |     | 0          |     | 0          |     | 0          |     | ns    |
| Output Active from End of Write  | t <sub>OW</sub> <sup>1</sup>  | 3          |     | 3          |     | 3          |     | 3          |     | ns    |
| Write Enable to Output in High Z | t <sub>WHZ</sub> <sup>1</sup> |            | 10  |            | 10  |            | 12  |            | 15  | ns    |
| Data Hold Time                   | t <sub>DH</sub>               | 0          |     | 0          |     | 0          |     | 0          |     | ns    |

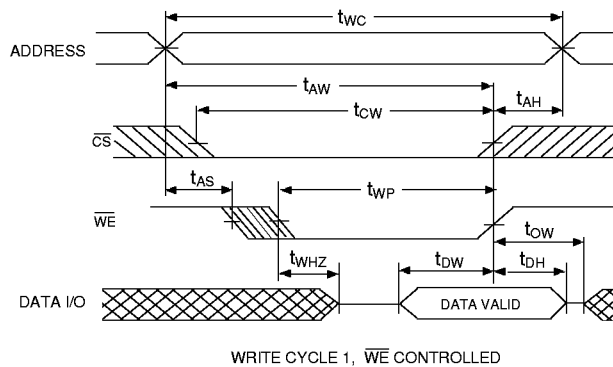
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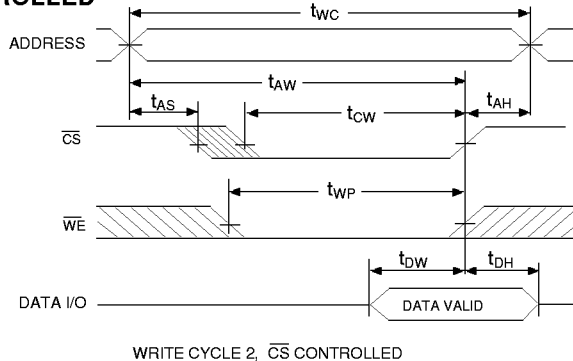
**FIG. 3**  
**TIMING WAVEFORM - READ CYCLE**



**FIG. 4**  
**WRITE CYCLE -  $\overline{WE}$  CONTROLLED**

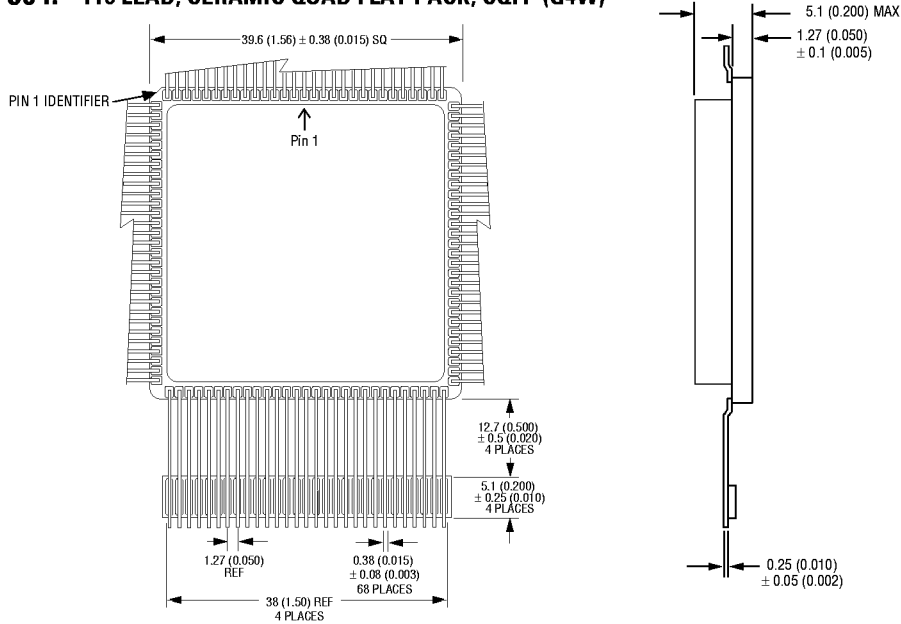


**FIG. 5**  
**WRITE CYCLE -  $\overline{CS}$  CONTROLLED**





**PACKAGE 504: 116 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4W)**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**ORDERING INFORMATION**

**W S 128K64 V - XXX G4W X**

