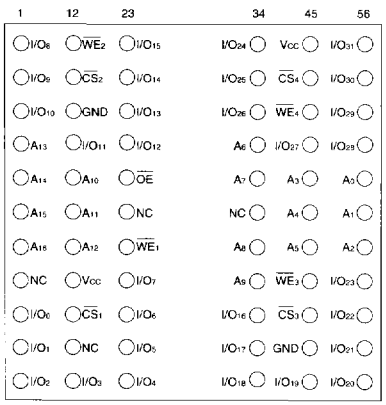
128Kx32 SRAM MODULE

FEATURES

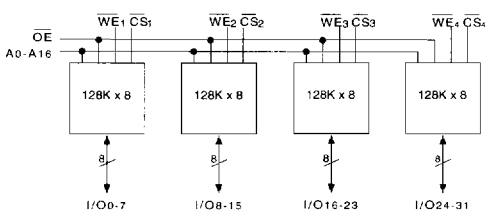
- Access Time 20nS
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 66-pin, PGA Type, 1.185 inch square HIP, Hermetic Ceramic Package, Industry Standard Pinout, SMD Number 5962-93187-09HXX
  - 68 lead, 40mm, Hermetic CQFP
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS128K32-XHX - 13 grams typical
  WS128K32-XG4X - 20 grams typical

FIG. 1 PIN CONFIGURATION FOR WS128K32N-20HX, SMD 5962-93187-09HXX

TOP VIEW



BLOCK DIAGRAM



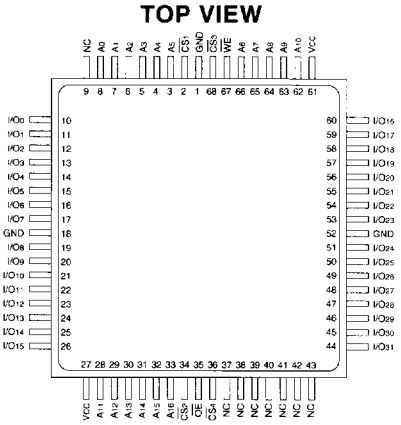
PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

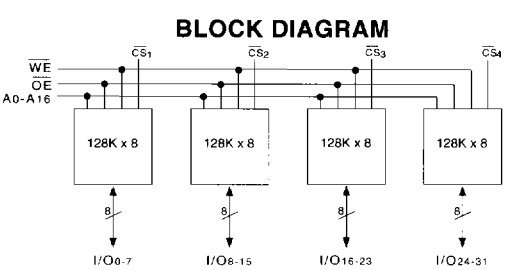
SID2301

FIG. 2 PIN CONFIGURATION FOR WS128K32-20G4X

TOP VIEW



BLOCK DIAGRAM



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature Range	T_{STG}	-65	+150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V
Signal Voltages Any Pin	V_G	-0.5	V_{CC} + 0.5	V
Junction Temperature	T_J		150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(@ T_A = +25°C)

Test	Symbol	Conditions	Limits		Unit
			Min	Max	
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz		50	pF
$\overline{WE}$ 1-4 capicitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz		30	pF
$\overline{CS}$ 1-4 capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz		30	pF
D0 - D31 capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz		30	pF
A0 - A16 capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz		50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-20			Units
			Min	Typ	Max	
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = GND to V_{CC}			10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}			10	µA
OperatingSupply Current x32 mode	I_{CCx32}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		430	750	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, V_{IN}=V_{IL} or V_{IH}, Duty Cycle = 100%		60	100	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4			V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-20			Units
			Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ ≥ V_{CC} -.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		0.1	8.5	mA

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter Read Cycle	Symbol	-20 Min	 Max	Units
Read Cycle Time	t_{RC}	20		nS
Address Access Time	t_{AA}		20	nS
Output Hold from Address Change	t_{OH}	4		nS
Chip Select Access Time	t_{ACS}		20	nS
Output Enable to Output Valid	t_{OE}		15	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	4		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	4		nS
Chip Select to Output in High Z	t_{CHZ}[1]		12	nS
Output Enable to Output in High Z	t_{OHZ}[1]		12	nS

1. This parameter is guaranteed by design but not tested.

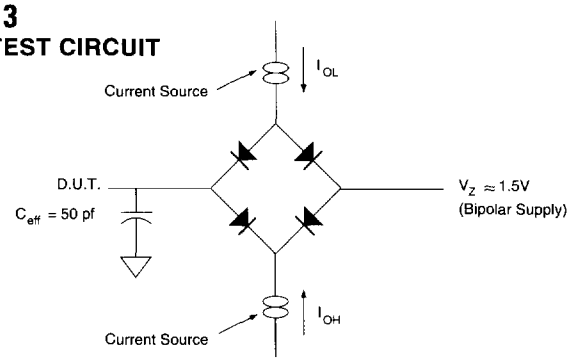
AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter Write Cycle	Symbol	-20 Min	 Max	Units
Write Cycle Time	t_{WC}	20		nS
Chip Select to End of Write	t_{CW}	15		nS
Address Valid to End of Write	t_{AW}	15		nS
Data Valid to End of Write	t_{DW}	12		nS
Write Pulse Width	t_{WP}	15		nS
Address Setup Time	t_{AS}	0		nS
Address Hold Time	t_{AH}	0		nS
Output Active from End of Write	t_{OW}[1]	4		nS
Write Enable to Output in High Z	t_{WHZ}[1]		10	nS
Data Hold Time	t_{DH}	0		nS

1. This parameter is guaranteed by design but not tested.

FIG. 3
AC TEST CIRCUIT

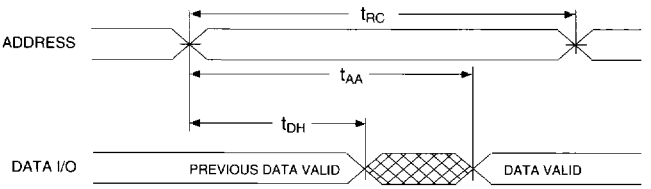


AC TEST CONDITIONS

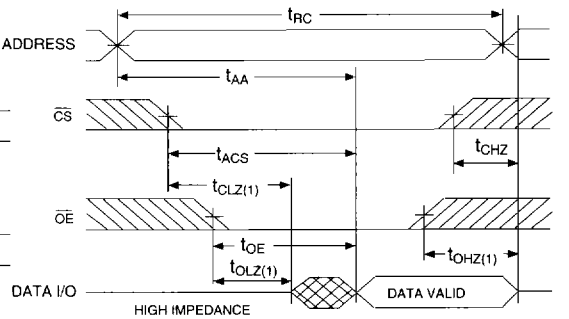
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 4
TIMING WAVEFORM - READ CYCLE



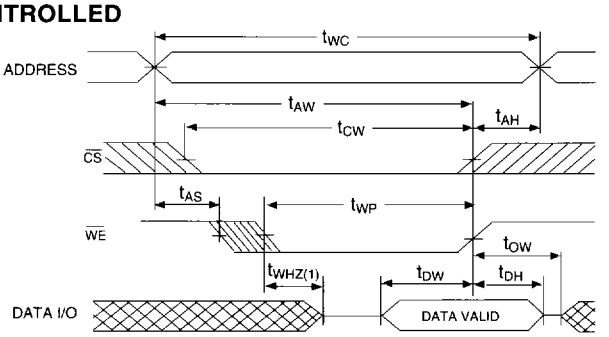
READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



READ CYCLE 2 ($\overline{WE}$ = V_{IH})

(1) GUARANTEED BY DESIGN BUT NOT TESTED

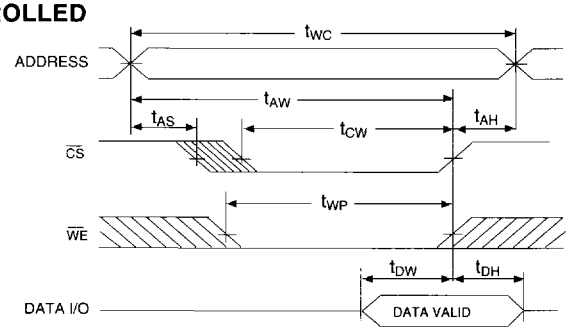
FIG. 5
WRITE CYCLE - $\overline{WE}$ CONTROLLED ($\overline{OE}$ IS INACTIVE - HIGH)



WRITE CYCLE 1 $\overline{WE}$ CONTROLLED ($\overline{OE}$ = V_{IH})

(1) GUARANTEED BY DESIGN BUT NOT TESTED

FIG. 6
WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2 $\overline{CS}$ CONTROLLED ($\overline{OE}$ = V_{IH})

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

FIG. 7
PACKAGE DIMENSIONS (16A06)

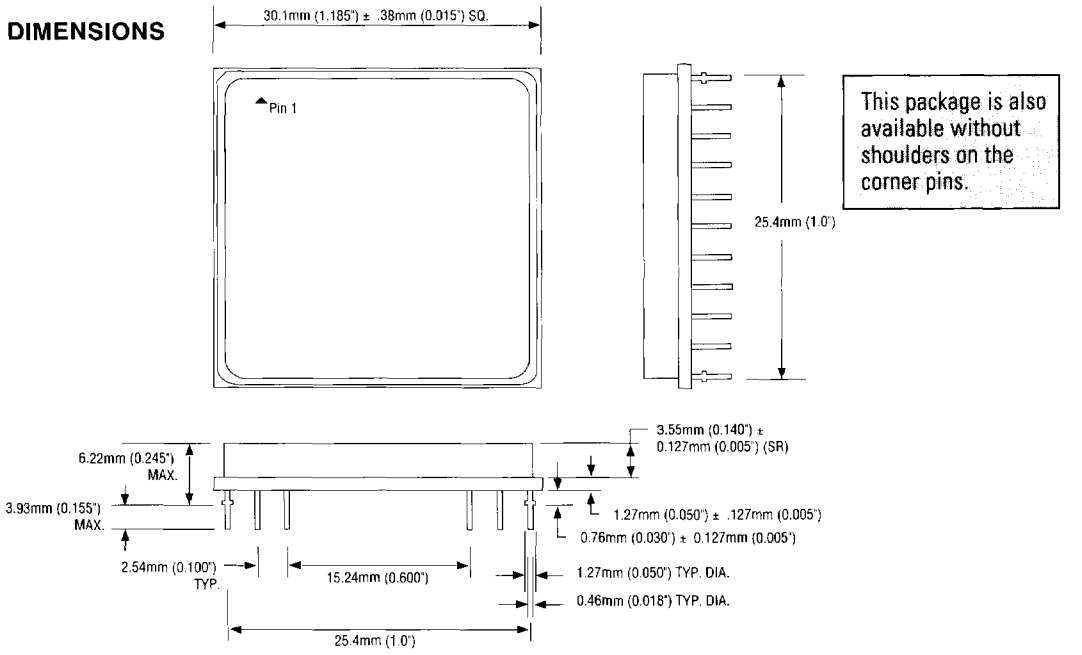
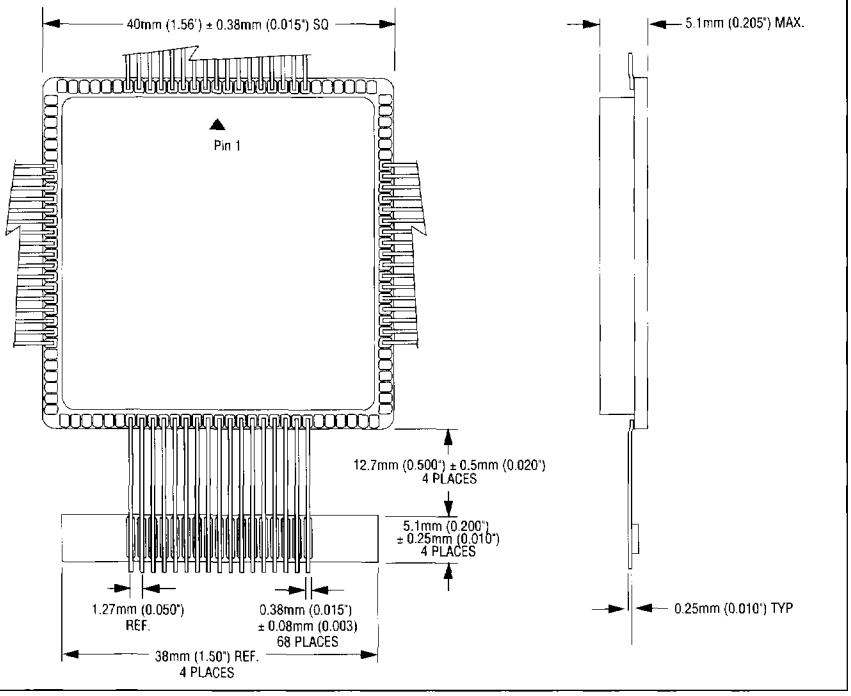


FIG. 8
PACKAGE DIMENSIONS (14A15)



ORDERING INFORMATION