4-BIT UNIVERSAL SHIFT REGISTER

The HEF4035B is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), two synchronous serial data inputs (J, $\overline{K}$), a synchronous parallel enable input (PE), buffered parallel outputs from all 4-bit positions (O_0 to O_3), a true/complement input ($T/\overline{C}$) and an overriding asynchronous master reset input (MR).
Each register is of a D-type master-slave flip-flop.

Operation is synchronous (except for MR) and is edge-triggered on the LOW to HIGH transition of the CP input. When PE is HIGH, data is loaded into the register from P_0 to P_3 on the LOW to HIGH transition of CP.

When PE is LOW, data is shifted into the first register position from J and $\overline{K}$ and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. D-type entry is obtained by interconnecting J and $\overline{K}$. When J = HIGH and $\overline{K}$ = LOW the first stage is in the toggle mode. When J = LOW and $\overline{K}$ = HIGH the first stage is in the hold mode.

The outputs (O_0 to O_3) are either inverting or non-inverting, depending on $T/\overline{C}$ state. With $T/\overline{C}$ HIGH, O_0 to O_3 are non-inverting (active HIGH) and when $T/\overline{C}$ is LOW, O_0 to O_3 are inverting (active LOW).

A HIGH on MR resets all four bit positions (O_0 to O_3 = LOW if $T/\overline{C}$ = HIGH, O_0 to O_3 = HIGH if $T/\overline{C}$ = LOW) independent of all other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

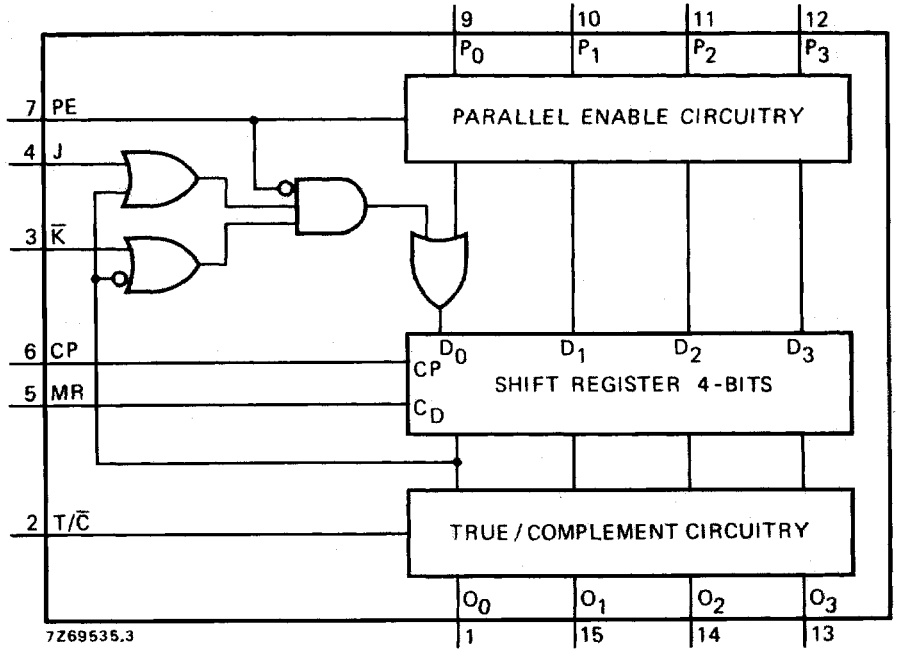

Fig. 1 Functional diagram.

FAMILY DATA
I_{DD} LIMITS category MSI
see Family Specifications

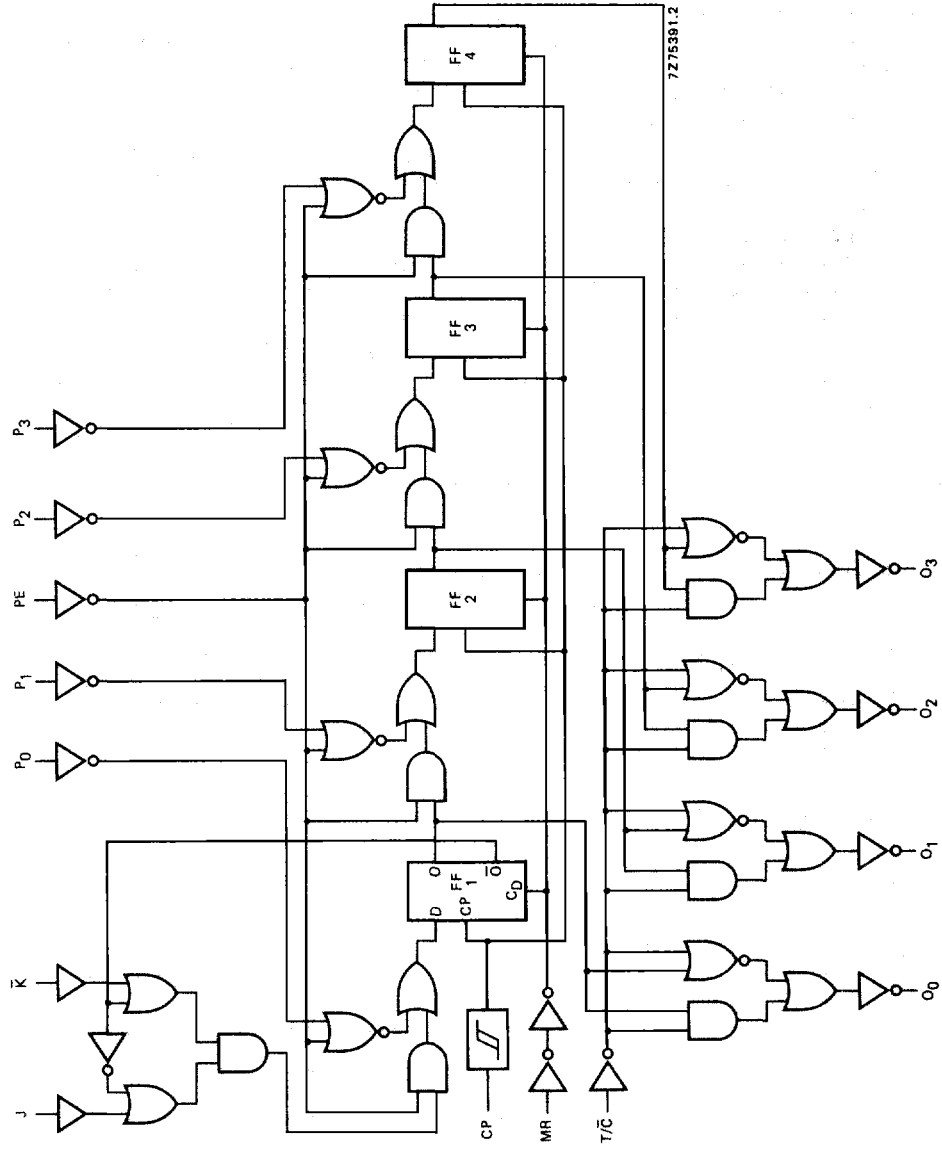

Fig. 2 Logic diagram.

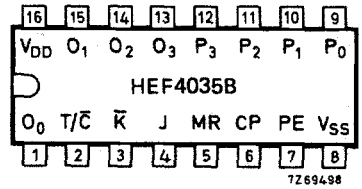

Fig. 3 Pinning diagram.

HEF4035BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4035BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4035BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

PINNING

PE	parallel enable input	CP	clock input (LOW to HIGH edge-triggered)
P_0 to P_3	parallel data inputs		
J	first stage J-input (active HIGH)	$T/\overline{C}$	true/complement input
$\overline{K}$	first stage K-input (active LOW)	MR	master reset input
		O_0 to O_3	buffered parallel outputs

FUNCTION TABLES

Serial operation first stage

inputs				output	mode of operation
CP	J	$\overline{K}$	MR	O_{0+1}	
⎍	H	H	L	H	D flip-flop
⎍	L	L	L	L	D flip-flop
⎍	H	L	L	$\overline{O}_0$	toggle
⎍	L	H	L	O_0	no change
X	X	X	H	L	reset

$T/\overline{C}$ = HIGH; PE = LOW

Parallel operation

CP	inputs				outputs			
	P_0	P_1	P_2	P_3	O_0	O_1	O_2	O_3
⎍	H	H	H	H	H	H	H	H
⎍	L	L	L	L	L	L	L	L

$T/\overline{C}$ = HIGH; PE = HIGH; MR = LOW

⎍ = positive-going transition
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
CP ⟶ O_n	5			170	340 ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		70	140 ns	59 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
	5			150	300 ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
MR ⟶ O_n	5			115	230 ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
	5			115	230 ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
$T/\overline{C}$ ⟶ O_n	5			105	210 ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
	5			85	170 ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	90 ns	34 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Minimum clock pulse width; LOW	5	t_{WCPL}	80	40		ns	see also waveforms Figs 4 and 5
	10		40	20		ns	
	15		30	15		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	50	25		ns	
	10		30	15		ns	
	15		20	10		ns	
Recovery time for MR	5	t_{RMR}	50	20		ns	
	10		40	15		ns	
	15		25	10		ns	
Set-up times $P_n \rightarrow CP$	5	t_{su}	40	5		ns	
	10		25	0		ns	
	15		15	0		ns	
$PE \rightarrow CP$	5	t_{su}	50	25		ns	
	10		35	15		ns	
	15		30	10		ns	
$J, \overline{K} \rightarrow CP$	5	t_{su}	55	40		ns	
	10		35	15		ns	
	15		25	10		ns	
Hold times $P_n \rightarrow CP$	5	t_{hold}	25	10		ns	
	10		20	10		ns	
	15		20	10		ns	
$PE \rightarrow CP$	5	t_{hold}	15	−5		ns	
	10		10	−5		ns	
	15		5	−5		ns	
$J, \overline{K} \rightarrow CP$	5	t_{hold}	10	−5		ns	
	10		10	0		ns	
	15		10	0		ns	
Maximum clock pulse frequency	5	f_{max}	5	10		MHz	
	10		12	25		MHz	
	15		15	30		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$20\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

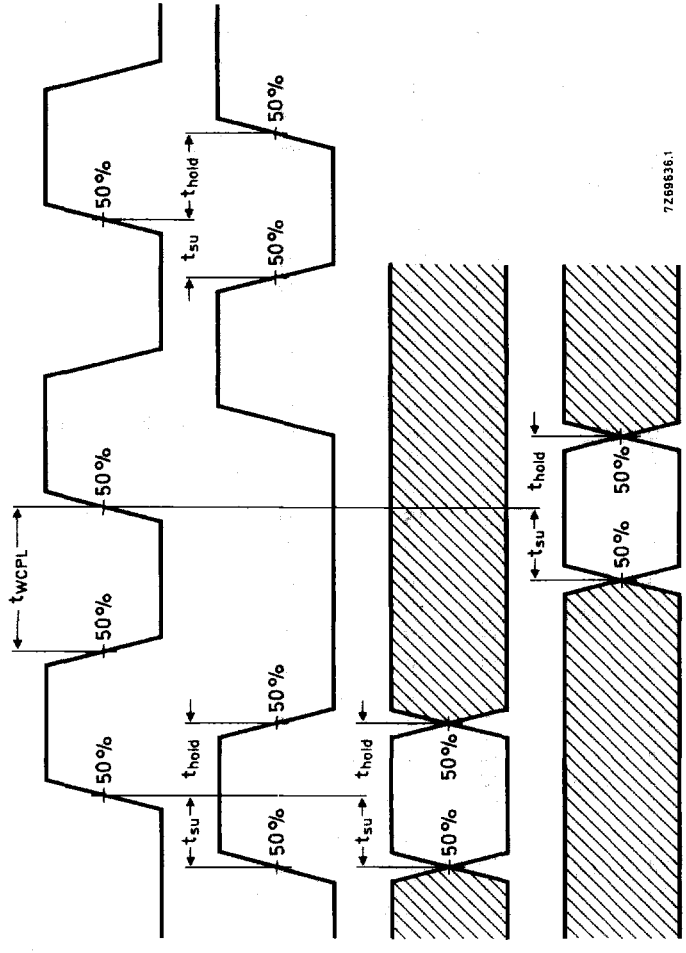

Fig. 4 Waveforms showing minimum clock pulse width, set-up times, hold times. Set-up times and hold times are shown as positive values but may be specified as negative values.

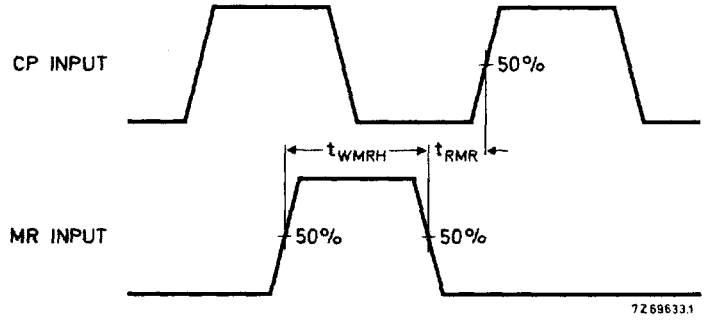

Fig. 5 Waveforms showing minimum MR pulse width and MR recovery time.

APPLICATION INFORMATION

Some examples of applications for the HEF4035B are:

- Counters, registers, arithmetic-unit registers, shift-left/shift-right registers.
- Serial-to-parallel/parallel-to-serial conversions.
- Sequence generation.
- Control circuits.
- Code conversion.

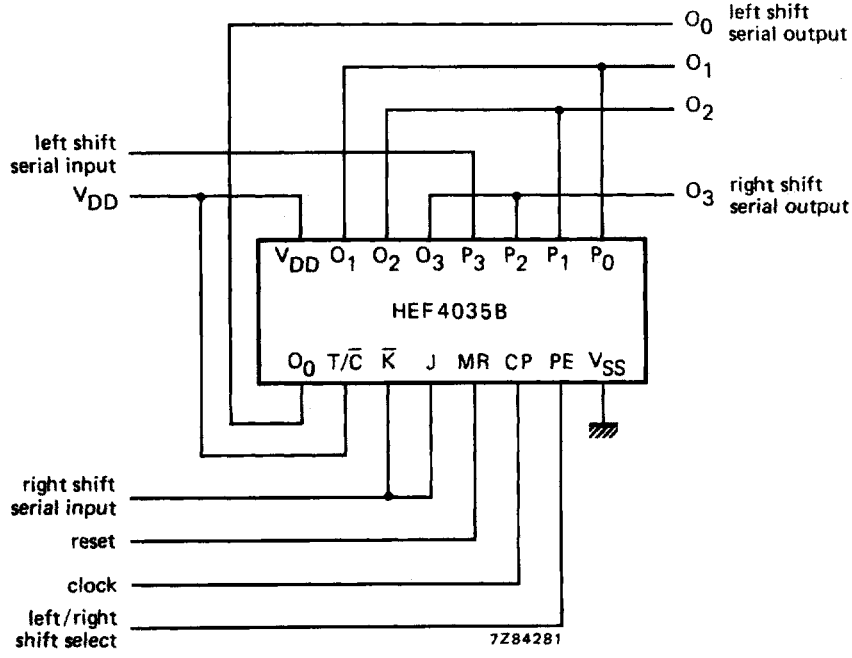

Fig. 6 Shift-left/shift-right register.