

MH1M08A0AJ-6,-7,-8/ MH1M08A0AJA-6,-7,-8

FAST PAGE MODE 8388608 - BIT(1048576 - WORD BY 8 - BIT) DYNAMIC RAM

DESCRIPTION

The MH1M08A0AJ/JA is 1048576-word $\times$ 8-bit dynamic RAM and consists of two industry standard 1M $\times$ 4 dynamic RAMs in SOJ.

The mounting of SOJ on a single in-line package provides any application where high densities and large quantities of memory are required.

FEATURES

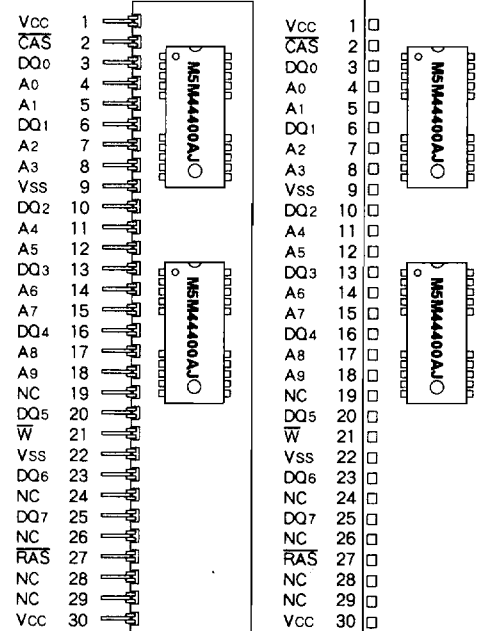
Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
MH1M08A0AJ-6 MH1M08A0AJA-6	60	120	800
MH1M08A0AJ-7 MH1M08A0AJA-7	70	140	700
MH1M08A0AJ-8 MH1M08A0AJA-8	80	160	600

- Utilizes industry standard 4M RAMs in SOJ and 1M RAM in SOJ
- 30 pins Single in-line Package
- Single +5V ($\pm 10\%$) supply operation
- Low stand by power dissipation..... 11mW(max)
- Low operation power dissipation
 - MH1M08A0AJ-6/MH1M08A0AJA-6..... 1.10W(max)
 - MH1M08A0AJ-7/MH1M08A0AJA-7..... 0.94W(max)
 - MH1M08A0AJ-8/MH1M08A0AJA-8..... 0.83W(max)
- All inputs, output TTL compatible and low capacitance
- Includes $(0.22 \mu F \times 2)$ decoupling capacitors
- 1024 refresh cycles every 16.4ms ($A_0 \sim A_9$)

APPLICATION

Main-memory unit for computers, Microcomputer memory,
Refresh memory for CRT

PIN CONFIGURATION(TOP VIEW) (Single side)



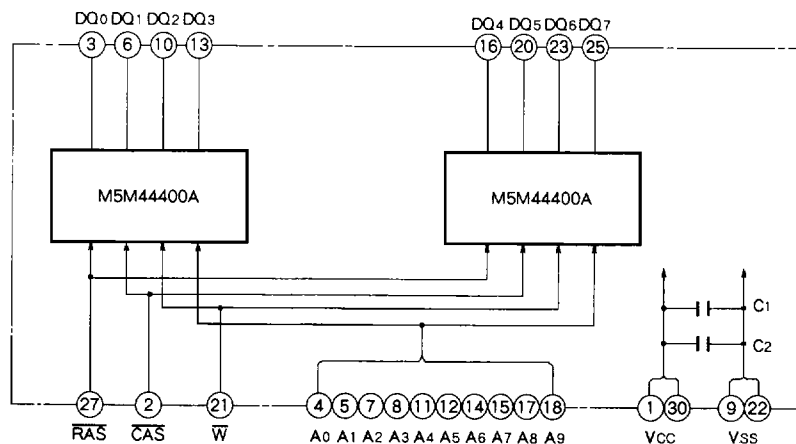
NC: NO CONNECTION

Outline

30N5F (MH1M08A0AJA)

30N9G (MH1M08A0AJ)

BLOCK DIAGRAM



MH1M08A0AJ- 6,- 7,- 8/MH1M08A0AJA- 6,- 7,- 8

FAST PAGE MODE 8388608 - BIT(1048576 - WORD BY 8 - BIT)DYNAMIC RAM

FUNCTION

The MH1M08A0AJ/JA provide, in addition to normal read, write a number of other functions, e.g., fast page mode, RAS only refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output		Refresh	Remark
	RAS	CAS	W	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
RAS-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	APD	DNC	OPN	VLD	YES	
CAS before RAS refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Stand by	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active. NAC : nonactive. DNC : don't care. VLD : valid. IVD : Invalid. APD : applied. OPN : open

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to V _{ss}	- 1~7	V
V _I	Input voltage		- 1~7	V
V _O	Output voltage		- 1~7	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a = 25 °C	2	W
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		- 40~125	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0~70 °C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{cc}	Supply voltage	4.5	5	5.5	V
V _{ss}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.5	V
V _{IL}	Low-level input voltage, all inputs	- 2.0		0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

MH1M08A0AJ- 6,- 7,- 8/MH1M08A0AJA- 6,- 7,- 8

FAST PAGE MODE 8388608 - BIT(1048576 - WORD BY 8 - BIT) DYNAMIC RAM

ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V _{OH}	High-level output voltage		I _{OH} = - 5mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage		I _{OL} = 4.2mA	0		0.4	V
I _{OZ}	Off-state output current		Q floating 0V ≤ V _{OUT} ≤ 5.5V	- 10		10	μA
I _I	Input current		0V ≤ V _{IN} ≤ 6.5V, Other inputs pins = 0V	- 10		10	μA
I _{CC1} (AV)	Average supply current from V _{CC} , operating (Note 3, 4)	MH1M08A0A-6	RAS, CAS cycling			200	mA
		MH1M08A0A-7	t _{CR} = t _{WC} = min.			170	
		MH1M08A0A-8	output open			150	
I _{CC2} (AV)	Supply current from V _{CC} , stand-by		RAS = CAS = V _{IH} , output open			4	mA
			RAS = CAS ≥ V _{CC} - 0.5			2	
I _{CC3} (AV)	Average supply current from V _{CC} , refreshing (Note 3)	MH1M08A0A-6	RAS cycling, CAS = V _{IH}			200	mA
		MH1M08A0A-7	t _{RC} = min.			170	
		MH1M08A0A-8	output open			150	
I _{CC4} (AV)	Average supply current from V _{CC} Fast-Page-Mode (Note 3, 4)	MH1M08A0A-6	RAS = V _{IL} , CAS cycling			200	mA
		MH1M08A0A-7	t _{PC} = min.			170	
		MH1M08A0A-8	output open			150	
I _{CC6} (AV)	Average supply current from V _{CC} , CAS before RAS refresh mode (Note 3)	MH1M08A0A-6	CAS before RAS refresh cycling			170	mA
		MH1M08A0A-7	t _{RC} = min.			150	
		MH1M08A0A-8	output open			130	

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1}(AV), I_{CC3}(AV) and I_{CC4}(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.4: I_{CC1}(AV) and I_{CC4}(AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta = 0~70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{I(A)}	Input capacitance, address inputs	V _i = V _{SS} f = 1MHz V _i = 25mVrms			25	pF
C _{I(W)}	Input capacitance, write control input				20	pF
C _{I(RAS)}	Input capacitance, RAS input				20	pF
C _{I(CAS)}	Input capacitance, CAS input				20	pF
C _{I/O}	Input/Output capacitance, data ports				15	pF

MH1M08A0AJ- 6, - 7, - 8/MH1M08A0AJA- 6, - 7, - 8

FAST PAGE MODE 8388608 - BIT(1048576 - WORD BY 8 - BIT)DYNAMIC RAM

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{cc} = 5\text{V} \pm 10\%$, $V_{ss} = 0\text{V}$, unless otherwise noted, See notes 5, 12, 13)

Symbol	Parameter	Limits						Unit
		MH1M08A0A-6		MH1M08A0A-7		MH1M08A0A-8		
		Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ (Note 6, 7)		15		20		20	ns
tRAC	Access time from $\overline{\text{RAS}}$ (Note 6, 8)		60		70		80	ns
tAA	Column Address access time (Note 6, 9)		30		35		40	ns
tCPA	Access time from $\overline{\text{CAS}}$ precharge (Note 6, 10)		35		40		45	ns
tCLZ	Output low impedance time from $\overline{\text{CAS}}$ low (Note 6)	5		5		5		ns
tOFF	Output disable time after $\overline{\text{CAS}}$ high (Note 11)	0	15	0	20	0	20	ns

Note 5: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh).

Note the $\overline{\text{RAS}}$ may be cycled during the initial pause. And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles are required after prolonged periods (greater than 16.4ms) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

6: Measured with a load circuit equivalent to 2TTL loads and 100pF.

7: Assumes that $\text{trCD} \geq \text{trCD}(\text{max})$ and $\text{tASC} \geq \text{tASC}(\text{max})$.

8: Assumes that $\text{trCD} \leq \text{trCD}(\text{max})$ and $\text{trAD} \leq \text{trAD}(\text{max})$. If trCD or trAD is greater than the maximum recommended value shown in this table, trAC will increase by amount that trCD or trAD exceeds the value shown.

9: Assumes that $\text{trAD} \geq \text{trAD}(\text{max})$ and $\text{tASC} \leq \text{tASC}(\text{max})$.

10: Assumes that $\text{tCP} \leq \text{tCP}(\text{max})$ and $\text{tASC} \geq \text{tASC}(\text{max})$.

11: $\text{toFF}(\text{max})$ defines the time at which the output achieves the high impedance state ($I_{\text{OUT}} \leq |\pm 10 \mu\text{A}|$) and is not reference to $V_{\text{OH}}(\text{min})$ or $V_{\text{OL}}(\text{max})$.

TIMING REQUIREMENTS (For Read, Write, Refresh, and Fast Page Cycles)

($T_a = 0 \sim 70^\circ\text{C}$, $V_{cc} = 5\text{V} \pm 10\%$, $V_{ss} = 0\text{V}$, unless otherwise noted, See notes 12, 13)

Symbol	Parameter	Limits						Unit
		MH1M08A0A-6		MH1M08A0A-7		MH1M08A0A-8		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		16.4		16.4		16.4	ms
trP	RAS high pulse width	50		60		70		ns
trCD	Delay time, RAS low to CAS low (Note 14)	20	45	20	50	20	60	ns
tCRP	Delay time, CAS high to RAS low	10		10		10		ns
trPC	Delay time, RAS high to CAS low	0		0		0		ns
tCPN	CAS high pulse width	10		10		10		ns
trAD	Column address delay time from RAS low (Note 15)	15	30	15	35	20	40	ns
tASR	Row address setup time before RAS low	0		0		0		ns
tASC	Column address setup time before CAS low (Note 16)	0	10	0	10	0	15	ns
trAH	Row address hold time after RAS low	10		10		15		ns
tCAH	Column address hold time after CAS low	15		15		20		ns
tt	Transition time (Note 17)	3	50	3	50	3	50	ns

Note 12: The timing requirements are assumed $t_T = 5\text{ns}$.

13: $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals.

14: $\text{trCD}(\text{max})$ is specified as a reference point only. If trCD is less than $\text{trCD}(\text{max})$, access time is trAC . If trCD is greater than $\text{trCD}(\text{max})$, access time is controlled exclusively by tCAC or tAA . $\text{trCD}(\text{min})$ is specified as $\text{trCD}(\text{min}) = \text{trAH}(\text{min}) + 2t_T + \text{tASC}(\text{min})$.

15: $\text{trAD}(\text{max})$ is specified as a reference point only. If $\text{trAD} \geq \text{trAD}(\text{max})$ and $\text{tASC} \leq \text{tASC}(\text{max})$, access time is controlled exclusively by tAA .

16: $\text{tASC}(\text{max})$ is specified as a reference point only. If $\text{trCD} \geq \text{trCD}(\text{max})$ and $\text{tASC} \geq \text{tASC}(\text{max})$, access time is controlled exclusively by tCAC .

17: t_T is measured between $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$.

MH1M08A0AJ- 6,- 7,- 8/MH1M08A0AJA- 6,- 7,- 8

FAST PAGE MODE 8388608 - BIT(1048576 - WORD BY 8 - BIT) DYNAMIC RAM

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		MH1M08A0A-6		MH1M08A0A-7		MH1M08A0A-8		
		Min	Max	Min	Max	Min	Max	
trc	Read cycle time	120		140		160		ns
trAS	RAS low pulse width	60	10000	70	10000	80	10000	ns
tcAS	CAS low pulse width	15	10000	20	10000	20	10000	ns
tCSH	CAS hold time after RAS low	60		70		80		ns
trSH	RAS hold time after CAS low	15		20		20		ns
trCS	Read Setup time before CAS low	0		0		0		ns
trCH	Read hold time after CAS high (Note 18)	0		0		0		ns
trRH	Read hold time after RAS high (Note 18)	10		10		10		ns
trAL	Column address to RAS hold time	30		35		40		ns

Note 18: Either trCH or trRH must be satisfied for a read cycle.

Write Cycle(Early Write)

Symbol	Parameter	Limits						Unit
		MH1M08A0A-6		MH1M08A0A-7		MH1M08A0A-8		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	120		140		160		ns
tRAS	$\overline{\text{RAS}}$ low pulse width	60	10000	70	10000	80	10000	ns
tCAS	$\overline{\text{CAS}}$ low pulse width	15	10000	20	10000	20	10000	ns
tCSH	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	60		70		80		ns
tRSH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	15		20		20		ns
tWCS	Write setup time before $\overline{\text{CAS}}$ low	0		0		0		ns
tWCH	Write hold time after $\overline{\text{CAS}}$ low	10		15		15		ns
tCWL	$\overline{\text{CAS}}$ hold time after $\overline{\text{W}}$ low	15		20		20		ns
tRWL	$\overline{\text{RAS}}$ hold time after $\overline{\text{W}}$ low	15		20		20		ns
tWP	Write pulse width	10		15		15		ns
tDS	Data setup time before $\overline{\text{CAS}}$ low or $\overline{\text{W}}$ low	0		0		0		ns
tDH	Data hold time after $\overline{\text{CAS}}$ low or $\overline{\text{W}}$ low	10		15		15		ns

Fast - Page Mode Cycle(Read, Early Write, Read - Write Cycle) (Note 19)

Symbol	Parameter	Limits						Unit
		MH1M08A0A-6		MH1M08A0A-7		MH1M08A0A-8		
		Min	Max	Min	Max	Min	Max	
tpc	Fast page mode read/write cycle time	40		45		50		ns
trās	RAS low pulse width for read write cycle (Note 20)	100	100000	115	100000	135	100000	ns
tcp	CAS high pulse width (Note 21)	10	15	10	15	10	20	ns
tcPRH	RAS hold time after CAS precharge	35		40		45		ns

Note 19: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

20: trās(min) is specified as two cycles of $\overline{\text{CAS}}$ input are performed.

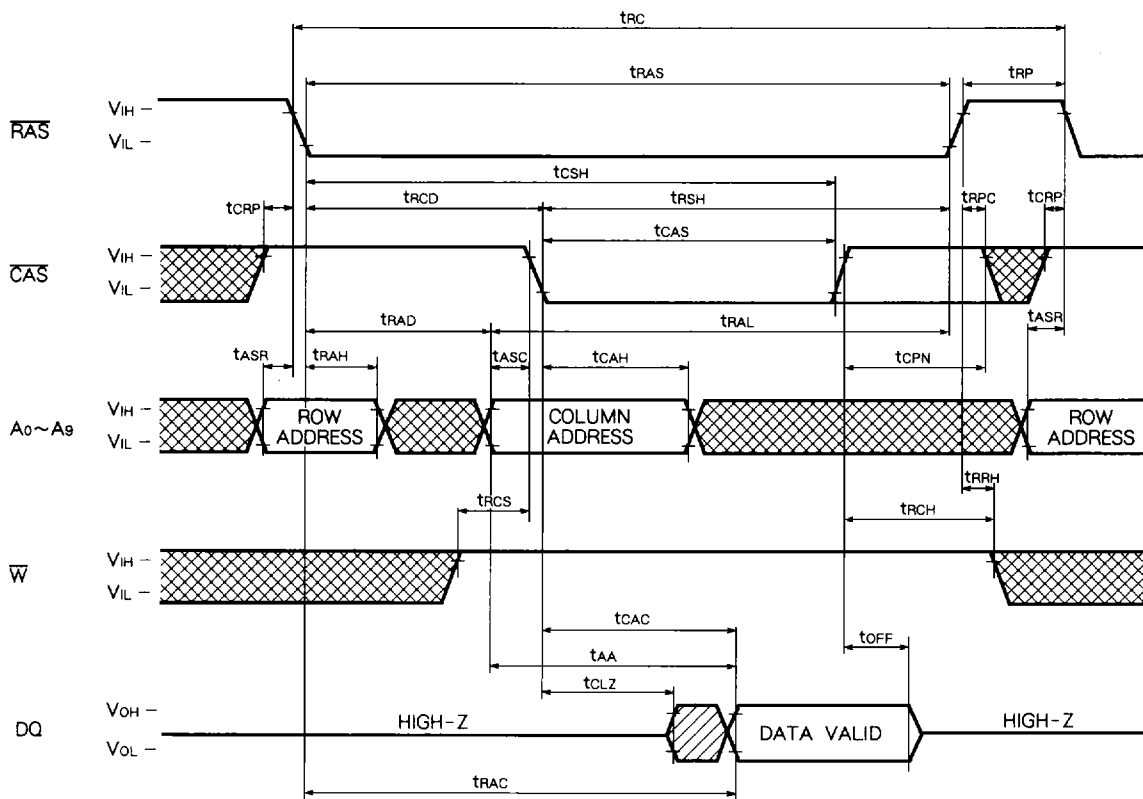
21: tcp(max) is specified as a reference point only.

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle (Note 22)

Symbol	Parameter	Limits						Unit
		MH1M08A0A-6		MH1M08A0A-7		MH1M08A0A-8		
		Min	Max	Min	Max	Min	Max	
tCSR	CAS setup time before RAS low	10		10		10		ns
tCHR	CAS hold time after RAS low	10		15		15		ns
trSR	Read setup time before RAS low	10		10		10		ns
trHR	Read hold time after RAS low	10		15		15		ns

Note 22: Eight or more $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles instead of eight $\overline{\text{RAS}}$ cycles are necessary for proper operation of $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode.

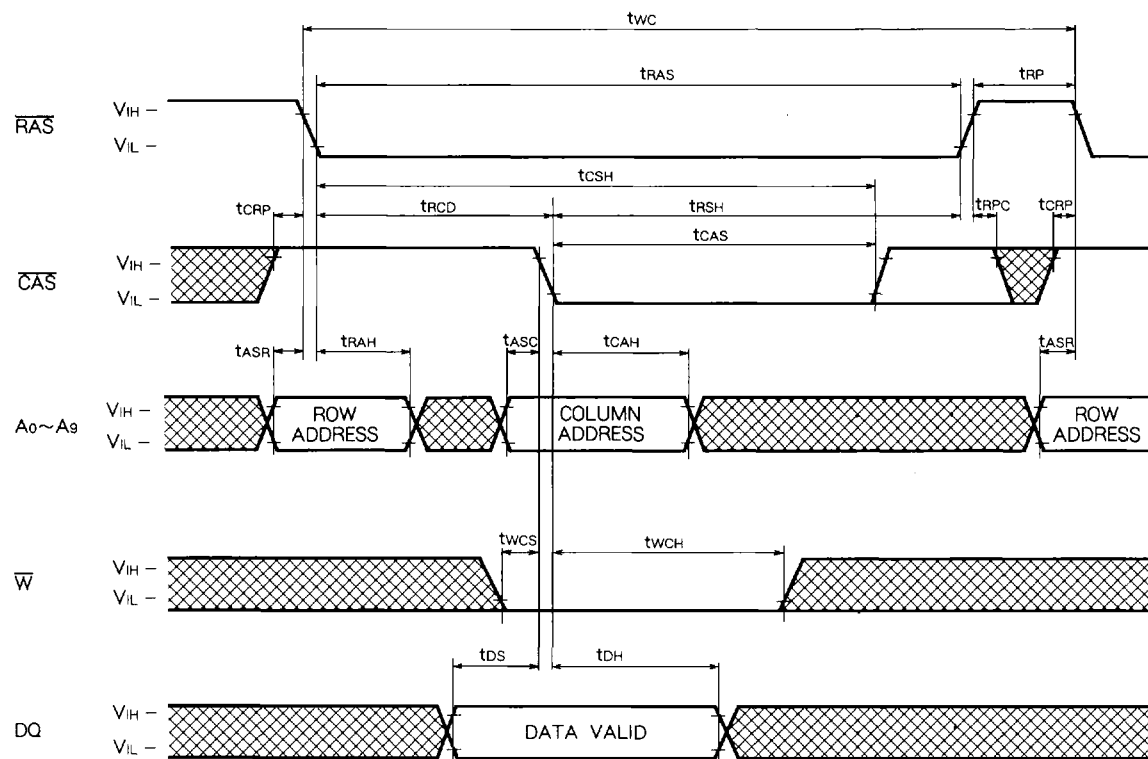
Road Cycle



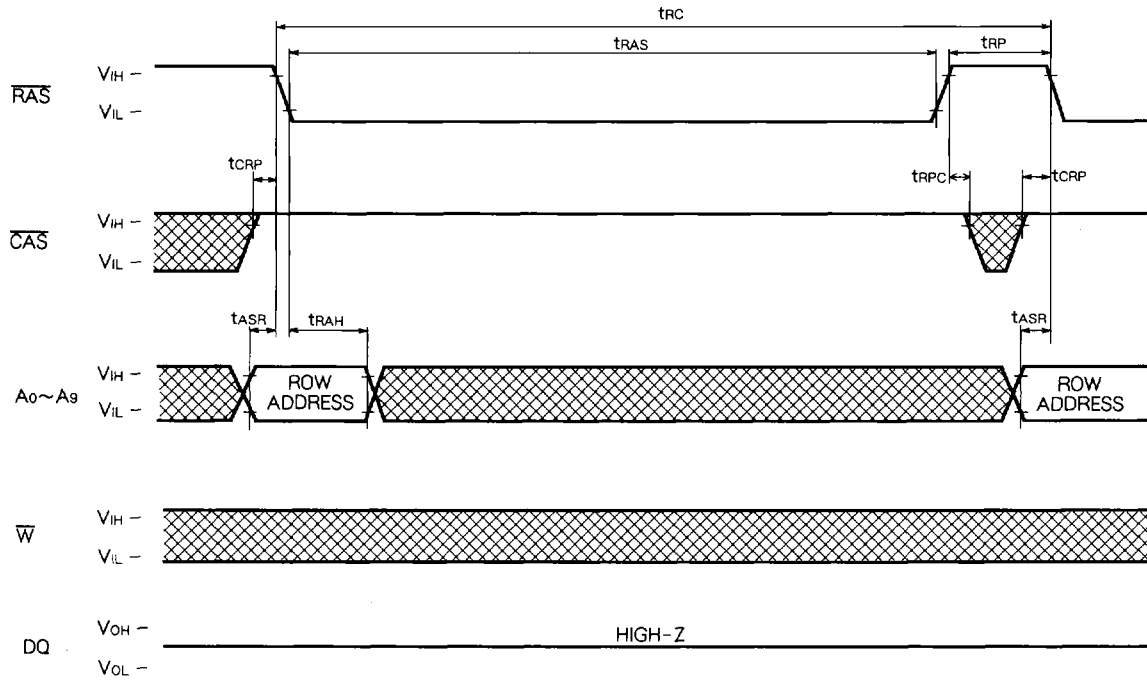
Note 23  Indicates the don't care input.

1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. 14. 15. 16. 17. 18. 19. 20. 21. 22. 23. 24. 25. 26. 27. 28. 29. 30. 31. 32. 33. 34. 35. 36. 37. 38. 39. 40. 41. 42. 43. 44. 45. 46. 47. 48. 49. 50. 51. 52. 53. 54. 55. 56. 57. 58. 59. 60. 61. 62. 63. 64. 65. 66. 67. 68. 69. 70. 71. 72. 73. 74. 75. 76. 77. 78. 79. 80. 81. 82. 83. 84. 85. 86. 87. 88. 89. 90. 91. 92. 93. 94. 95. 96. 97. 98. 99. 100. 101. 102. 103. 104. 105. 106. 107. 108. 109. 110. 111. 112. 113. 114. 115. 116. 117. 118. 119. 120. 121. 122. 123. 124. 125. 126. 127. 128. 129. 130. 131. 132. 133. 134. 135. 136. 137. 138. 139. 140. 141. 142. 143. 144. 145. 146. 147. 148. 149. 150. 151. 152. 153. 154. 155. 156. 157. 158. 159. 160. 161. 162. 163. 164. 165. 166. 167. 168. 169. 170. 171. 172. 173. 174. 175. 176. 177. 178. 179. 180. 181. 182. 183. 184. 185. 186. 187. 188. 189. 190. 191. 192. 193. 194. 195. 196. 197. 198. 199. 200. 201. 202. 203. 204. 205. 206. 207. 208. 209. 210. 211. 212. 213. 214. 215. 216. 217. 218. 219. 220. 221. 222. 223. 224. 225. 226. 227. 228. 229. 230. 231. 232. 233. 234. 235. 236. 237. 238. 239. 240. 241. 242. 243. 244. 245. 246. 247. 248. 249. 250. 251. 252. 253. 254. 255. 256. 257. 258. 259. 260. 261. 262. 263. 264. 265. 266. 267. 268. 269. 270. 271. 272. 273. 274. 275. 276. 277. 278. 279. 280. 281. 282. 283. 284. 285. 286. 287. 288. 289. 290. 291. 292. 293. 294. 295. 296. 297. 298. 299. 300. 301. 302. 303. 304. 305. 306. 307. 308. 309. 310. 311. 312. 313. 314. 315. 316. 317. 318. 319. 320. 321. 322. 323. 324. 325. 326. 327. 328. 329. 330. 331. 332. 333. 334. 335. 336. 337. 338. 339. 340. 341. 342. 343. 344. 345. 346. 347. 348. 349. 350. 351. 352. 353. 354. 355. 356. 357. 358. 359. 360. 361. 362. 363. 364. 365. 366. 367. 368. 369. 370. 371. 372. 373. 374. 375. 376. 377. 378. 379. 380. 381. 382. 383. 384. 385. 386. 387. 388. 389. 390. 391. 392. 393. 394. 395. 396. 397. 398. 399. 400. 401. 402. 403. 404. 405. 406. 407. 408. 409. 410. 411. 412. 413. 414. 415. 416. 417. 418. 419. 420. 421. 422. 423. 424. 425. 426. 427. 428. 429. 430. 431. 432. 433. 434. 435. 436. 437. 438. 439. 440. 441. 442. 443. 444. 445. 446. 447. 448. 449. 450. 451. 452. 453. 454. 455. 456. 457. 458. 459. 460. 461. 462. 463. 464. 465. 466. 467. 468. 469. 470. 471. 472. 473. 474. 475. 476. 477. 478. 479. 480. 481. 482. 483. 484. 485. 486. 487. 488. 489. 490. 491. 492. 493. 494. 495. 496. 497. 498. 499. 500. 501. 502. 503. 504. 505. 506. 507. 508. 509. 510. 511. 512. 513. 514. 515. 516. 517. 518. 519. 520. 521. 522. 523. 524. 525. 526. 527. 528. 529. 530. 531. 532. 533. 534. 535. 536. 537. 538. 539. 540. 541. 542. 543. 544. 545. 546. 547. 548. 549. 550. 551. 552. 553. 554. 555. 556. 557. 558. 559. 560. 561. 562. 563. 564. 565. 566. 567. 568. 569. 570. 571. 572. 573. 574. 575. 576. 577. 578. 579. 580. 581. 582. 583. 584. 585. 586. 587. 588. 589. 590. 591. 592. 593. 594. 595. 596. 597. 598. 599. 600. 601. 602. 603. 604. 605. 606. 607. 608. 609. 610. 611. 612. 613. 614. 615. 616. 617. 618. 619. 620. 621. 622. 623. 624. 625. 626. 627. 628. 629. 630. 631. 632. 633. 634. 635. 636. 637. 638. 639. 640. 641. 642. 643. 644. 645. 646. 647. 648. 649. 650. 651. 652. 653. 654. 655. 656. 657. 658. 659. 660. 661. 662. 663. 664. 665. 666. 667. 668. 669. 670. 671. 672. 673. 674. 675. 676. 677. 678. 679. 680. 681. 682. 683. 684. 685. 686. 687. 688. 689. 690. 691. 692. 693. 694. 695. 696. 697. 698. 699. 700. 701. 702. 703. 704. 705. 706. 707. 708. 709. 710. 711. 712. 713. 714. 715. 716. 717. 718. 719. 720. 721. 722. 723. 724. 725. 726. 727. 728. 729. 730. 731. 732. 733. 734. 735. 736. 737. 738. 739. 740. 741. 742. 743. 744. 745. 746. 747. 748. 749. 750. 751. 752. 753. 754. 755. 756. 757. 758. 759. 760. 761. 762. 763. 764. 765. 766. 767. 768. 769. 770. 771. 772. 773. 774. 775. 776. 777. 778. 779. 780. 781. 782. 783. 784. 785. 786. 787. 788. 789. 790. 791. 792. 793. 794. 795. 796. 797. 798. 799. 800. 801. 802. 803. 804. 805. 806. 807. 808. 809. 810. 811. 812. 813. 814. 815. 816. 817. 818. 819. 820. 821. 822. 823. 824. 825. 826. 827. 828. 829. 830. 831. 832. 833. 834. 835. 836. 837. 838. 839. 840. 84

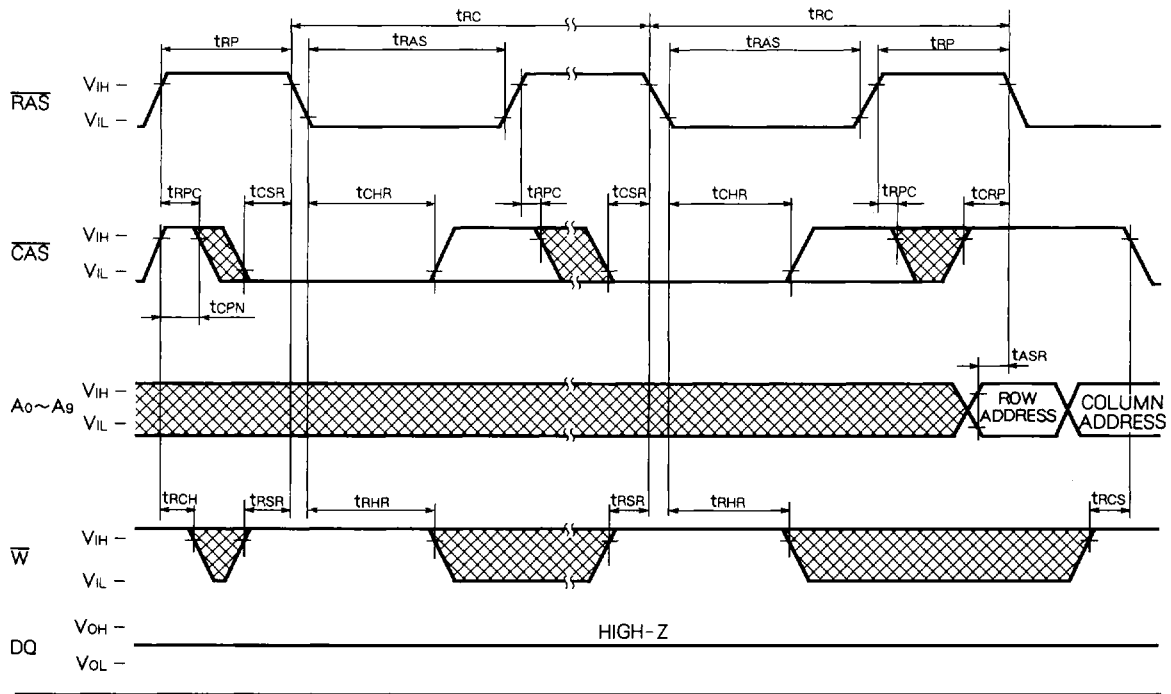
Write Cycle(Early Write)



$\overline{\text{RAS}}$ only Refresh Cycle



$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle



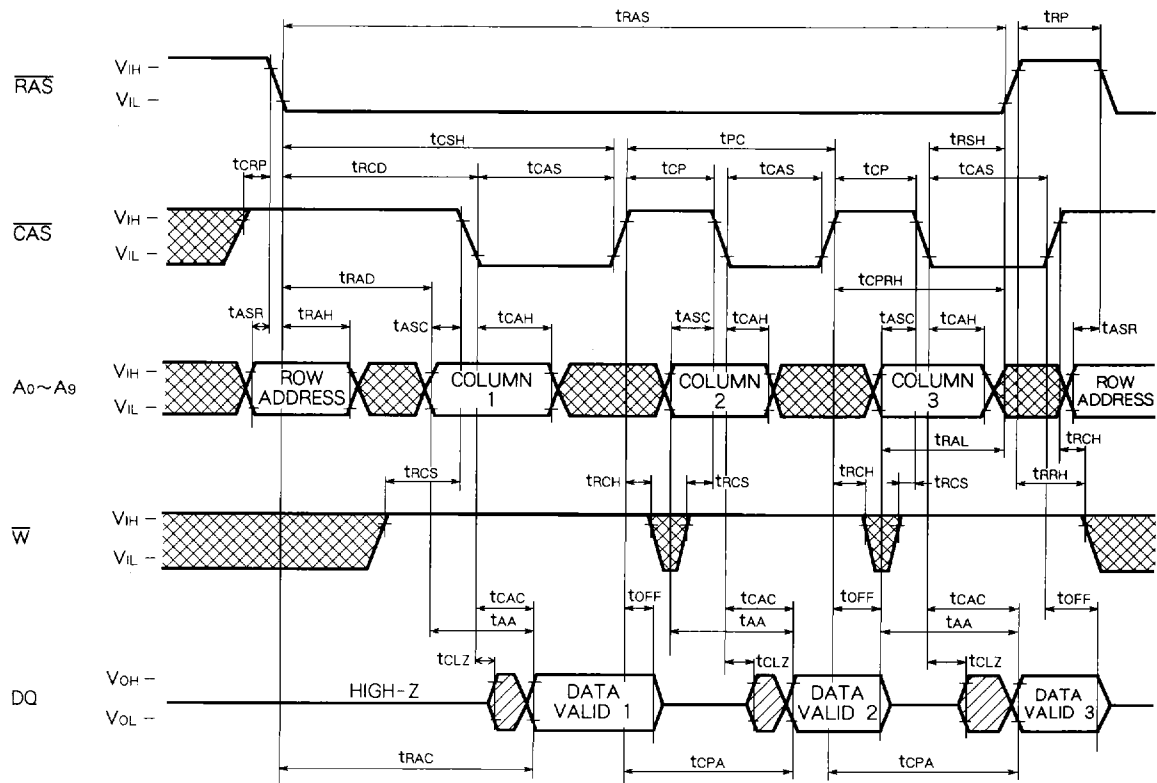
Hidden Refresh Cycle(Read)



MH1M08A0AJ- 6,- 7,- 8/MH1M08A0AJA- 6,- 7,- 8

FAST PAGE MODE 8388608 - BIT(1048576 - WORD BY 8 - BIT)DYNAMIC RAM

Fast-Page-Mode Read Cycle



MH1M08A0AJ- 6,- 7,- 8/MH1M08A0AJA- 6,- 7,- 8

FAST PAGE MODE 8388608 - BIT(1048576 - WORD BY 8 - BIT) DYNAMIC RAM

Fast - Page - Mode Early Write Cycle

