# Document Title

## Multi-Chip Package MEMORY

**128M Bit (8Mx16) Nand Flash Memory / 64M Bit (4Mx16) U*t*RAM / 32M Bit (2Mx16) U*t*RAM / 8M Bit (*512Kx16*) SRAM**

# Revision History

| Revision No. | History | Draft Date | Remark |
|---|---|---|---|
| 0.0 | Initial draft. | November 22, 2002 | Preliminary |
| 1.0 | Finalize<br><NAND Flash><br>- Correct the some minor mis-spelling<br><64M UtRAM><br>- Changed Power Up sequence and Wake Up sequence<br><SRAM><br>- Changed operation current(Max)- $I_{CC2}$ from 40mA to 35mA | May 20. 2003 | Final |
| 1.1 | <NAND><br>- Corrected the FLASH READ1 OPERATION(READ ONE PAGE) timing in Page 24. | October 28. 2003 | Final |

Note : For more detailed features and specifications including FAQ, please refer to Samsung's web site.
http://samsungelectronics.com/semiconductors/products/products_index.html

## *Multi-Chip Package MEMORY*

**128M Bit (8Mx16) Nand Flash Memory / 64M Bit (4Mx16) U*t*RAM / 32M Bit (2Mx16) U*t*RAM / 8M Bit (*512Kx16*) SRAM**

## FEATURES

- Power Supply Voltage
  - Flash : 2.7 ~ 3.1V
  - U*t*RAM(32M, 64M) : 2.7 ~ 3.1V
  - SRAM : 2.7 ~ 3.1V
- Organization
  - Flash : (8M + 256K)bit x 16bit
  - U*t*RAM(64M) : 4M x 16 bit
  - U*t*RAM(32M) : 2M x 16 bit
  - SRAM : 512K x 16 bit
- Access Time
  - Flash : Random Access : 10us(Max.),
    Serial Page Access : 50ns(Min.)
  - U*t*RAM(64M) : 70ns
  - U*t*RAM(32M) : 85ns
  - SRAM : 55ns
- Power Consumption (typical value)
  - Flash Read Current : 10 mA(@20MHz)
    Program/Erase Current : 10 mA
    Standby Current : 10 μA
  - U*t*RAM(64M) Operating Current : 35mA
    Standby Current : 80μA
  - U*t*RAM(32M) Operating Current : 30mA
    Standby Current : 80μA
  - SRAM Operating Current : 30mA
    Standby Current : 0.5μA
- Flash Automatic Program and Erase
  Page Program : (256 + 8)Word
  Block Erase : (8K + 256)Word
- Flash Fast Write Cycle Time
  Program time : 200us(Typ.)
  Block Erase Time : 2ms(Typ.)
- U*t*RAM Support Deep Power Down : Memory cell data holds invalid
- SRAM Low Data Retention Voltage : 1.5V(Min.)
- Flash Endurance : 100,000 Program/Erase Cycles Minimum
- Flash Data Retention : 10 years
- Operating Temperature : -25°C ~ 85°C
- Package : 87 - ball TBGA Type - 10 x 12mm, 0.8 mm pitch

## GENERAL DESCRIPTION

The KBC00A6A0M is a Multi Chip Package Memory which combines 128Mbit Nand Flash and 64Mbit Unit Transistor CMOS RAM and 32Mbit Unit Transistor CMOS RAM and 8Mbit SRAM.

128Mbit NAND Flash memory is organized as 8M x16 bit and 64Mbit U*t*RAM is organized as 4M x16 bit and 32Mbit U*t*RAM is organized as 2M x16 bit and 8Mbit SRAM is organized as 512K x16 bit. In 128Mb NAND Flash a 264-word page program can be typically achieved within 200us and an 8K-word block erase can be typically achieved within 2ms. In serial read operation, a word can be read by 50ns. DQ Pins serve as the ports for address and data input/output as well as command inputs. Even the write-intensive systems can take advantage of the FLASH′s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. These algorithms have been implemented in many mass storage applications.

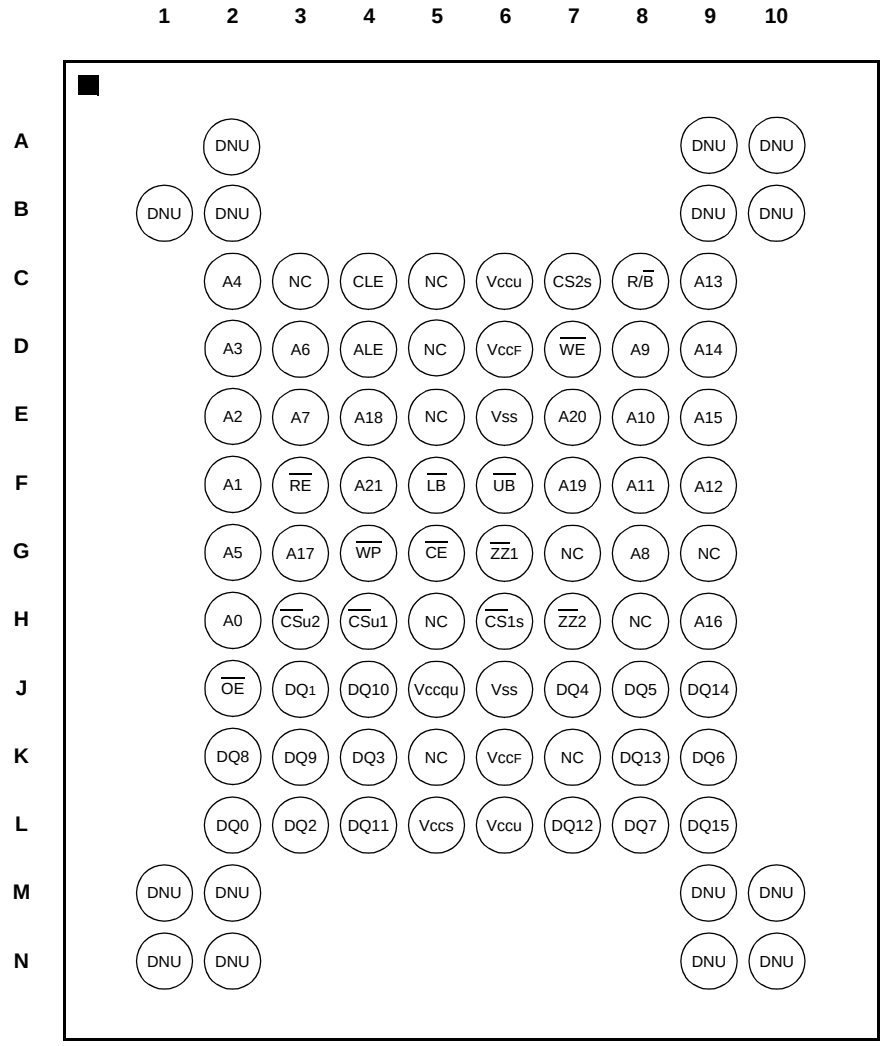
The 64Mbit(32Mbit) U*t*RAM is fabricated by SAMSUNG′s advanced CMOS technology using one transistor memory cell. The device supports deep power down mode for low standby current.

The 8Mbit SRAM is fabricated by SAMSUNG′s advanced full CMOS process technology. The device supports low data retention voltage for battery back-up operation with low data retention current.

The KBC00A6A0M is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption.

This device is available in 87-ball TBGA Type.

## PIN CONFIGURATION




**87-TBGA: Top View (Ball Down)**

## PIN DESCRIPTION

| Ball Name | Description | Ball Name | Description |
|---|---|---|---|
| $A_0$ to $A_{18}$ | Address Input Balls (U*t*RAM1,U*t*RAM2,SRAM) | R/$\overline{B}$ | Ready/Busy (Flash Memory) |
| $A_{19}$ to $A_{20}$ | Address Input Balls (U*t*RAM1, U*t*RAM2) | $\overline{ZZ}$1 | Deep Power Down (U*t*RAM1) |
| $A_{21}$ | Address Input Balls (U*t*RAM1) | $\overline{ZZ}$2 | Deep Power Down (U*t*RAM2) |
| $DQ_0$ to $DQ_{15}$ | Data Input/Output Balls (Common) | $\overline{CE}$ | Chip Enable (Flash Memory) |
| $\overline{WP}$ | Write Protection (Flash Memory) | $\overline{CS}$u1 | Chip Select (U*t*RAM1) |
| $V_{CCF}$ | Power Supply (Flash Memory) | $\overline{CS}$u2 | Chip Select (U*t*RAM2) |
| Vccu | Power Supply (U*t*RAM1,U*t*RAM2) | $\overline{CS}$1s | Chip Select (SRAM) |
| Vccs | Power Supply (SRAM) | CS2s | Chip Select (SRAM) |
| Vccqu | Data Out Power (U*t*RAM1,U*t*RAM2) | $\overline{WE}$ | Write Enable (Common) |
| Vss | Ground (Common) | $\overline{OE}$ | Output Enable (U*t*RAM1,U*t*RAM2, SRAM) |
| $\overline{UB}$ | Upper Byte Enable (U*t*RAM1,U*t*RAM2, SRAM) | $\overline{RE}$ | Read Enable (Flash Memory) |
| $\overline{LB}$ | Lower Byte Enable (U*t*RAM1,U*t*RAM2, SRAM) | NC | No Connection |
| ALE | Address Latch Enable (Flash Memory) | DNU | Do Not Use |
| CLE | Command Latch Enable (Flash Memory) | | |

1. U*t*RAM1: 64Mbit U*t*RAM,
   U*t*RAM2: 32Mbit U*t*RAM

## ORDERING INFORMATION

**K B C 00 A 6 A 0 M - T 403**

**Samsung**
**MCP(4 Chip) Memory**

**Device Type**
NAND Flash+U*t*RAM+U*t*RAM
+SRAM

**NOR Flash Density , Vcc , Org.**
**00 :** NONE

**NAND Flash Density , Vcc , Org.**
**A :** 128Mbit, 3.0V, x16

**U*t*RAM Density , Vcc/Vccq , Org.**
**6 :** 64Mbit+32Mbit, 3.0V/3.0V, x16

**Access Time**
**403 :** NAND Flash: 50ns
U*t*RAM(64Mbit): 70ns
U*t*RAM(32Mbit): 85ns
SRAM: 55ns

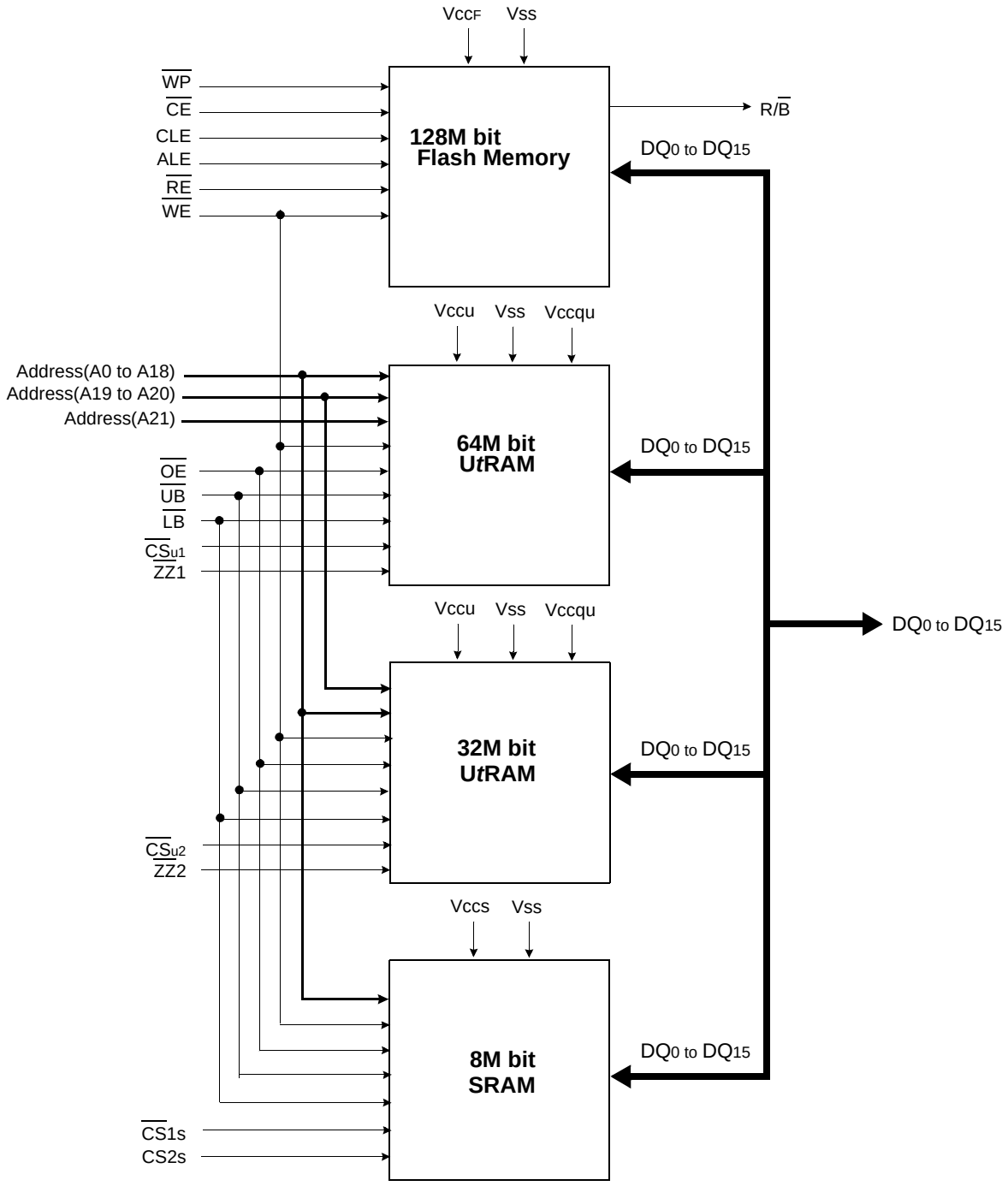
**Package**
**T :** TBGA

**Version**
**M :** 1st Generation

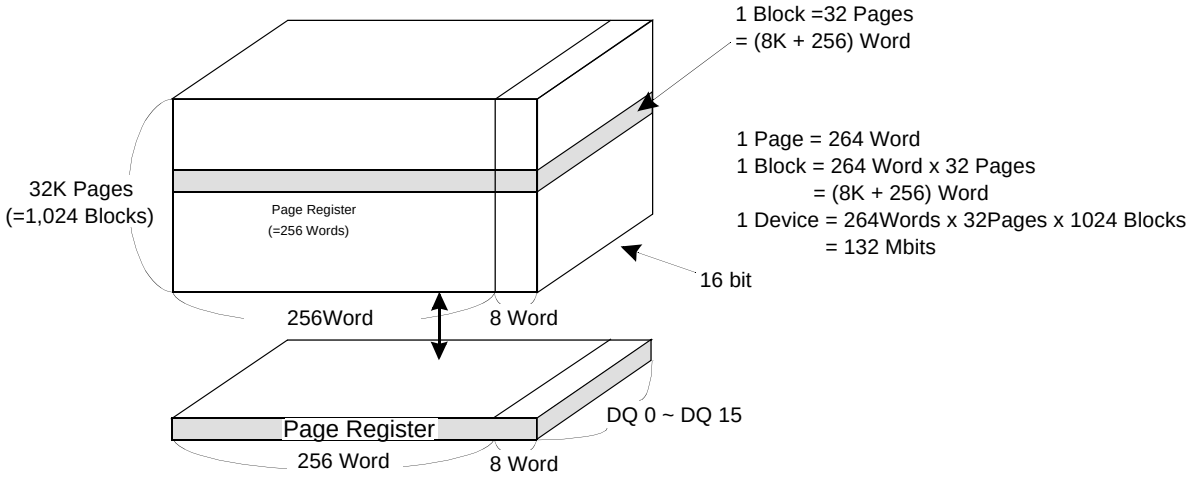
**SDRAM Density , Vcc , Org.**
**0 :** NONE

**SRAM Density , Vcc , Org.**
**A :** 8Mbit, 3.0V, x16

**Figure 1. FUNCTIONAL BLOCK DIAGRAM**



## Figure 2. Flash ARRAY ORGANIZATION




| | DQ 0 | DQ 1 | DQ 2 | DQ 3 | DQ 4 | DQ 5 | DQ 6 | DQ 7 | DQ8 to 15 | |
|---|---|---|---|---|---|---|---|---|---|---|
| 1st Cycle | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | L* | **Column Address** |
| 2nd Cycle | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_{16}$ | L* | **Row Address (Page Address)** |
| 3rd Cycle | $A_{17}$ | $A_{18}$ | $A_{19}$ | $A_{20}$ | $A_{21}$ | $A_{22}$ | $A_{23}$ | L* | L* | |

**NOTE** : Column Address : Starting Address of the Register.

* L must be set to "Low".

## NAND FLASH PRODUCT INTRODUCTION

The NAND Flash Memory is a 132Mbit(138,412,032 bit) memory organized as 32,768 rows(pages) by 264 columns. Spare eight columns are located from column address of 256~263. A 264-word data register is connected to memory cell arrays accommodating data transfer between the DQ buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected like NAND structure. Each of the 16 cells resides in a different page. A block consists of the 32 pages formed by one NAND structures, totaling 8448 NAND structures of 16 cells. The array organization is shown in Figure 2. Program and read operations are executed on a page basis, while erase operation is executed on a block basis. The memory array consists of 1024 blocks, and a block is separately erasable by 8K-Word unit. It indicates that the bit by bit erase operation is prohibited on the NAND Flash Memory.

The NAND Flash Memory has addresses multiplexed with lower 8 DQ′s. The NAND Flash allows sixteen bit wide data transport into and out of page registers. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through DQ′s by bringing WE to low while CE is low. Data is latched on the rising edge of WE. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the DQ pins. All commands require one bus cycle except Page Program command and Block Erase command which require two cycles: one cycle for setup and another for execution. The 32K-word physical space requires 24 addresses, thereby requiring three cycles for word-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following required command input. In Block Erase operation, however, only two row address cycles are used. Device operations are selected by writing specific commands into command register. Table 1 defines the specific commands of the Flash Memory.

### Table 1. COMMAND SETS

| Function | 1st. Cycle | 2nd. Cycle | Acceptable Command during Busy |
|---|---|---|---|
| Read 1 | 00h | - | |
| Read 2 | 50h | - | |
| Read ID | 90h | - | |
| Reset | FFh | - | O |
| Page Program | 80h | 10h | |
| Block Erase | 60h | D0h | |
| Read Status | 70h | - | O |

Caution : Any undefined command inputs are prohibited except for above command set of Table1.

## Table 2. FLASH MEMORY OPERATIONS TABLE

| CLE | ALE | $\overline{CE}$ | $\overline{WE}$ | $\overline{RE}$ | $\overline{WP}$ | Mode | |
|---|---|---|---|---|---|---|---|
| H | L | L | ⌐↑ | H | X | Read Mode | Command Input |
| L | H | L | ⌐↑ | H | X | | Address Input(3clock) |
| H | L | L | ⌐↑ | H | H | Write Mode | Command Input |
| L | H | L | ⌐↑ | H | H | | Address Input(3clock) |
| L | L | L | ⌐↑ | H | H | Data Input | |
| L | L | L | H | ↓⌐ | X | Data Output | |
| X | X | X | X | H | X | During Read(Busy) | |
| X | X | X | X | X | H | During Program(Busy) | |
| X | X | X | X | X | H | During Erase(Busy) | |
| X | X(1) | X | X | X | L | Write Protect | |
| X | X | H | X | X | 0V/VCC(2) | Stand-by | |

**NOTE:** 1. X can be $V_{IL}$ or $V_{IH}$.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

## Table 3. U*t*RAM OPERATIONS TABLE

| $\overline{CS_U}$ | $\overline{ZZ}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | $DQ_{0\sim7}$ | $DQ_{8\sim15}$ | Mode | Power |
|---|---|---|---|---|---|---|---|---|---|
| H | H | X1) | X1) | X1) | X1) | High-Z | High-Z | Deselected | Standby |
| X1) | L | X1) | X1) | X1) | X1) | High-Z | High-Z | Deselected | Deep Power Down |
| L | H | X1) | X1) | H | H | High-Z | High-Z | Deselected | Standby |
| L | H | H | H | L | X1) | High-Z | High-Z | Output Disabled | Active |
| L | H | H | H | X1) | L | High-Z | High-Z | Output Disabled | Active |
| L | H | L | H | L | H | Dout | High-Z | Lower Byte Read | Active |
| L | H | L | H | H | L | High-Z | Dout | Upper Byte Read | Active |
| L | H | L | H | L | L | Dout | Dout | Word Read | Active |
| L | H | X1) | L | L | H | Din | High-Z | Lower Byte Write | Active |
| L | H | X1) | L | H | L | High-Z | Din | Upper Byte Write | Active |
| L | H | X1) | L | L | L | Din | Din | Word Write | Active |

1. X means $V_{IL}$ or $V_{IH}$.

## Table 4. SRAM OPERATIONS TABLE

| $\overline{CS_{1s}}$ | $CS_{2s}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | $DQ_{0\sim7}$ | $DQ_{8\sim15}$ | Mode | Power |
|---|---|---|---|---|---|---|---|---|---|
| H | X1) | X1) | X1) | X1) | X1) | High-Z | High-Z | Deselected | Standby |
| X1) | L | X1) | X1) | X1) | X1) | High-Z | High-Z | Deselected | Standby |
| X1) | X1) | X1) | X1) | H | H | High-Z | High-Z | Deselected | Standby |
| L | H | H | H | L | X1) | High-Z | High-Z | Output Disabled | Active |
| L | H | H | H | X1) | L | High-Z | High-Z | Output Disabled | Active |
| L | H | L | H | L | H | Dout | High-Z | Lower Byte Read | Active |
| L | H | L | H | H | L | High-Z | Dout | Upper Byte Read | Active |
| L | H | L | H | L | L | Dout | Dout | Word Read | Active |
| L | H | X1) | L | L | H | Din | High-Z | Lower Byte Write | Active |
| L | H | X1) | L | H | L | High-Z | Din | Upper Byte Write | Active |
| L | H | X1) | L | L | L | Din | Din | Word Write | Active |

1. X means $V_{IL}$ or $V_{IH}$.

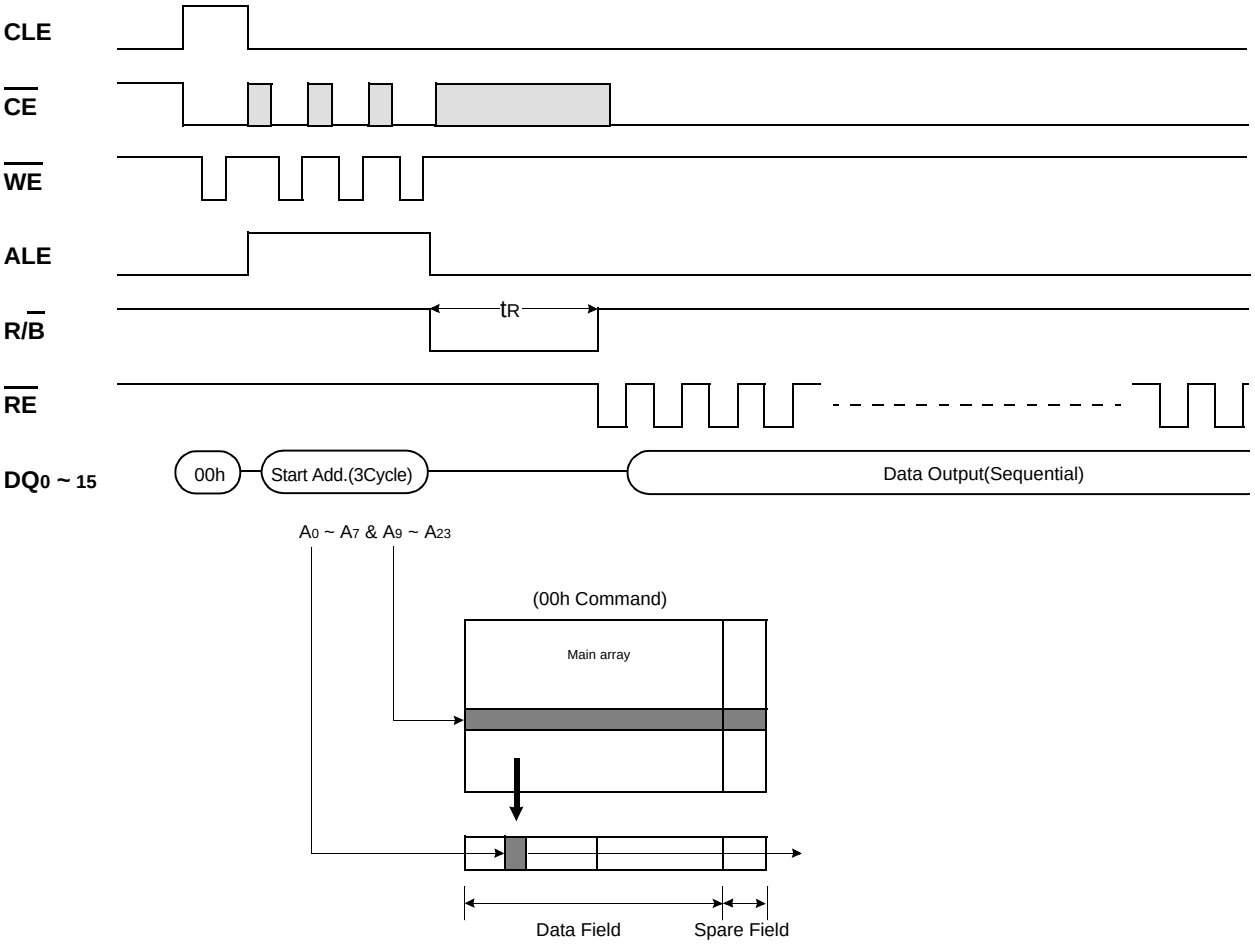
## FLASH MEMORY OPERATION

### PAGE READ

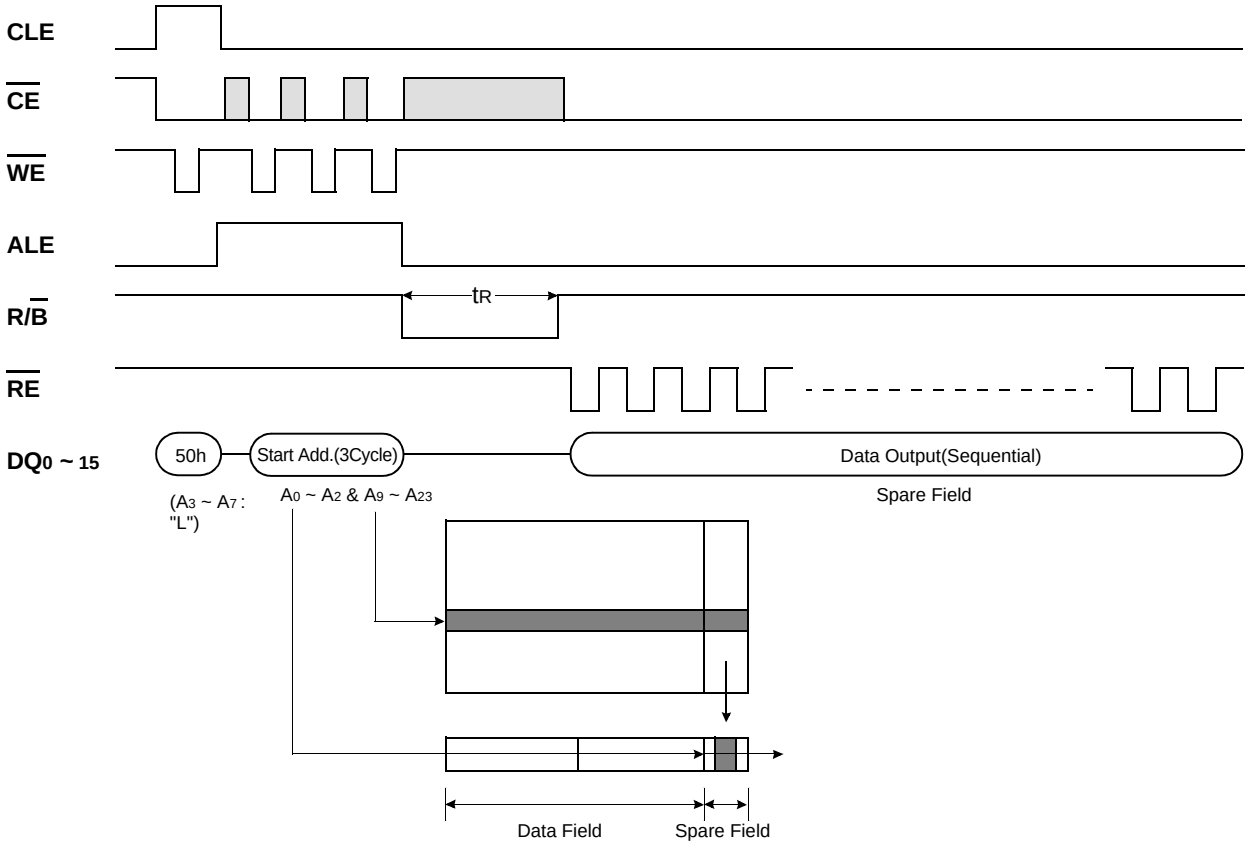
Upon initial device power up, the device status defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Two types of operation are available : random read, serial page read. The random read mode is enabled when the page address is changed. The 264 words of data within the selected page are transferred to the data registers in less than 10μs(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing $\overline{RE}$. High to low transitions of the $\overline{RE}$ clock output the data starting from the selected column address up to the last column address.

The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area(256 to 263 words) may be selectively accessed by writing the Read2 command. Addresses $A_0$ to $A_2$ set the starting address of spare area while addresses $A_3$~$A_7$ must be "L". Read1 command(00h) is needed to move the pointer back to the main area. Figures 3, 4 show typical sequence and timings for each read operation.

**Figure 3. Read1 Operation**



## Figure 4. Read2 Operation

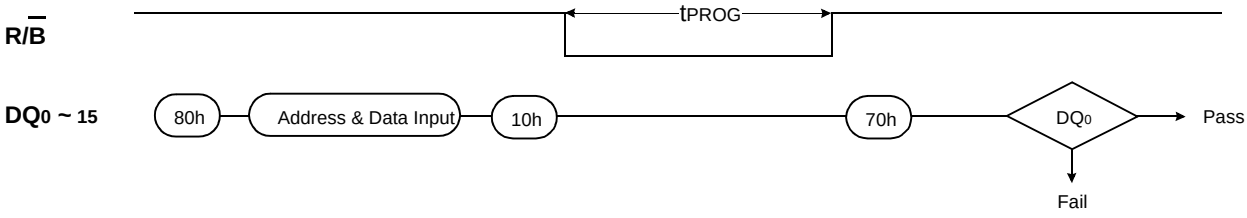



## PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programing of a byte/word or consecutive bytes/words up to 264(X16 device), in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation should not exceed 2 for main array and 3 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 264 words of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. About the pointer operation, please refer to the attached technical notes.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the three cycle address input and then serial data loading. The words other than those to be programmed do not need to be loaded.The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with RE and CEn low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/Bn output, or the Status bit(DQ 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(DQ 0) may be checked(Figure 5). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

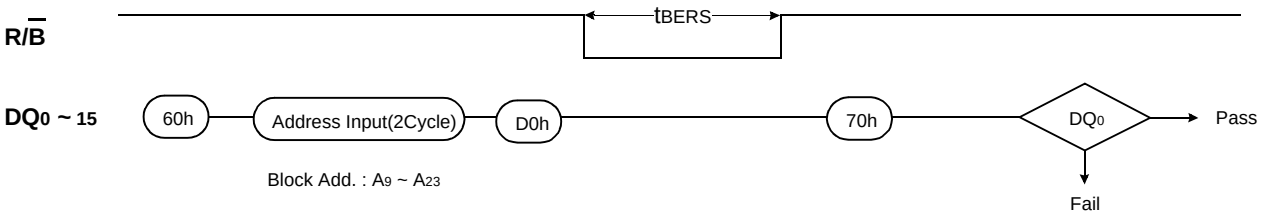
## Figure 5. Program & Read Status Operation



## BLOCK ERASE

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address $A_{14}$ to $A_{23}$ is valid while $A_9$ to $A_{13}$ is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(DQ 0) may be checked. Figure 6 details the sequence.

### Figure 6. Block Erase Operation




## READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to command register, a read cycle outputs the content of the Status Register to the DQ pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 5 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

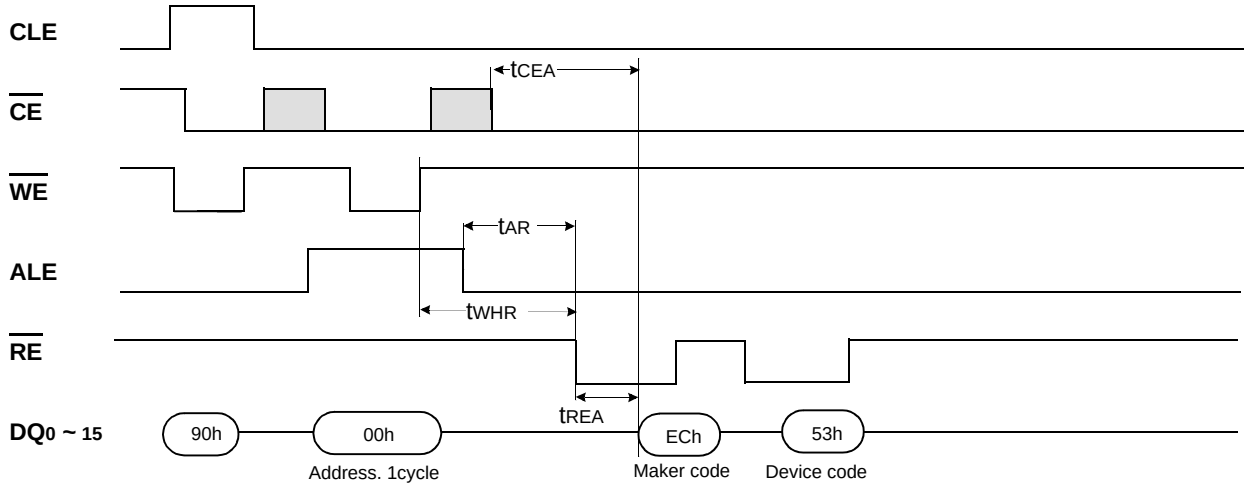
### Table 5. Read Status Register Definition

| DQ # | Status | Definition |
|---|---|---|
| $DQ_0$ | Program / Erase | "0" : Successful Program / Erase |
| | | "1" : Error in Program / Erase |
| $DQ_1$ | Reserved for Future Use | "0" |
| $DQ_2$ | | "0" |
| $DQ_3$ | | "0" |
| $DQ_4$ | | "0" |
| $DQ_5$ | | "0" |
| $DQ_6$ | Device Operation | "0" : Busy "1" : Ready |
| $DQ_7$ | Write Protect | "0" : Protected "1" : Not Protected |
| $DQ_{8\sim15}$ | Not use | Don't care |

## READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECh), and the device code (53h) respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 7 shows the operation sequence.

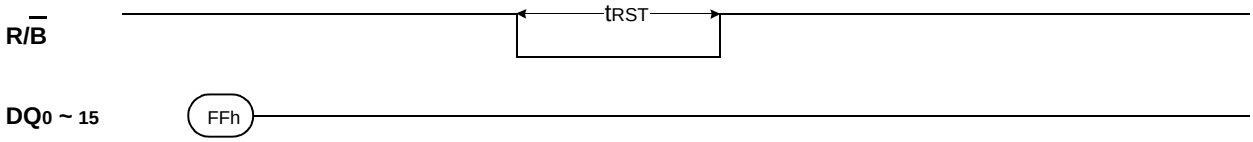
### Figure 7. Read ID Operation




## RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 6 for device status after reset operation. If the device is already in reset state, new reset command will not be accepted by the command register. The R/B pin transitions to low for tRST after the Reset command is written. Reset command is not necessary for normal operation. Refer to Figure 8 below.

### Figure 8. RESET Operation




### Table 6. Device Status

| | After Power-up | After Reset |
|---|---|---|
| Operation Mode | Read 1 | Waiting for next command |

## READY/BUSY

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 9). Its value can be determined by the following guidance.

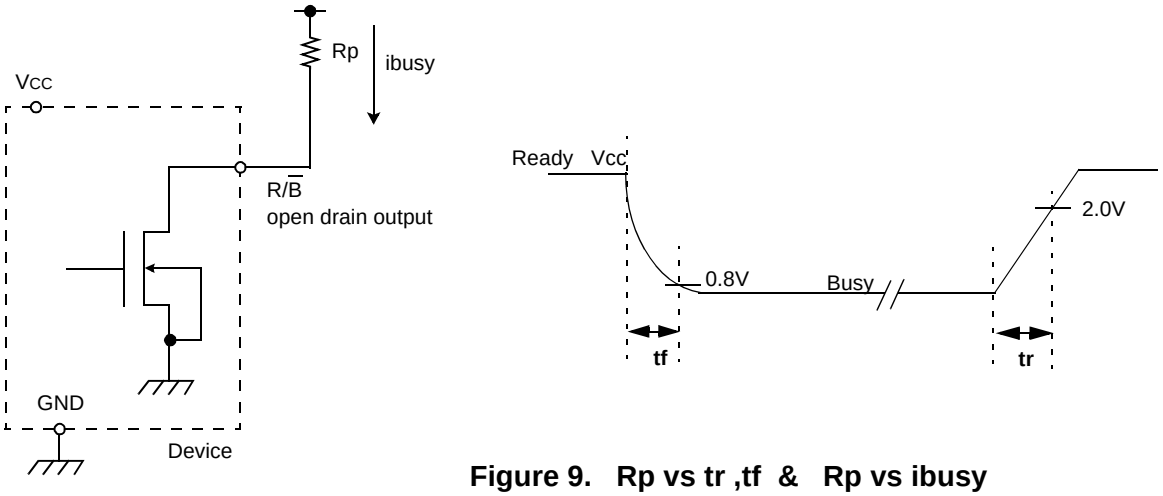
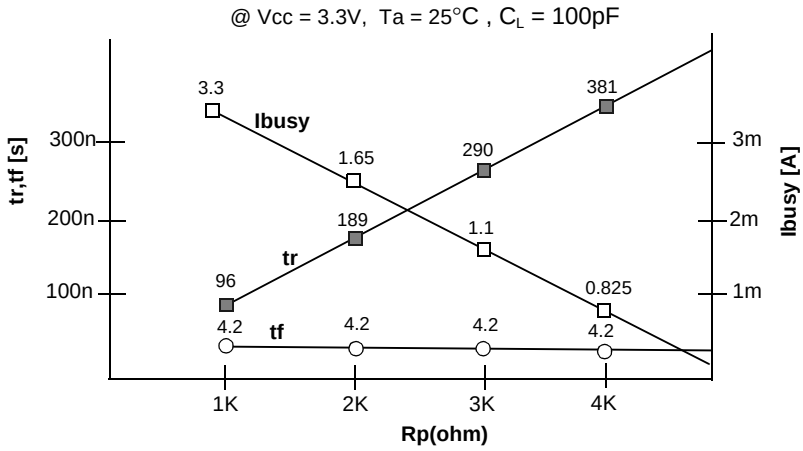



**Figure 9. Rp vs tr ,tf & Rp vs ibusy**




**Rp value guidance**

$$Rp = \frac{Vcc(Max.) - VOL(Max.)}{IOL + \Sigma IL} = \frac{2.7V}{8mA + \Sigma IL}$$

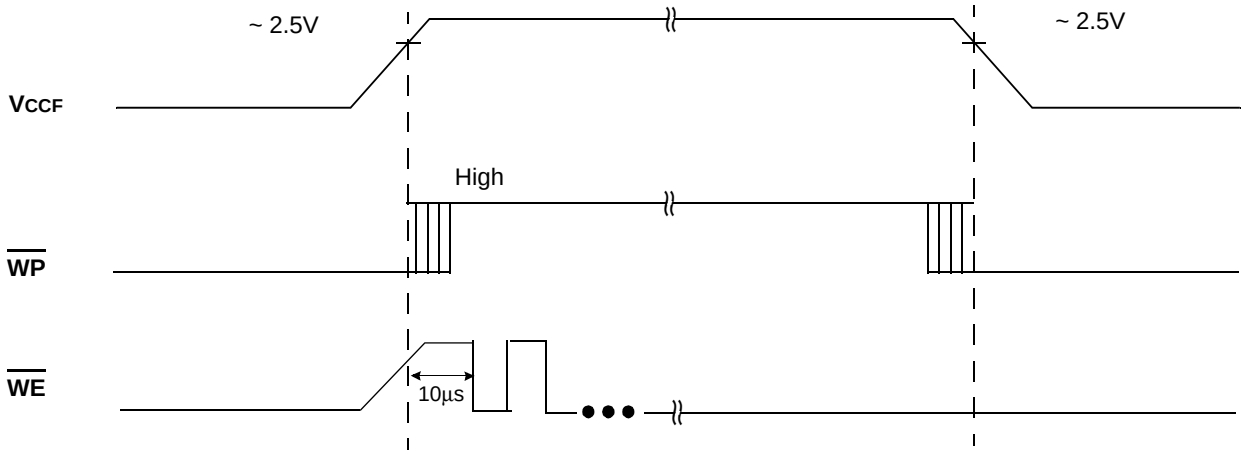
where $I_L$ is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

## Data Protection & Powerup sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.3V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at $V_{IL}$ during power-up and power-down and recovery time of minimum 10μs is required before internal circuit gets ready for any command sequences as shown in Figure 10. The two step command sequence for program/erase provides additional software protection.

### Figure 10. AC Waveforms for Power Transition



## Flash ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN/OUT}$ | -0.6 to + 4.6 | V |
| | $V_{CC}$ | -0.6 to + 4.6 | |
| Temperature Under Bias | $T_{BIAS}$ | -40 to +125 | °C |
| Operating Temperature | $T_A$ | -25 to +85 | °C |
| Storage Temperature | $T_{STG}$ | -65 to +150 | °C |

**NOTE:**

1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is $V_{CC}$,+0.3V which, during transitions, may overshoot to $V_{CC}$+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## U*t*RAM ABSOLUTE MAXIMUM RATINGS[1)]

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Voltage on any pin relative to Vss | $V_{IN}$, $V_{OUT}$ | -0.2 to $V_{CC}$+0.3V | V |
| Voltage on Vcc supply relative to Vss | $V_{CC}$ | -0.2 to 3.6V | V |
| Power Dissipation | $P_D$ | 1.0 | W |
| Operating Temperature | $T_A$ | -25 to 85 | °C |
| Storage temperature | $T_{STG}$ | -65 to 150 | °C |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

## SRAM ABSOLUTE MAXIMUM RATINGS[1)]

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Voltage on any pin relative to Vss | $V_{IN}$, $V_{OUT}$ | -0.5 to $V_{CC}$+0.3V | V |
| Voltage on Vcc supply relative to Vss | $V_{CC}$ | -0.3 to 3.6 | V |
| Power Dissipation | $P_D$ | 1.0 | W |
| Operating Temperature | $T_A$ | -25 to 85 | °C |
| Storage temperature | $T_{STG}$ | -65 to 150 | °C |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

## Flash/UtRAM/SRAM RECOMMENDED OPERATING CONDITIONS ($T_A$=-25 to 85°C)

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 2.7 | 2.9 | 3.1 | V |
| Ground | $V_{SS}$ | 0 | 0 | 0 | V |

## Flash DC AND OPERATING CHARACTERISTICS(Recommended operating conditions)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input Leakage Current | | $I_{LI}$ | $V_{IN}$=0 to Vcc(max) | - | - | ±10 | µA |
| Output Leakage Current | | $I_{LO}$ | $V_{OUT}$=0 to Vcc(max) | - | - | ±10 | |
| Operating Current | Sequential Read | $I_{CC}1$ | tRC=50ns, $\overline{CE}$=$V_{IL}$<br>$I_{OUT}$=0mA | - | 10 | 20 | mA |
| | Program | $I_{CC}2$ | - | - | 10 | 20 | |
| | Erase | $I_{CC}3$ | - | - | 10 | 20 | |
| Input High Voltage | | $V_{IH}$ | - | 2.0 | - | $V_{CC}$+0.3 | V |
| Input Low Voltage, All inputs | | $V_{IL}$ | - | -0.3 | - | 0.8 | |
| Output High Voltage Level | | $V_{OH}$ | $I_{OH}$=-400µA | 2.4 | - | - | |
| Output Low Voltage Level | | $V_{OL}$ | $I_{OL}$=2.1mA | - | - | 0.4 | |
| Output Low Current(R/$\overline{B}$) | | $I_{OL}$(R/$\overline{B}$) | $V_{OL}$=0.4V | 8 | 10 | - | mA |
| Stand-by Current(TTL) | | $I_{SB}1$ | $\overline{CE}$=$V_{IH}$, $\overline{WP}$=0V/$V_{CC}$ | - | - | 1 | mA |
| Stand-by Current(CMOS) | | $I_{SB}2$ | $\overline{CE}$=$V_{CC}$-0.2, $\overline{WP}$=0V/$V_{CC}$ | - | 10 | 50 | µA |

## 64Mbit U*t*RAM DC AND OPERATING CHARACTERISTICS

| Item | Symbol | Test Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $V_{IN}$=Vss to Vcc | -1 | - | 1 | µA |
| Output leakage current | $I_{LO}$ | $\overline{CS}$=$V_{IH}$, $\overline{ZZ}$=$V_{IH}$, $\overline{OE}$=$V_{IH}$ or $\overline{WE}$=$V_{IL}$, $V_{IO}$=Vss to Vcc | -1 | - | 1 | µA |
| Average operating current | $I_{CC1}$ | Cycle time=1µs, 100% duty, $I_{IO}$=0mA, $\overline{CS}$≤0.2V, $\overline{ZZ}$≥Vcc-0.2V, $V_{IN}$≤0.2V or $V_{IN}$≥$V_{CC}$-0.2V | - | 3 | 7 | mA |
| | $I_{CC2}$ | Cycle time=Min, $I_{IO}$=0mA, 100% duty, $\overline{CS}$=$V_{IL}$, $\overline{ZZ}$=$V_{IH}$, $V_{IN}$=$V_{IL}$ or $V_{IH}$ | - | 35 | 40 | mA |
| Input high voltage | $V_{IH}$ | - | 2.2 | - | Vcc+0.3[2] | V |
| Input low voltage | $V_{IL}$ | - | -0.3[3] | - | 0.6 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$=-1.0mA | 2.4 | - | - | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$=2.1mA | - | - | 0.4 | V |
| Standby Current(CMOS) | $I_{SB1}$ | $\overline{CS}$≥Vcc-0.2V, $\overline{ZZ}$≥Vcc-0.2V, Other inputs=Vss to Vcc | - | 80 | 100 | µA |
| Deep Power Down | $I_{SBD}$ | $\overline{ZZ}$≤0.2V, Other inputs=Vss to Vcc | - | - | 20 | µA |

1. Typical values are tested at $V_{CC}$=2.9V, $T_A$=25°C and not guaranteed.
2. In case that the device maintains standby state without any read or write activity after power up, the standby current will be increased and so the device may not meet the specification presented above.[See page 33 "TIMING WAVEFORM OF POWER UP"]
3. Overshoot: Vcc+1.0V in case of pulse width ≤20ns.
4. Undershoot: -1.0V in case of pulse width ≤20ns.
5. Overshoot and undershoot are sampled, not 100% tested.

## 32Mbit U*t*RAM DC AND OPERATING CHARACTERISTICS

| Item | Symbol | Test Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $V_{IN}$=Vss to Vcc | -1 | - | 1 | µA |
| Output leakage current | $I_{LO}$ | $\overline{CS}$=$V_{IH}$, $\overline{ZZ}$=$V_{IH}$, $\overline{OE}$=$V_{IH}$ or $\overline{WE}$=$V_{IL}$, $V_{IO}$=Vss to Vcc | -1 | - | 1 | µA |
| Average operating current | $I_{CC1}$ | Cycle time=1µs, 100% duty, $I_{IO}$=0mA, $\overline{CS}$≤0.2V, $\overline{ZZ}$≥Vcc-0.2V, $V_{IN}$≤0.2V or $V_{IN}$≥$V_{CC}$-0.2V | - | 4 | 7 | mA |
| | $I_{CC2}$ | Cycle time=Min, $I_{IO}$=0mA, 100% duty, $\overline{CS}$=$V_{IL}$, $\overline{ZZ}$=$V_{IH}$, $V_{IN}$=$V_{IL}$ or $V_{IH}$ | - | 30 | 35 | mA |
| Input high voltage | $V_{IH}$ | - | 2.2 | - | Vcc+0.3[3] | V |
| Input low voltage | $V_{IL}$ | - | -0.3[4] | - | 0.6 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$=-1.0mA | 2.4 | - | - | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$=2.1mA | - | - | 0.4 | V |
| Standby Current(CMOS) | $I_{SB1}$[2] | $\overline{CS}$≥Vcc-0.2V, $\overline{ZZ}$≥Vcc-0.2V, Other inputs=Vss to Vcc | - | 80 | 100 | µA |
| Deep Power Down | $I_{SBD}$ | $\overline{ZZ}$≤0.2V, Other inputs=Vss to Vcc | - | 5 | 10 | µA |

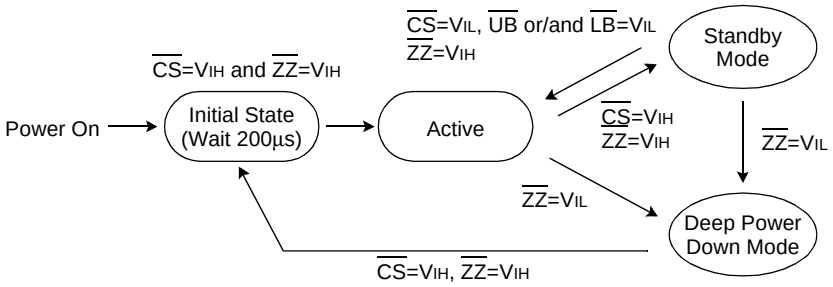
1. Typical values are tested at $V_{CC}$=2.9V, $T_A$=25°C and not guaranteed.
2. In case that the device maintains standby state without any read or write activity after power up, the standby current will be increased and so the device may not meet the specification presented above.[See page 33 "TIMING WAVEFORM OF POWER UP"]
3. Overshoot: Vcc+1.0V in case of pulse width ≤20ns.
4. Undershoot: -1.0V in case of pulse width ≤20ns.
5. Overshoot and undershoot are sampled, not 100% tested.

## SRAM DC AND OPERATING CHARACTERISTICS($V_{CC}$=2.7~3.1V, $T_A$=-25 to 85°C)

| Item | Symbol | Test Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $V_{IN}$=Vss to $V_{CC}$ | -1 | - | 1 | µA |
| Output leakage current | $I_{LO}$ | $\overline{CS_1}$=$V_{IH}$ or $CS_2$=$V_{IL}$ or $\overline{OE}$=$V_{IH}$ or $\overline{WE}$=$V_{IL}$ or $\overline{LB}$=$\overline{UB}$=$V_{IH}$, $V_{IO}$=Vss to $V_{CC}$ | -1 | - | 1 | µA |
| Average operating current | $I_{CC1}$ | Cycle time=1µs, 100%duty, $I_{IO}$=0mA, $\overline{CS_1}$≤0.2V, $\overline{LB}$≤0.2V or/and $\overline{UB}$≤0.2V, $CS_2$≥$V_{CC}$-0.2V, $V_{IN}$≤0.2V or $V_{IN}$≥$V_{CC}$-0.2V | - | - | 3 | mA |
| | $I_{CC2}$ | Cycle time=Min, $I_{IO}$=0mA, 100% duty, $\overline{CS_1}$≤0.2V, $\overline{LB}$≤0.2V or/and $\overline{UB}$≤0.2V, $CS_2$≥$V_{CC}$-0.2V, $V_{IN}$≤0.2V or $V_{IN}$≥$V_{CC}$-0.2V | - | 30 | 35 | mA |
| Input high voltage | $V_{IH}$ | - | 2.2 | - | $V_{CC}$+0.3[2] | V |
| Input low voltage | $V_{IL}$ | - | -0.3[3] | - | 0.6 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = -1.0mA | 2.4 | - | - | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 2.1mA | - | - | 0.4 | V |
| Standby Current(CMOS) | $I_{SB1}$ | Other input =0~Vcc<br>1) $CS_1$≥$V_{CC}$-0.2V, $CS_2$≥$V_{CC}$-0.2V($\overline{CS_1}$ controlled) or<br>2) 0V≤$CS_2$≤0.2V($CS_2$ controlled) | - | 0.5 | 15 | µA |

1. Typical values are measured at $V_{CC}$=2.9V, $T_A$=25°C and not 100% tested.
2. Overshoot: $V_{CC}$+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and Undershoot are sampled, not 100% tested.

## STANDBY MODE STATE MACHINES(U*t*RAM)




## STANDBY MODE CHARACTERISTIC(64Mbit U*t*RAM)

| Power Mode | Memory Cell Data | Standby Current(μA) | Wait Time(μs) |
|---|---|---|---|
| Standby | Valid | 100 | 0 |
| Deep Power Down | Invaild | 20 | 200 |

## STANDBY MODE CHARACTERISTIC(32Mbit U*t*RAM)

| Power Mode | Memory Cell Data | Standby Current(μA) | Wait Time(μs) |
|---|---|---|---|
| Standby | Valid | 100 | 0 |
| Deep Power Down | Invaild | 10 | 200 |

## CAPACITANCE ($T_A$ = 25 °C, f = 1.0MHz)

| Item | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input/Output Capacitance | $C_{DQ}$ | $V_{IL}$=0V | - | 40 | pF |
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 40 | pF |

**NOTE:** Capacitance is periodically sampled and not 100% tested.

## VALID BLOCK(Flash)

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Valid Block Number | $N_{VB}$ | 1004 | - | 1024 | Blocks |

**NOTE:**
1. The Flash memory may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not try to access these invalid blocks for program and erase. Refer to the attached technical notes for a appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

## Flash AC TEST CONDITION

| Parameter | Value |
|---|---|
| Input Pulse Levels | 0.4V to 2.4V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | 1.5V |
| Output Load | 1 TTL GATE and CL=50pF |

## Flash Program/Erase Characteristics

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Program Time | | $t_{PROG}$ | - | 200 | 500 | µs |
| Number of Partial Program Cycles in the Same Page | Main Array | Nop | - | - | 2 | cycles |
| | Spare Array | | - | - | 3 | cycles |
| Block Erase Time | | $t_{BERS}$ | - | 2 | 3 | ms |

## Flash AC Timing Characteristics for Command / Address / Data Input

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| CLE Set-up Time | $t_{CLS}$ | 0 | - | ns |
| CLE Hold Time | $t_{CLH}$ | 10 | - | ns |
| $\overline{CE}$ Setup Time | $t_{CS}$ | 0 | - | ns |
| $\overline{CE}$ Hold Time | $t_{CH}$ | 10 | - | ns |
| $\overline{WE}$ Pulse Width | $t_{WP}$(1) | 25 | - | ns |
| ALE Setup Time | $t_{ALS}$ | 0 | - | ns |
| ALE Hold Time | $t_{ALH}$ | 10 | - | ns |
| Data Setup Time | $t_{DS}$ | 20 | - | ns |
| Data Hold Time | $t_{DH}$ | 10 | - | ns |
| Write Cycle Time | $t_{WC}$ | 45 | - | ns |
| $\overline{WE}$ High Hold Time | $t_{WH}$ | 15 | - | ns |

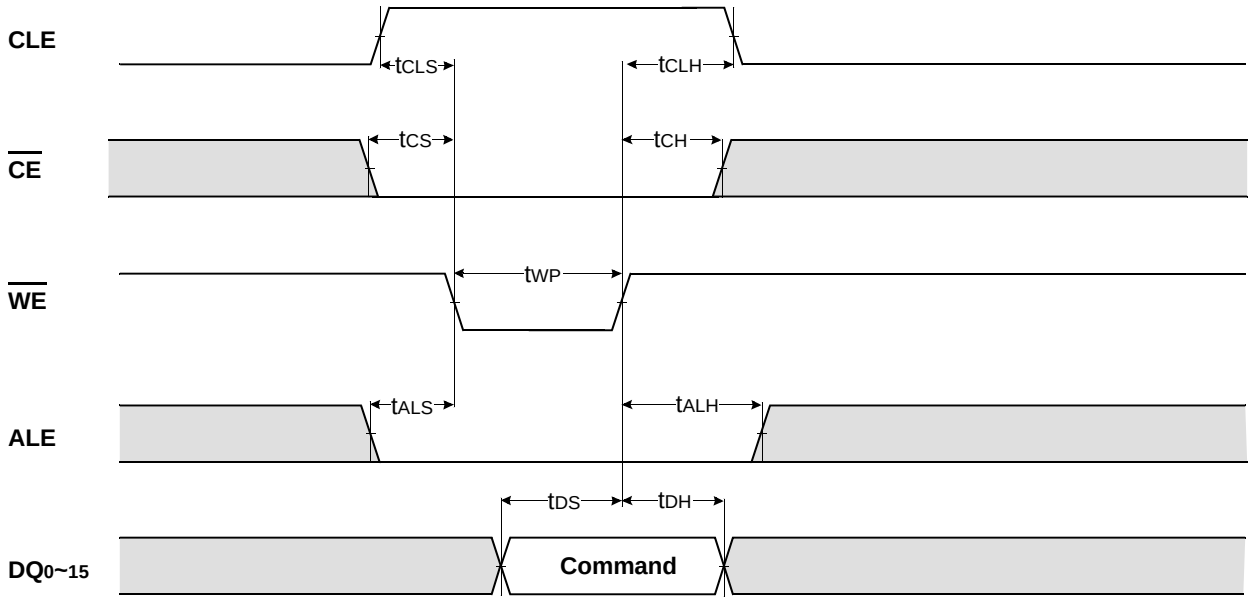
**NOTE:** 1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

## Flash AC Characteristics for Operation

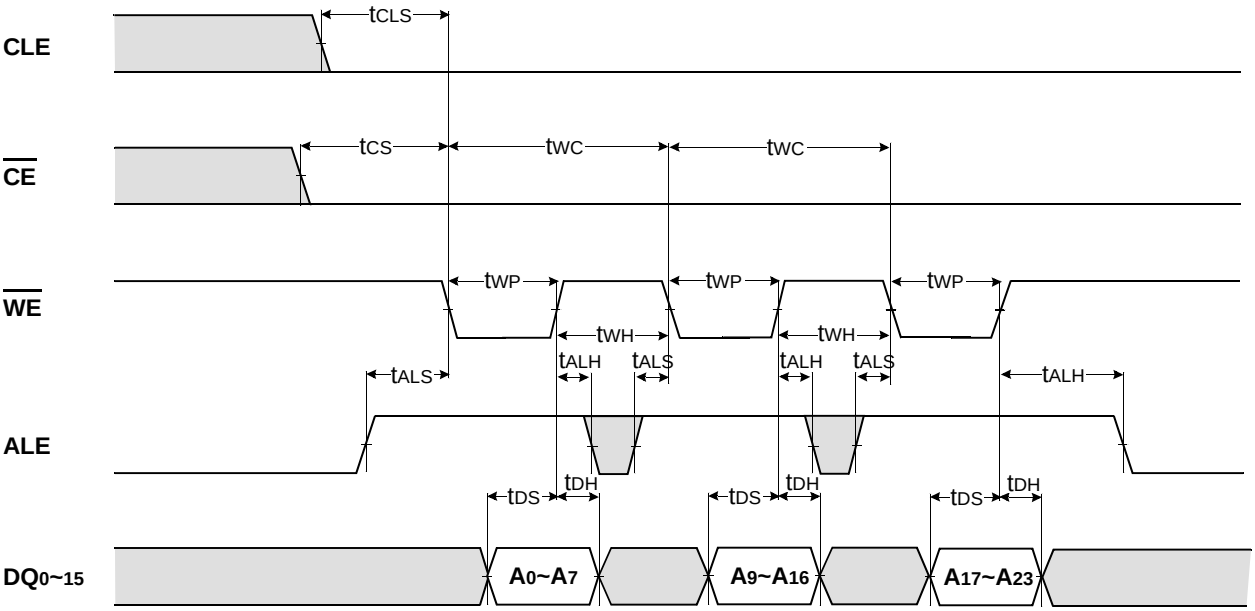
| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Data Transfer from Cell to Register | $t_R$ | - | 10 | µs |
| ALE to $\overline{RE}$ Delay | $t_{AR}$ | 10 | - | ns |
| CLE to $\overline{RE}$ Delay | $t_{CLR}$ | 10 | - | ns |
| Ready to $\overline{RE}$ Low | $t_{RR}$ | 20 | - | ns |
| $\overline{RE}$ Pulse Width | $t_{RP}$ | 25 | - | ns |
| $\overline{WE}$ High to Busy | $t_{WB}$ | - | 100 | ns |
| Read Cycle Time | $t_{RC}$ | 50 | - | ns |
| $\overline{CE}$ Access Time | $t_{CEA}$ | - | 45 | ns |
| $\overline{RE}$ Access Time | $t_{REA}$ | - | 30 | ns |
| $\overline{RE}$ High to Output Hi-Z | $t_{RHZ}$ | - | 30 | ns |
| $\overline{CE}$ High to Output Hi-Z | $t_{CHZ}$ | - | 20 | ns |
| $\overline{RE}$ or $\overline{CE}$ High to Output hold | $t_{OH}$ | 15 | - | ns |
| $\overline{RE}$ High Hold Time | $t_{REH}$ | 15 | - | ns |
| Output Hi-Z to $\overline{RE}$ Low | $t_{IR}$ | 0 | - | ns |
| $\overline{WE}$ High to $\overline{RE}$ Low | $t_{WHR}$ | 60 | - | ns |
| Device Resetting Time(Read/Program/Erase) | $t_{RST}$ | - | 5/10/500(1) | µs |

**NOTE:**
1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.

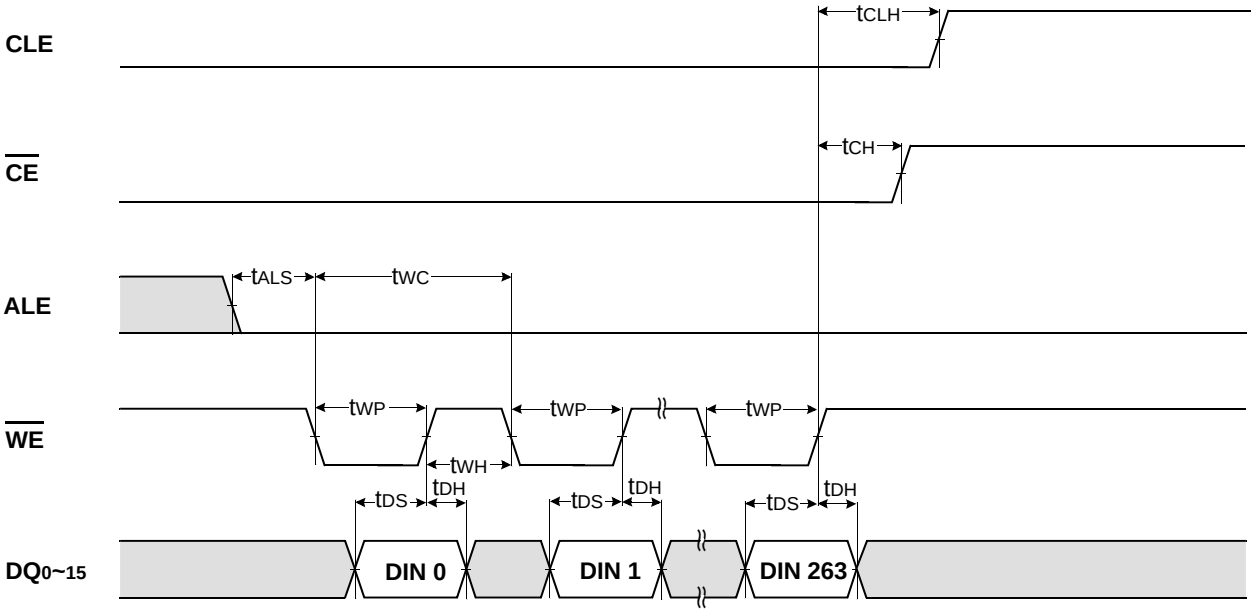
## Flash Command Latch Cycle



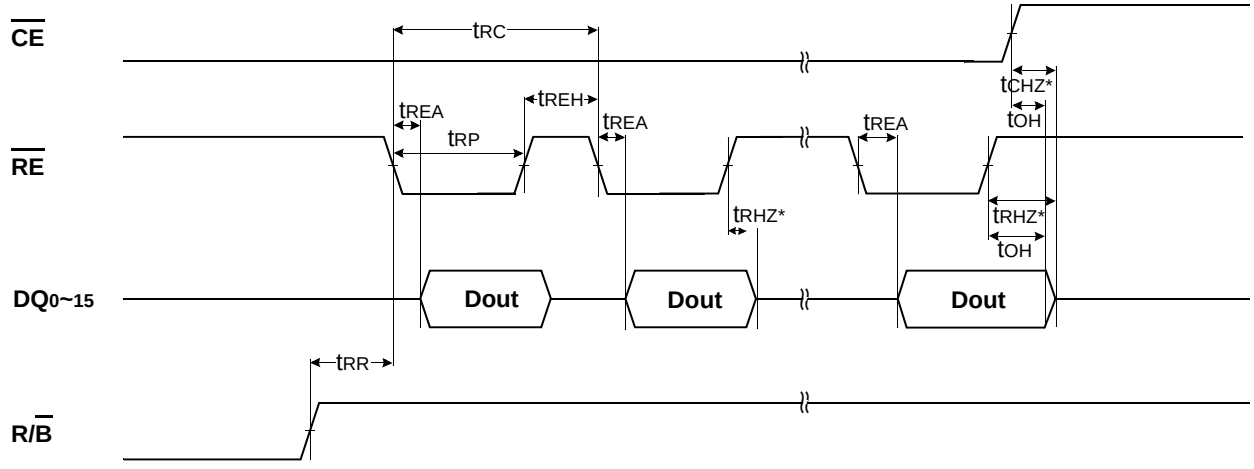

## Flash Address Latch Cycle



## Flash Input Data Latch Cycle

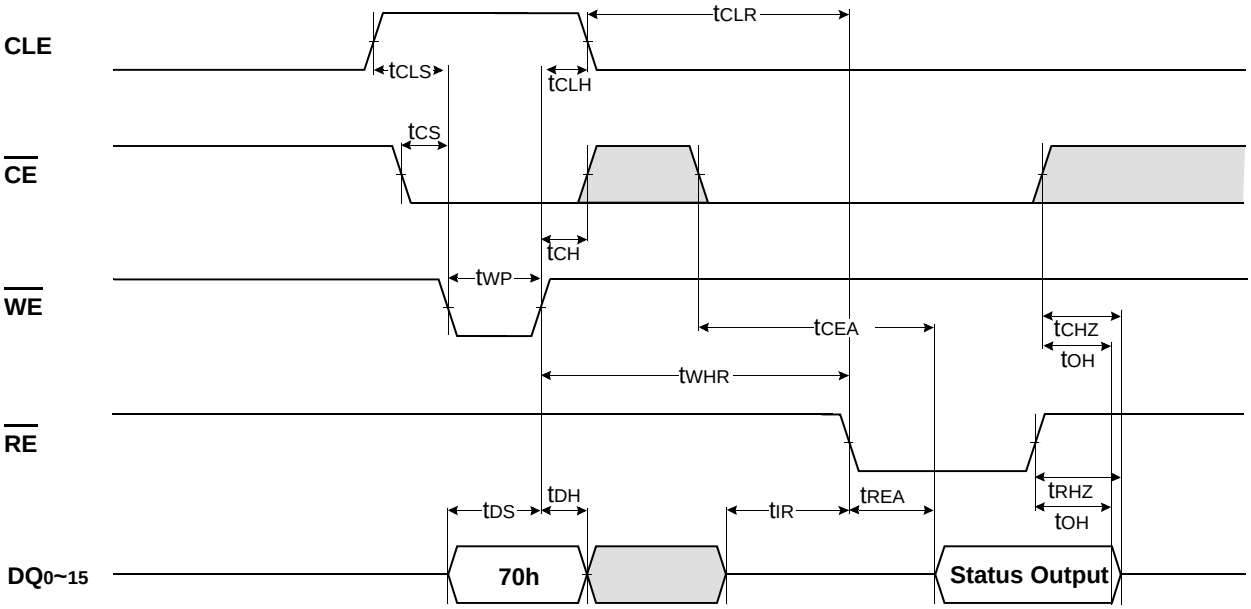



## Flash Serial access Cycle after Read(CLE=L, $\overline{WE}$=H, ALE=L)

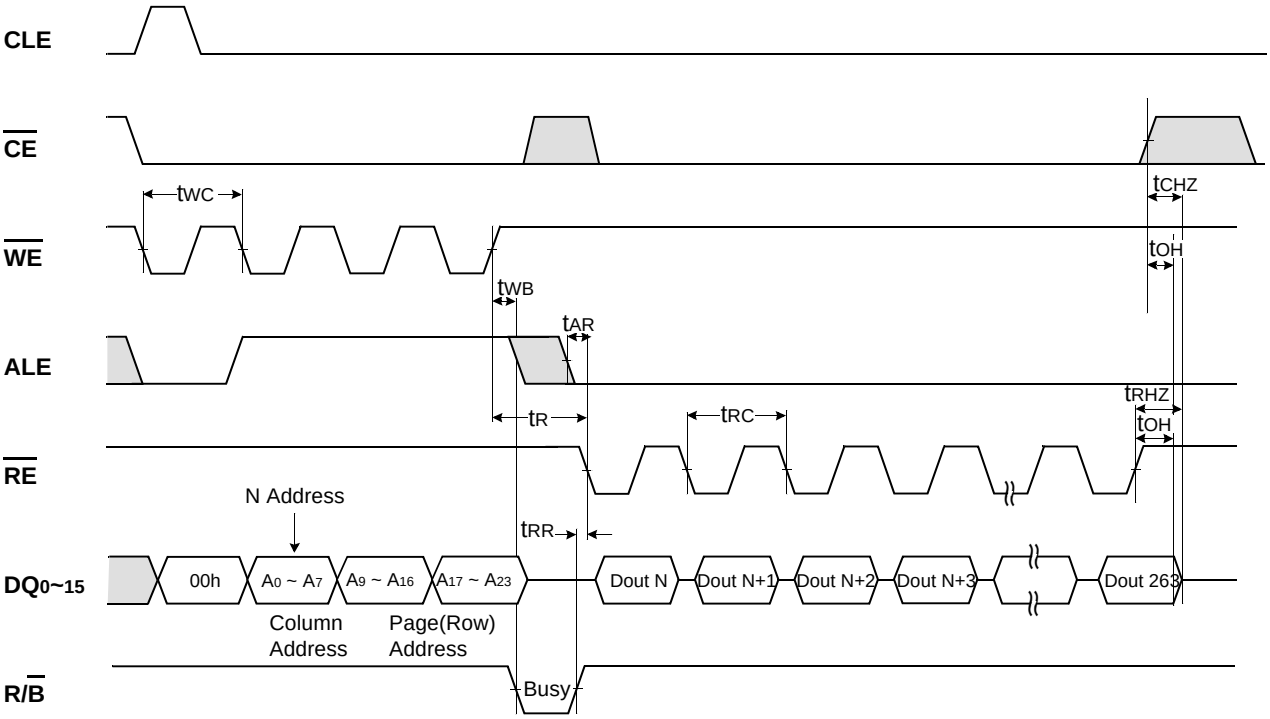



**NOTES :** Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

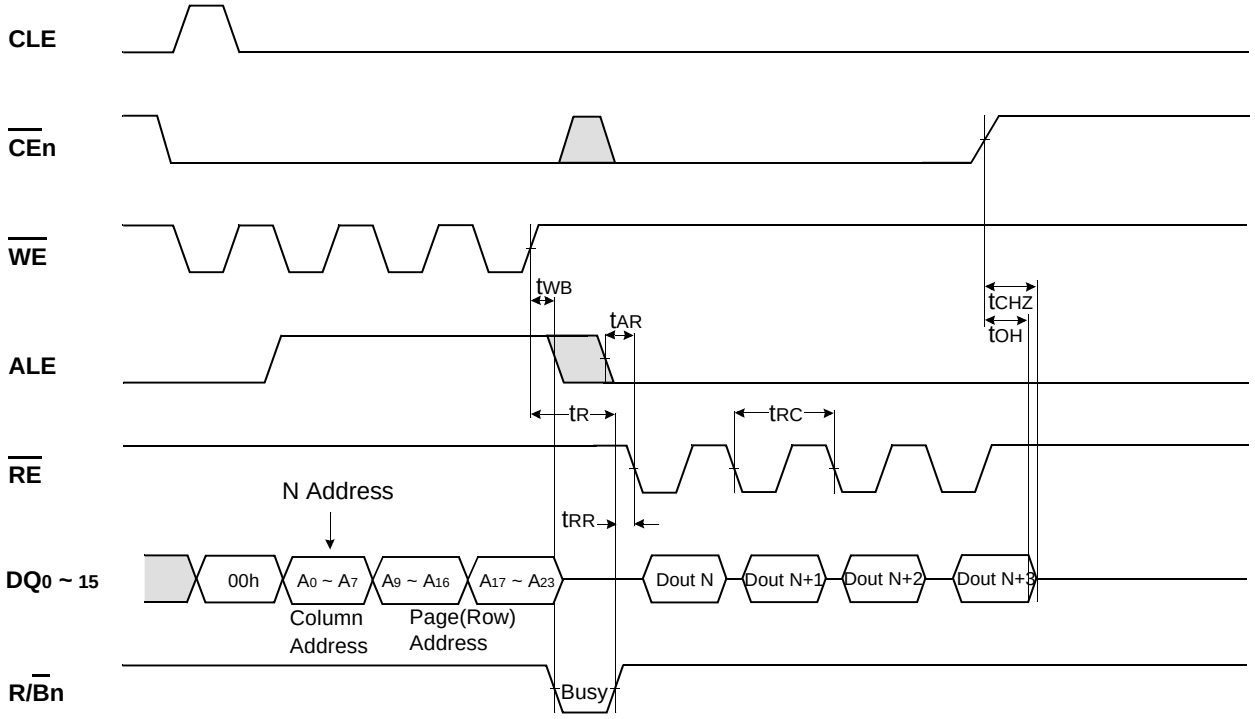
### Flash Status Read Cycle



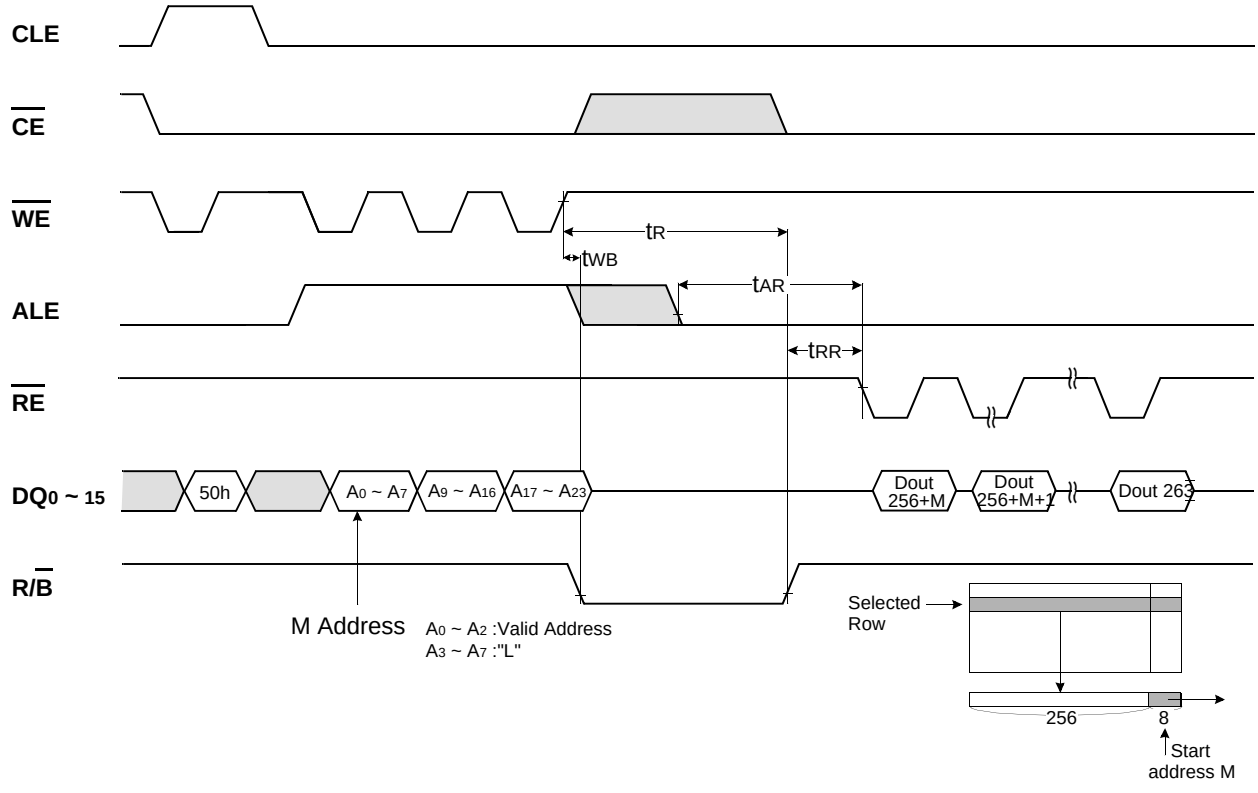

### FLASH READ1 OPERATION(READ ONE PAGE)



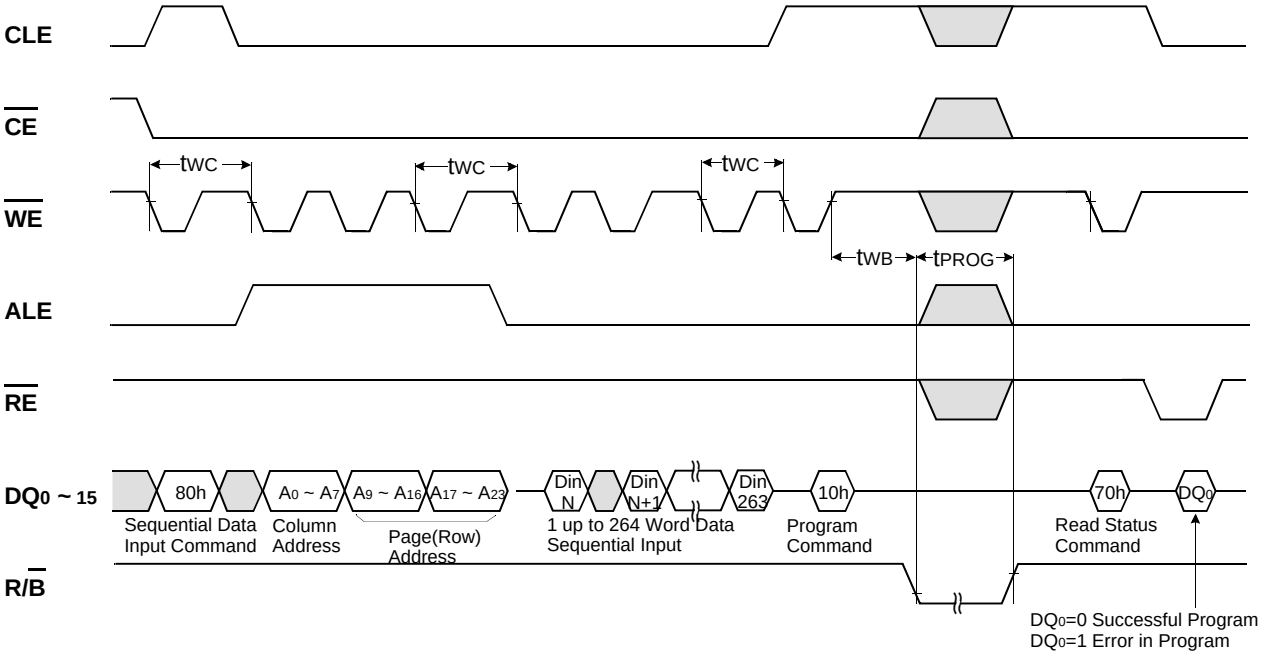
## Flash READ1 OPERATION (INTERCEPTED BY $\overline{CE}$)



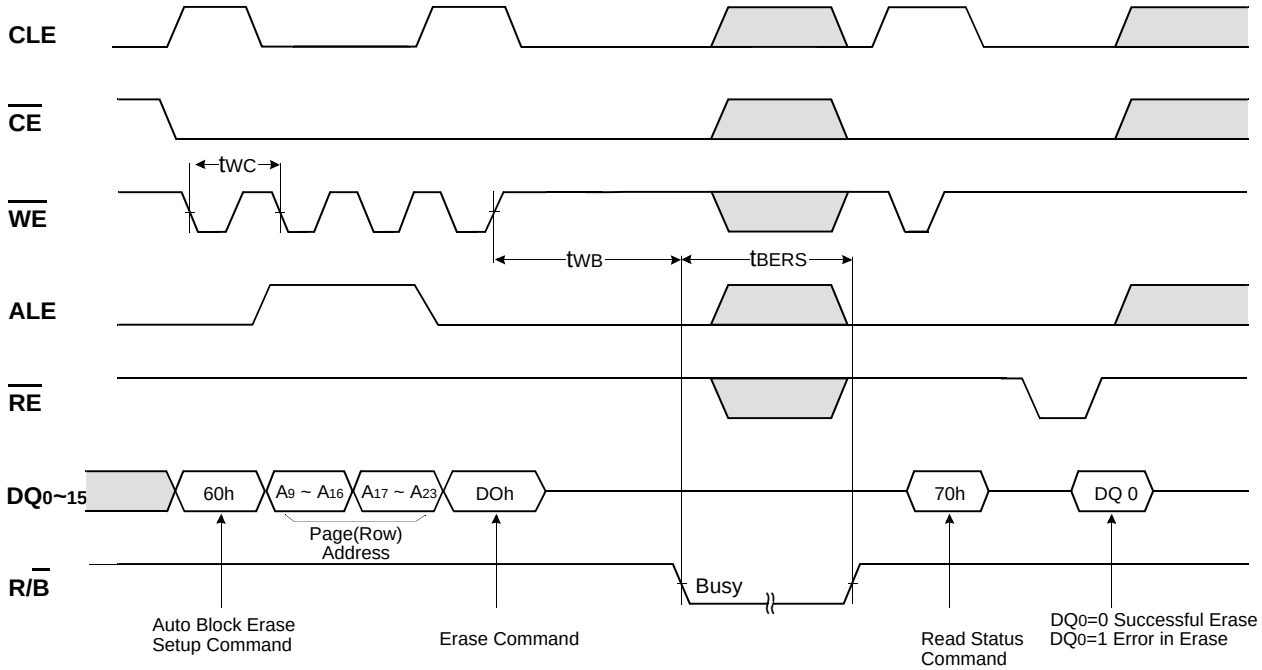

## FLASH READ2 OPERATION(READ ONE PAGE)



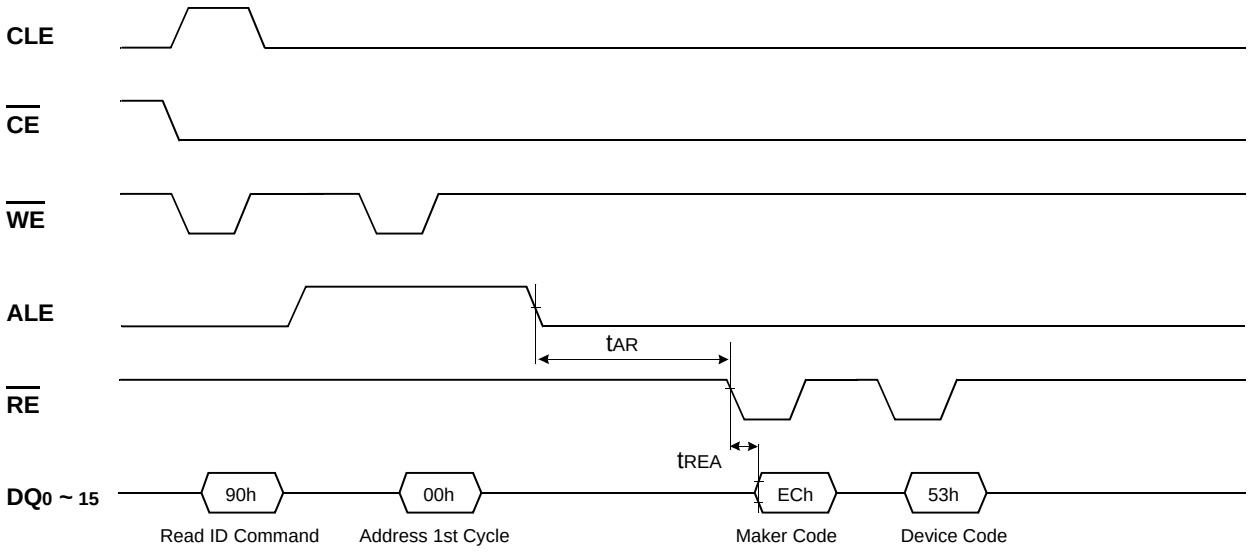
## FLASH PAGE PROGRAM OPERATION




## FLASH BLOCK ERASE OPERATION(ERASE ONE BLOCK)



## FLASH MANUFACTURE & DEVICE ID READ OPERATION



## 64Mbit U*t*RAM AC OPERATING CONDITIONS

**TEST CONDITIONS**(Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load: $C_L$=50pF

## 64Mbit U*t*RAM AC CHARACTERISTICS($V_{CC}$=2.7~3.1V, $T_A$=-25 to 85°C)

| Parameter List | | Symbol | Speed | | Units |
|---|---|---|---|---|---|
| | | | 70ns | | |
| | | | Min | Max | |
| Read | Read Cycle Time | $t_{RC}$ | 70 | - | ns |
| | Address Access Time | $t_{AA}$ | - | 70 | ns |
| | Chip Select to Output | $t_{CO}$ | - | 70 | ns |
| | Output Enable to Valid Output | $t_{OE}$ | - | 35 | ns |
| | $\overline{UB}$, $\overline{LB}$ Access Time | $t_{BA}$ | - | 70 | ns |
| | Chip Select to Low-Z Output | $t_{LZ}$ | 10 | - | ns |
| | $\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output | $t_{BLZ}$ | 10 | - | ns |
| | Output Enable to Low-Z Output | $t_{OLZ}$ | 5 | - | ns |
| | Chip Disable to High-Z Output | $t_{HZ}$ | 0 | 25 | ns |
| | $\overline{UB}$, $\overline{LB}$ Disable to High-Z Output | $t_{BHZ}$ | 0 | 25 | ns |
| | Output Disable to High-Z Output | $t_{OHZ}$ | 0 | 25 | ns |
| | Output Hold from Address Change | $t_{OH}$ | 5 | - | ns |
| Write | Write Cycle Time | $t_{WC}$ | 70 | - | ns |
| | Chip Select to End of Write | $t_{CW}$ | 60 | - | ns |
| | Address Set-up Time | $t_{AS}$ | 0 | - | ns |
| | Address Valid to End of Write | $t_{AW}$ | 60 | - | ns |
| | $\overline{UB}$, $\overline{LB}$ Valid to End of Write | $t_{BW}$ | 60 | - | ns |
| | Write Pulse Width | $t_{WP}$ | 55[1)] | - | ns |
| | Write Recovery Time | $t_{WR}$ | 0 | - | ns |
| | Write to Output High-Z | $t_{WHZ}$ | 0 | 25 | ns |
| | Data to Write Time Overlap | $t_{DW}$ | 30 | - | ns |
| | Data Hold from Write Time | $t_{DH}$ | 0 | - | ns |
| | End Write to Output Low-Z | $t_{OW}$ | 5 | - | ns |

1. $t_{WP}$(min)=70ns for continuous write operation over 50 times.

## 32Mbit U*t*RAM AC OPERATING CONDITIONS

**TEST CONDITIONS**(Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load: $C_L$=50pF

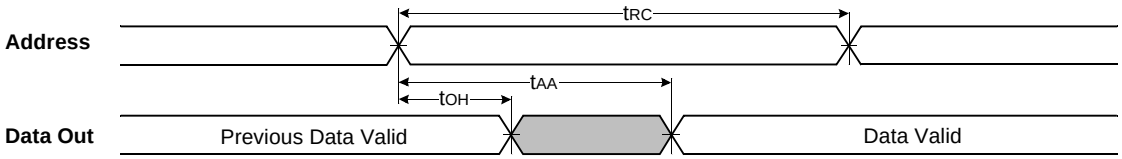
## 32Mbit U*t*RAM AC CHARACTERISTICS($V_{CC}$=2.7~3.1V, $T_A$=-25 to 85°C)

| Parameter List | | Symbol | Speed Bins | | Units |
|---|---|---|---|---|---|
| | | | 85ns[1] | | |
| | | | Min | Max | |
| Read | Read Cycle Time | $t_{RC}$ | 85 | - | ns |
| | Address Access Time | $t_{AA}$ | - | 85 | ns |
| | Chip Select to Output | $t_{CO}$ | - | 85 | ns |
| | Output Enable to Valid Output | $t_{OE}$ | - | 40 | ns |
| | $\overline{UB}$, $\overline{LB}$ Access Time | $t_{BA}$ | - | 85 | ns |
| | Chip Select to Low-Z Output | $t_{LZ}$ | 10 | - | ns |
| | $\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output | $t_{BLZ}$ | 10 | - | ns |
| | Output Enable to Low-Z Output | $t_{OLZ}$ | 5 | - | ns |
| | Chip Disable to High-Z Output | $t_{HZ}$ | 0 | 25 | ns |
| | $\overline{UB}$, $\overline{LB}$ Disable to High-Z Output | $t_{BHZ}$ | 0 | 25 | ns |
| | Output Disable to High-Z Output | $t_{OHZ}$ | 0 | 25 | ns |
| | Output Hold from Address Change | $t_{OH}$ | 5 | - | ns |
| Write | Write Cycle Time | $t_{WC}$ | 85 | - | ns |
| | Chip Select to End of Write | $t_{CW}$ | 70 | - | ns |
| | Address Set-up Time | $t_{AS}$ | 0 | - | ns |
| | Address Valid to End of Write | $t_{AW}$ | 70 | - | ns |
| | $\overline{UB}$, $\overline{LB}$ Valid to End of Write | $t_{BW}$ | 70 | - | ns |
| | Write Pulse Width | $t_{WP}$ | 60[1] | - | ns |
| | Write Recovery Time | $t_{WR}$ | 0 | - | ns |
| | Write to Output High-Z | $t_{WHZ}$ | 0 | 25 | ns |
| | Data to Write Time Overlap | $t_{DW}$ | 35 | - | ns |
| | Data Hold from Write Time | $t_{DH}$ | 0 | - | ns |
| | End Write to Output Low-Z | $t_{OW}$ | 5 | - | ns |

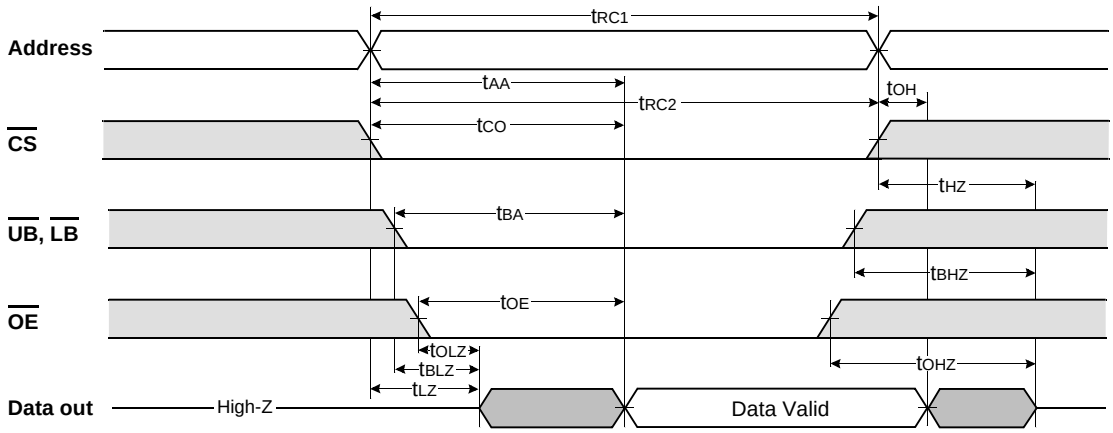
1. $t_{WP}$(min)=85ns for continuous write operation over 50 times.

## U*t*RAM TIMING DIAGRAMS

### TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CS}$=$\overline{OE}$=$V_{IL}$, $\overline{ZZ}$=$\overline{WE}$=$V_{IH}$, $\overline{UB}$ or/and $\overline{LB}$=$V_{IL}$)



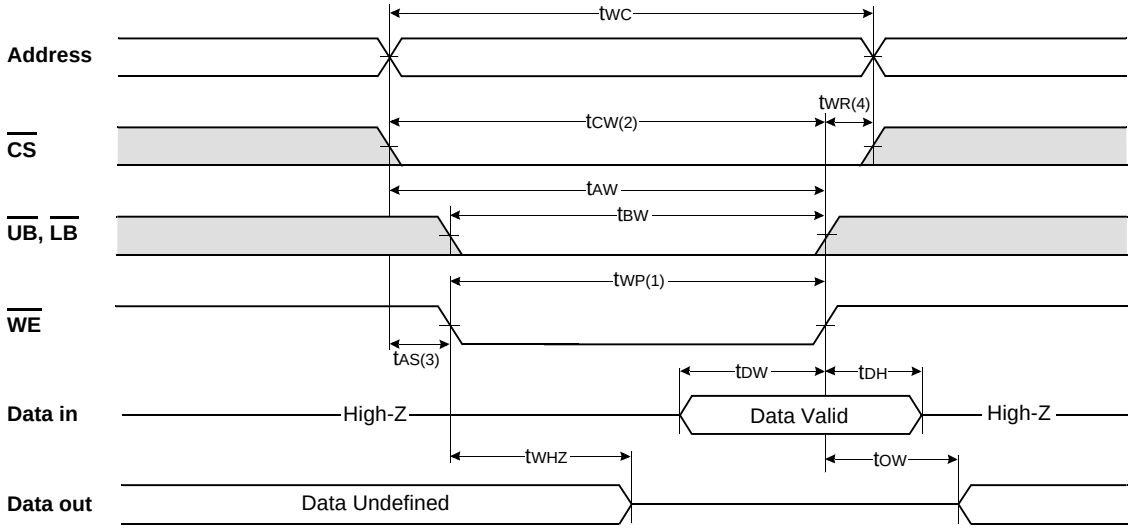

### TIMING WAVEFORM OF READ CYCLE(2)($\overline{ZZ}$=$\overline{WE}$=$V_{IH}$)



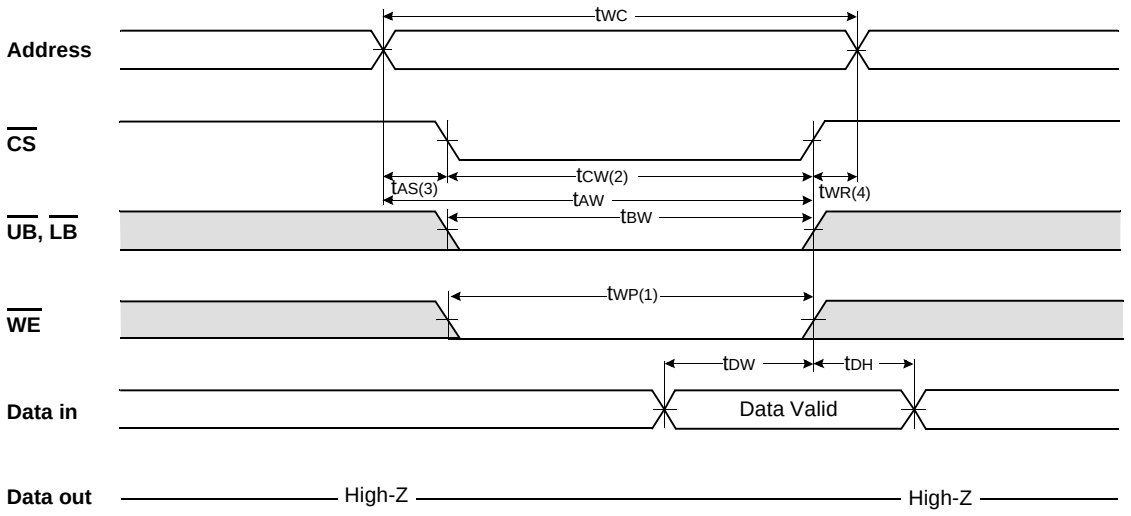

(READ CYCLE)

1. $t_{HZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}$(Max.) is less than $t_{LZ}$(Min.) both for a given device and from device to device interconnection.
3. $t_{OE}$(max) is met only when $\overline{OE}$ becomes enabled after $t_{AA}$(max).
4. If invalid address signals shorter than min. $t_{RC}$ are continuously repeated for over 4us, the device needs a normal read timing($t_{RC}$) or needs to sustain standby state for min. $t_{RC}$ at least once in every 4us.

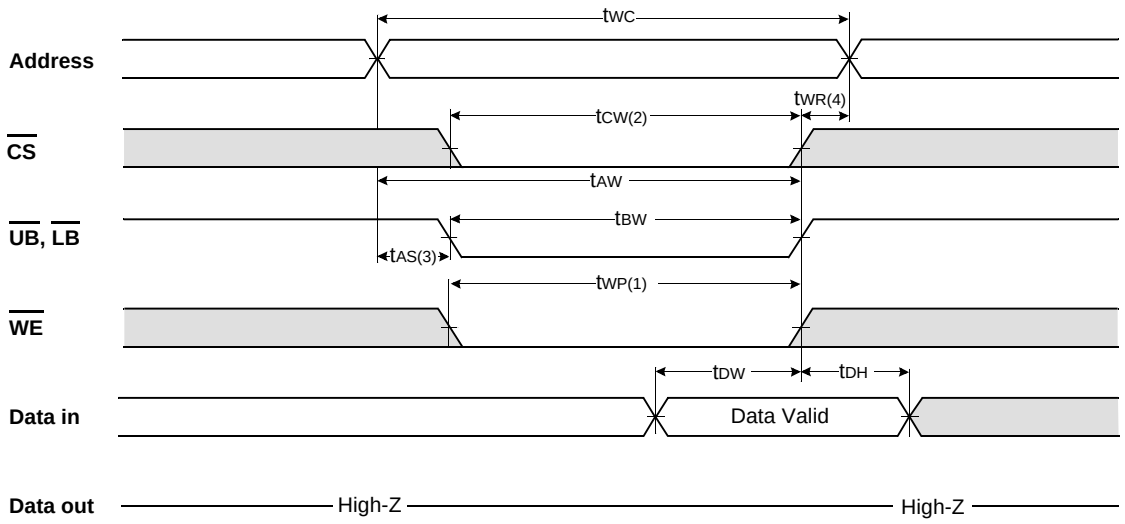
**TIMING WAVEFORM OF WRITE CYCLE(1)**($\overline{WE}$ Controlled, $\overline{ZZ}$=$V_{IH}$)




**TIMING WAVEFORM OF WRITE CYCLE(2)**($\overline{CS}$ Controlled, $\overline{ZZ}$=$V_{IH}$)



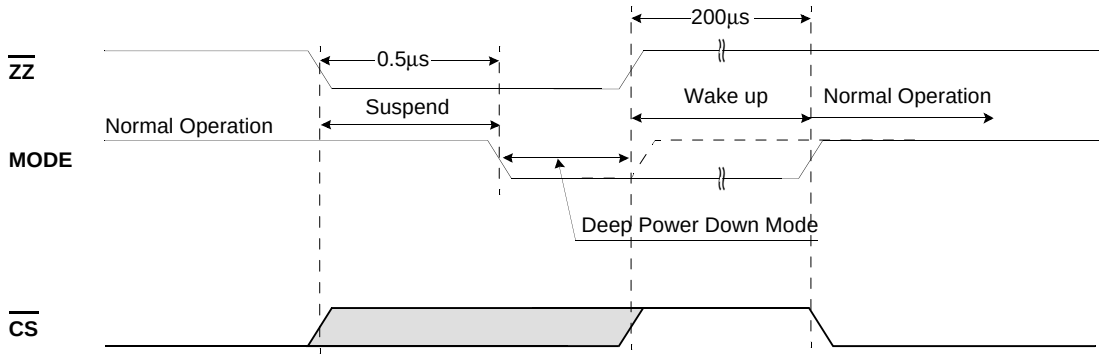
**TIMING WAVEFORM OF WRITE CYCLE(3)**($\overline{UB}$, $\overline{LB}$ Controlled, $\overline{ZZ}$=$V_{IH}$)




(WRITE CYCLE)

1. A write occurs during the overlap($t_{WP}$) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The $t_{WP}$ is measured from the beginning of write to the end of write.
2. $t_{CW}$ is measured from the $\overline{CS}$ going low to the end of write.
3. $t_{AS}$ is measured from the address valid to the beginning of write.
4. $t_{WR}$ is measured from the end of write to the address change. $t_{WR}$ is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.

**TIMING WAVEFORM OF DEEP POWER DOWN MODE**



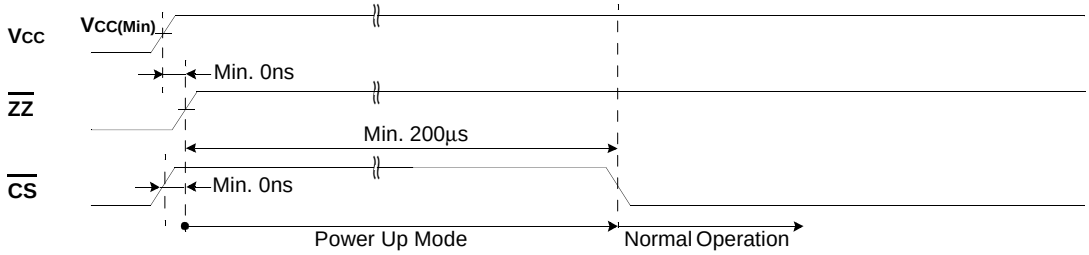

(DEEP POWER DOWN MODE)

1. When you toggle $\overline{ZZ}$ pin low, the device gets into the Deep Power Down mode after 0.5µs suspend period.
2. To return to normal operation, the device needs Wake Up period.
3. Wake Up sequence is just the same as Power Up sequence.

## POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power(Vcc min.=2.7V) for a minimum 200µs with $\overline{CS}$ and $\overline{ZZ}$ high.

## TIMING WAVEFORM OF POWER UP



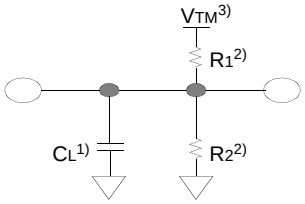

(POWER UP)

1. After $V_{CC}$ reaches $V_{CC}$(Min.), wait 200µs with $\overline{CS}$ and $\overline{ZZ}$ high. Then you get into the normal operation.

## SRAM AC OPERATING CONDITIONS

**TEST CONDITIONS**(Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load(see right): $C_L$=30pF+1TTL




1. Including scope and jig capacitance
2. $R_1$=3070Ω, $R_2$=3150Ω
3. $V_{TM}$ =2.8V

## SRAM AC CHARACTERISTICS ($V_{CC}$=2.7~3.1V, $T_A$=-25 to 85°C)

| Parameter List | | Symbol | Speed Bins | | Units |
|---|---|---|---|---|---|
| | | | 55ns | | |
| | | | Min | Max | |
| Read | Read Cycle Time | $t_{RC}$ | 55 | - | ns |
| | Address Access Time | $t_{AA}$ | - | 55 | ns |
| | Chip Select to Output | $t_{CO}$ | - | 55 | ns |
| | Output Enable to Valid Output | $t_{OE}$ | - | 25 | ns |
| | $\overline{UB}$, $\overline{LB}$ Access Time | $t_{BA}$ | - | 55 | ns |
| | Chip Select to Low-Z Output | $t_{LZ}$ | 10 | - | ns |
| | $\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output | $t_{BLZ}$ | 10 | - | ns |
| | Output Enable to Low-Z Output | $t_{OLZ}$ | 5 | - | ns |
| | Chip Disable to High-Z Output | $t_{HZ}$ | 0 | 20 | ns |
| | $\overline{UB}$, $\overline{LB}$ Disable to High-Z Output | $t_{BHZ}$ | 0 | 20 | ns |
| | Output Disable to High-Z Output | $t_{OHZ}$ | 0 | 20 | ns |
| | Output Hold from Address Change | $t_{OH}$ | 10 | - | ns |
| Write | Write Cycle Time | $t_{WC}$ | 55 | - | ns |
| | Chip Select to End of Write | $t_{CW}$ | 45 | - | ns |
| | Address Set-up Time | $t_{AS}$ | 0 | - | ns |
| | Address Valid to End of Write | $t_{AW}$ | 45 | - | ns |
| | $\overline{UB}$, $\overline{LB}$ Valid to End of Write | $t_{BW}$ | 45 | - | ns |
| | Write Pulse Width | $t_{WP}$ | 40 | - | ns |
| | Write Recovery Time | $t_{WR}$ | 0 | - | ns |
| | Write to Output High-Z | $t_{WHZ}$ | 0 | 20 | ns |
| | Data to Write Time Overlap | $t_{DW}$ | 25 | - | ns |
| | Data Hold from Write Time | $t_{DH}$ | 0 | - | ns |
| | End Write to Output Low-Z | $t_{OW}$ | 5 | - | ns |

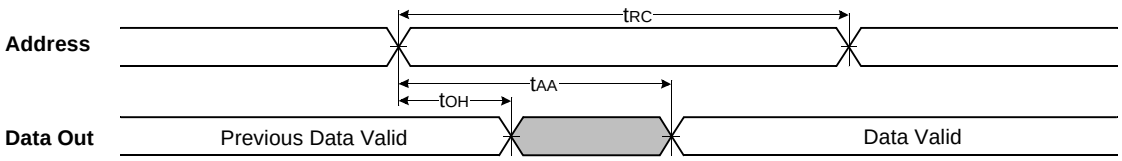
## DATA RETENTION CHARACTERISTICS

| Item | Symbol | Test Condition | Min | Typ2) | Max | Unit |
|---|---|---|---|---|---|---|
| Vcc for data retention | $V_{DR}$ | $\overline{CS_1}$≥Vcc-0.2V1) | 1.5 | - | 3.1 | V |
| Data retention current | $I_{DR}$ | Vcc=1.5V, $\overline{CS_1}$≥Vcc-0.2V1) | - | 0.5 | 6 | µA |
| Data retention set-up time | $t_{SDR}$ | See data retention waveform | 0 | - | - | ns |
| Recovery time | $t_{RDR}$ | | tRC | - | - | |

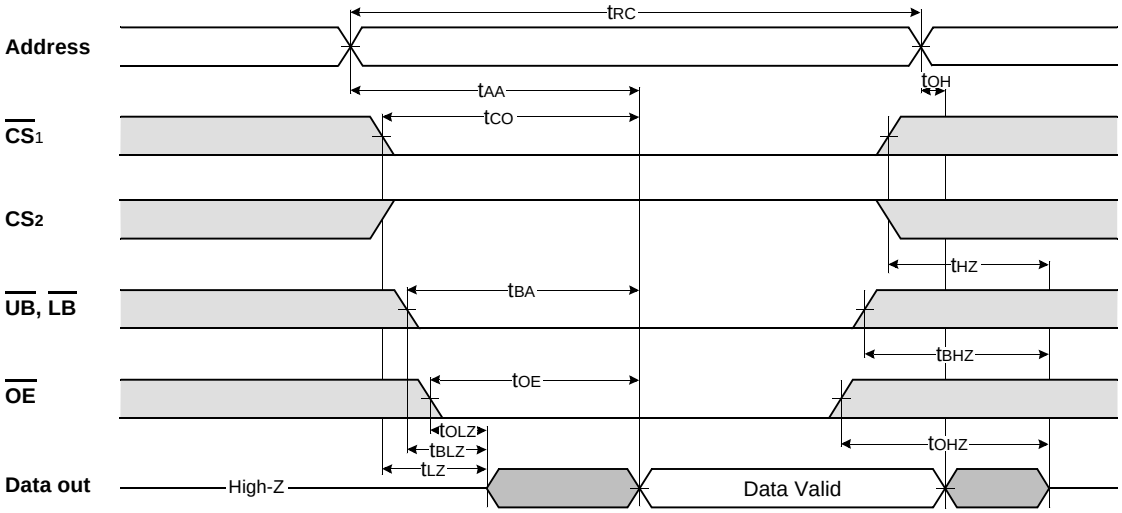
1. 1) $\overline{CS_1}$≥Vcc-0.2V, $CS_2$≥Vcc-0.2V($\overline{CS_1}$ controlled) or
   2) 0≤$CS_2$≤0.2V($CS_2$ controlled)
2. Typical value is measured at $T_A$=25°C and not 100% tested.

## SRAM TIMING DIAGRAMS

### TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS_1}$=$\overline{OE}$=$V_{IL}$, $CS_2$=$\overline{WE}$=$V_{IH}$, $\overline{UB}$ or/and $\overline{LB}$=$V_{IL}$)



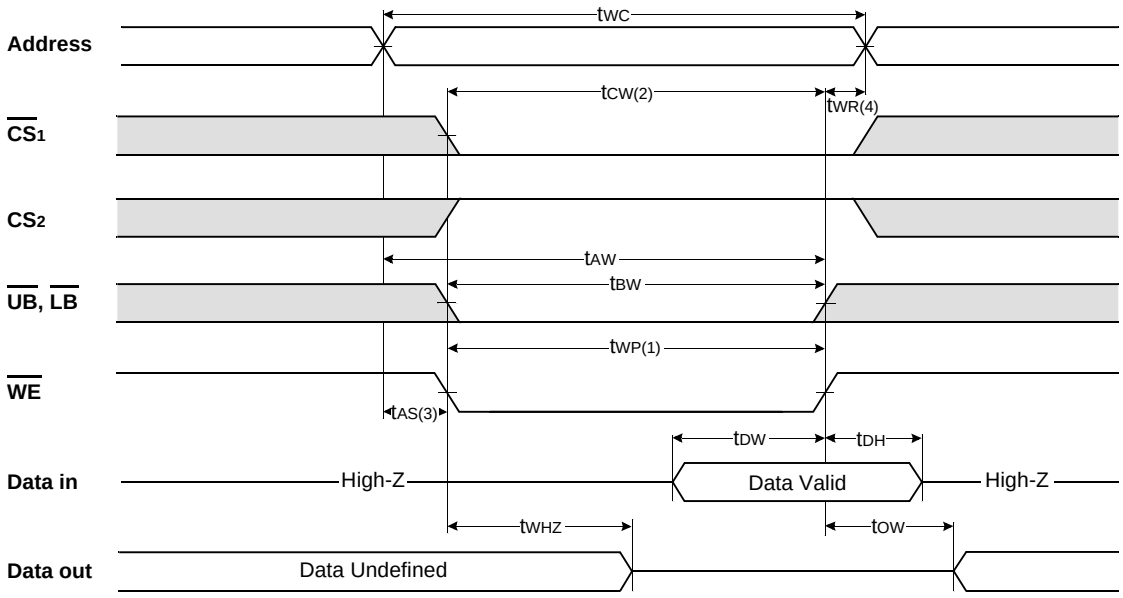

### TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=$V_{IH}$)



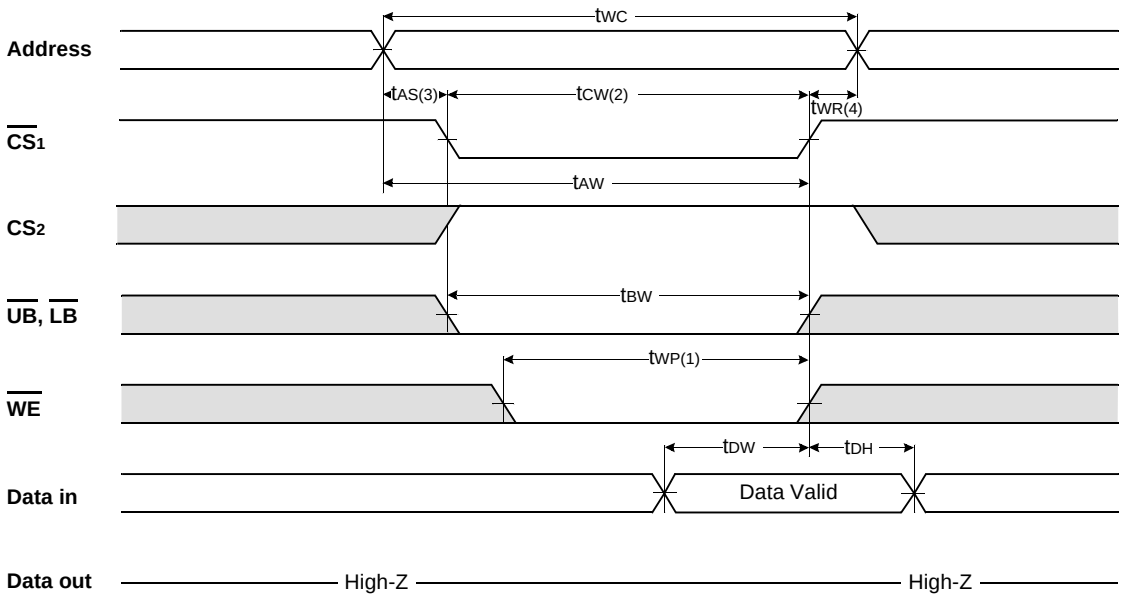

**NOTES (**READ CYCLE)

1. $t_{HZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}$(Max.) is less than $t_{LZ}$(Min.) both for a given device and from device to device interconnection.

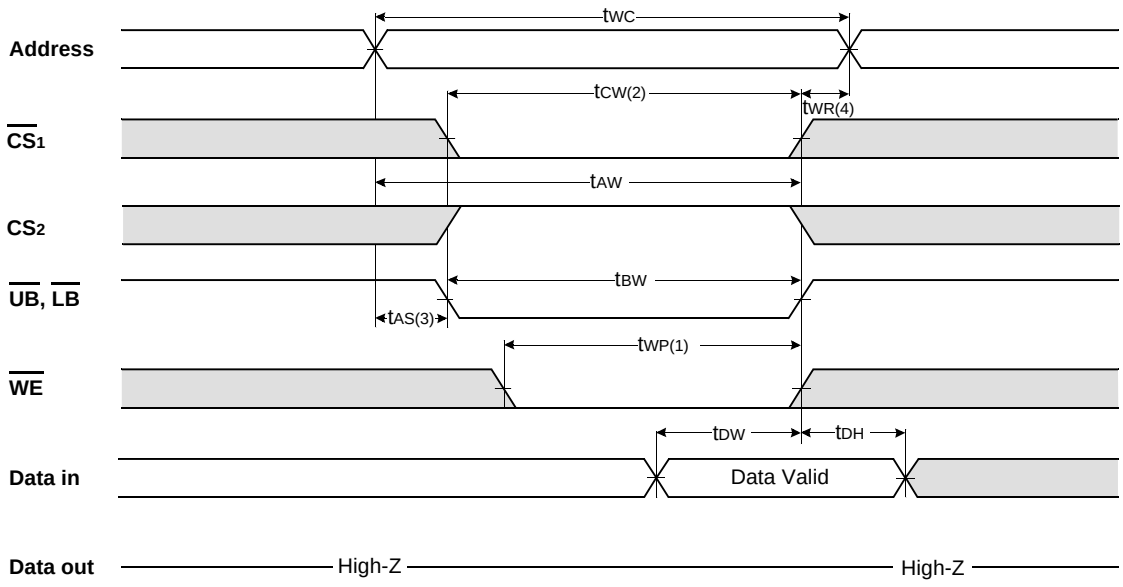
**TIMING WAVEFORM OF WRITE CYCLE(1)** ($\overline{WE}$ Controlled)




**TIMING WAVEFORM OF WRITE CYCLE(2)** ($\overline{CS_1}$ Controlled)



**TIMING WAVEFORM OF WRITE CYCLE(3)** ($\overline{UB}$, $\overline{LB}$ Controlled)

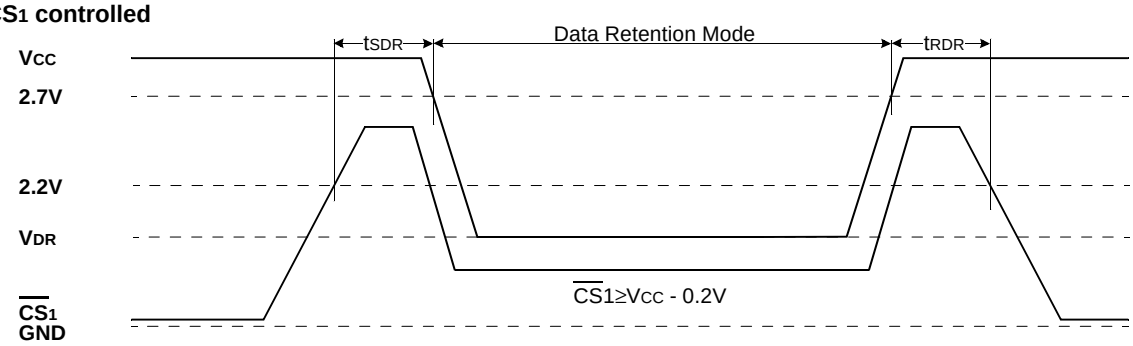



**NOTES** (WRITE CYCLE)

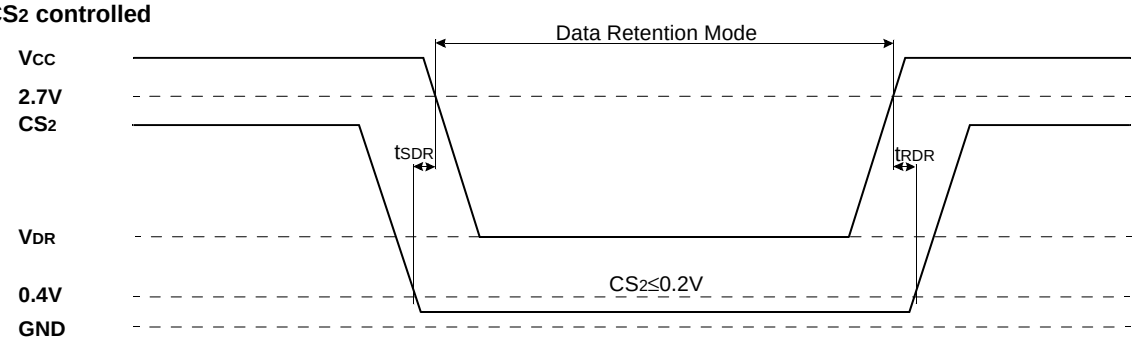
1. A write occurs during the overlap($t_{WP}$) of low $\overline{CS_1}$ and low $\overline{WE}$. A write begins when $\overline{CS_1}$ goes low and $\overline{WE}$ goes low with asserting UB or LB for single byte operation or simultaneously asserting UB and LB for double byte operation. A write ends at the earliest transition when $\overline{CS_1}$ goes high and $\overline{WE}$ goes high. The $t_{WP}$ is measured from the beginning of write to the end of write.
2. $t_{CW}$ is measured from the $\overline{CS_1}$ going low to the end of write.
3. $t_{AS}$ is measured from the address valid to the beginning of write.
4. $t_{WR}$ is measured from the end of write to the address change. $t_{WR}$ applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high.

## DATA RETENTION WAVE FORM

**$\overline{CS_1}$ controlled**




**$CS_2$ controlled**



## *NAND Flash Technical Notes*

### Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. Devices with invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

### Identifying Invalid Block(s)

All device locations are erased(FFh) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 1st & 6th word(X16 device) in the spare area. Samsung makes sure that either the 1st or 2nd page of every invalid block has non-FFFFh(X16 device) data at the column address of 256 and 261(X16 device). Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 11). Any intentional erasure of the original invalid block information is prohibited.

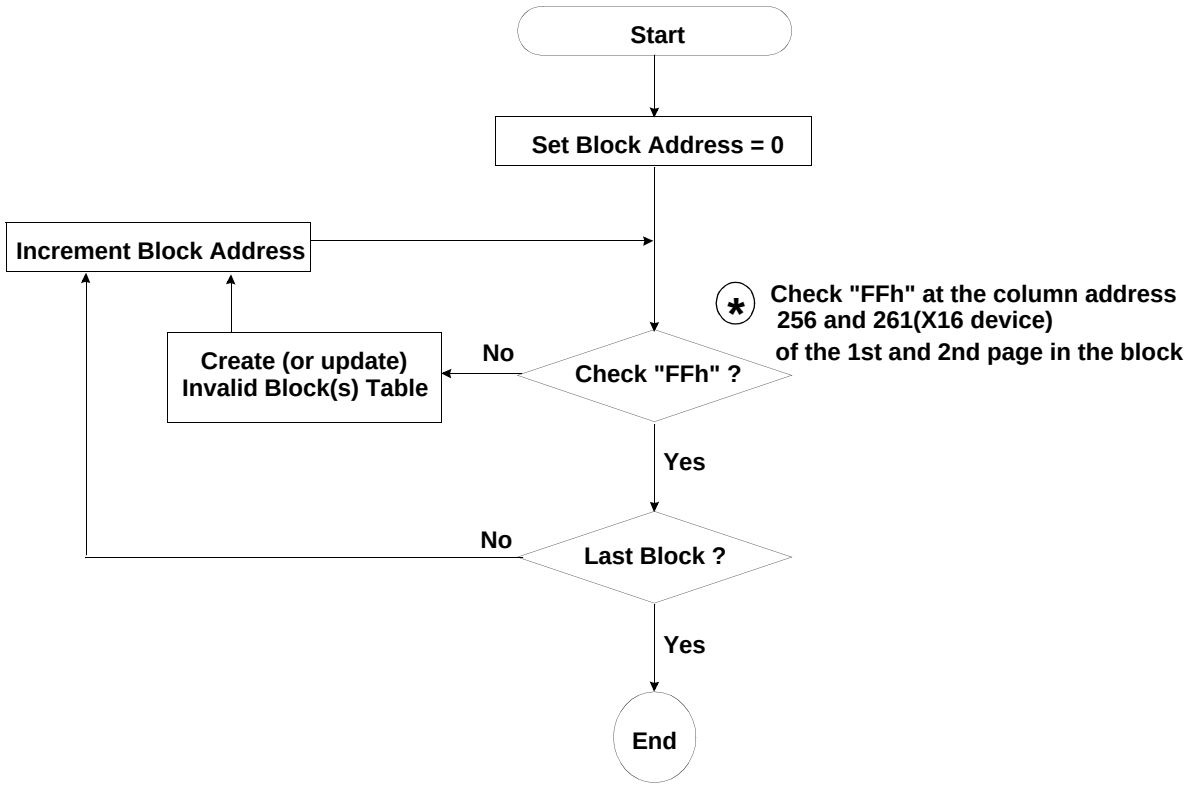



**Figure 11. Flow chart to create invalid block table.**

## *NAND Flash Technical Notes*

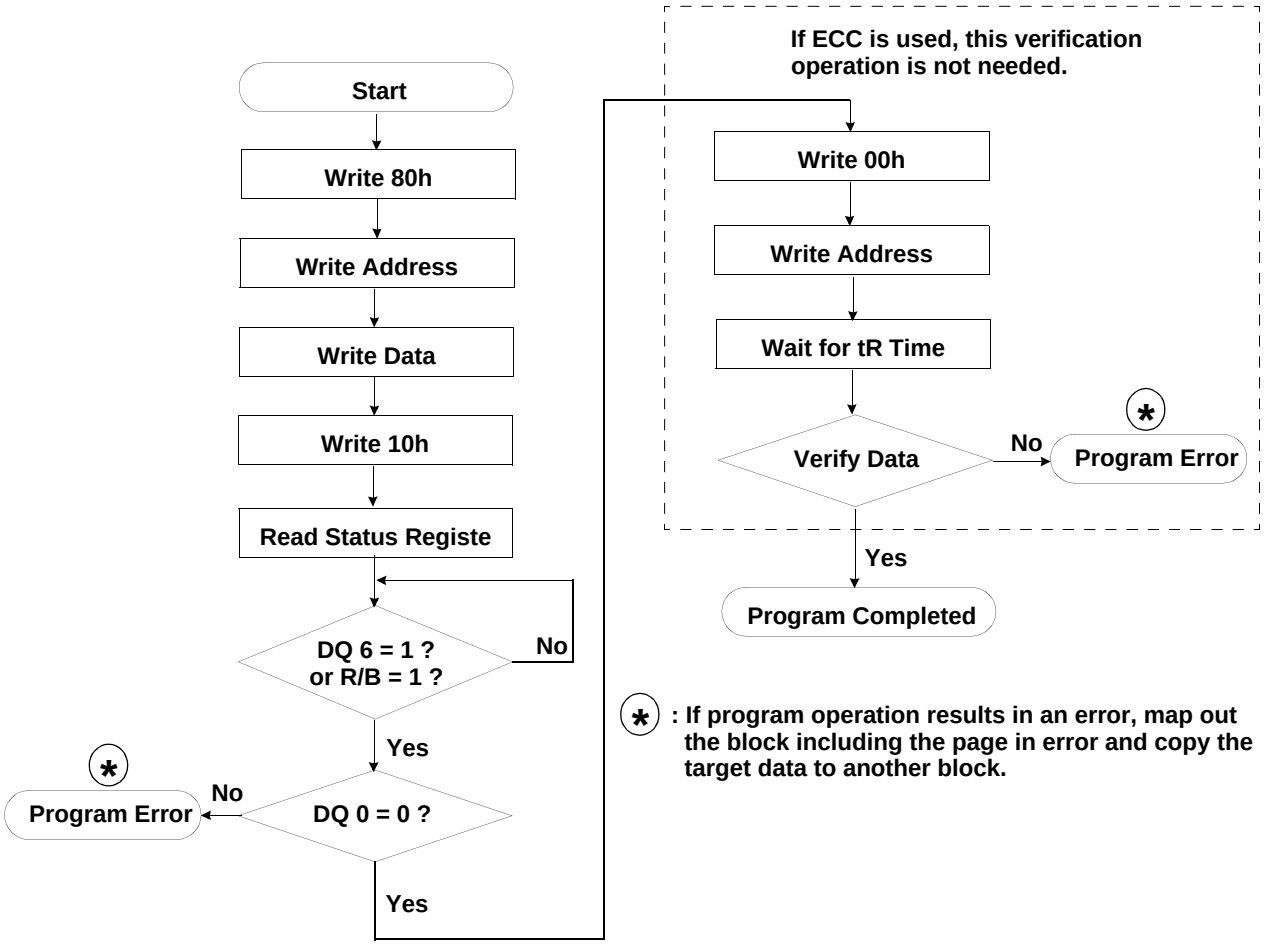
### Error in write or read operation

Over its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, so you can execute block replacement on a page basis with a page sized buffer. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

| Failure Mode | | Detection and Countermeasure sequence |
|---|---|---|
| Write | Erase Failure | Status Read after Erase --> Block Replacement |
| | Program Failure | Status Read after Program --> Block Replacement<br>Read back ( Verify after Program) --> Block Replacement<br>or ECC Correction |
| Read | Single Bit Failure | Verify ECC -> ECC Correction |

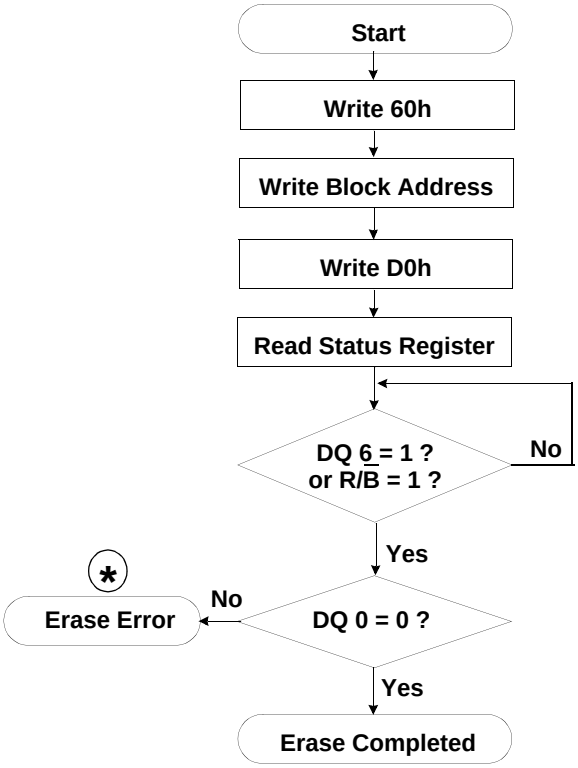
**ECC** : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

### Figure 12. Flash Program flow chart

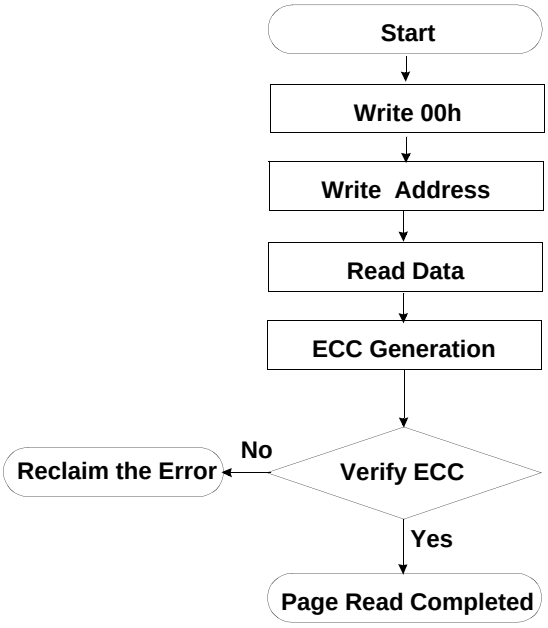


## *NAND Flash Technical Notes*

### Figure 13. Flash Erase Flow Chart

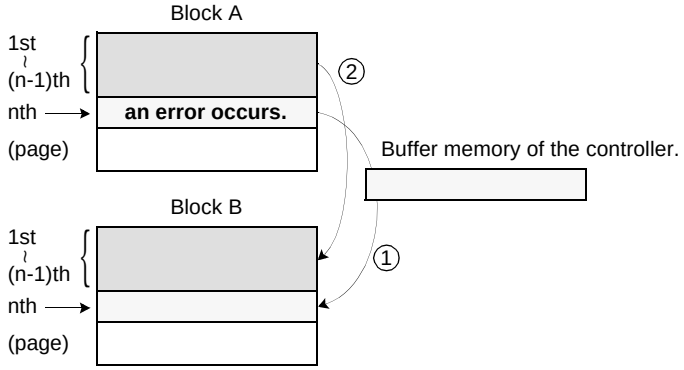



### Figure 14. Flash Read Flow Chart




(*) : If erase operation results in an error, map out the failing block and replace it with another block.

### Figure 15. Flash Block Replacement




* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the nth page data of the Block 'A' in the buffer memory to the nth page of another free block. (Block 'B')
* Step3
Then, copy the data in the 1st ~ (n-1)th page to the same location of the Block 'B'.
* Step4
Do not further erase Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

## *NAND Flash Technical Notes*

### Pointer Operation of NAND Flash

Samsung NAND Flash(x16) has two address pointer commands as a substitute for the two most significant column addresses. '00h' command sets the pointer to 'A' area(0~255word), and '50h' command sets the pointer to 'B' area(256~263word). With these commands, the starting column address can be set to any of a whole page(0~263word). '00h' or '50h' is sustained until another address pointer command is inputted. To program data starting from 'A' or 'B' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary.

**Table 7. Destination of the pointer**

| Command | Pointer position | Area |
|---|---|---|
| 00h<br>50h | 0 ~ 255 word<br>256 ~ 263 word | main array(A)<br>spare array(B) |

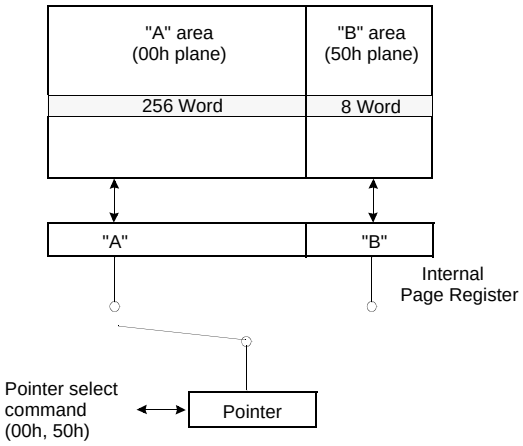
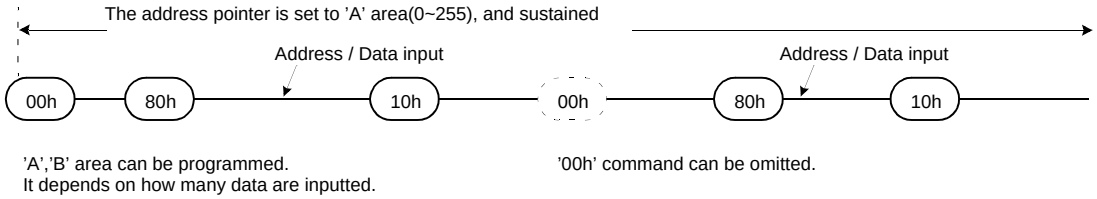
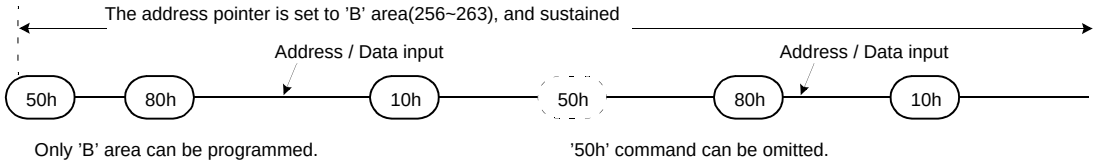



**Figure 16. Block Diagram of Pointer Operation**

**(1) Command input sequence for programming 'A' area**




**(2) Command input sequence for programming 'B' area**



## *NAND Flash Technical Notes*

### System Interface Using CE don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during data-loading or sequential data-reading as shown below. The internal 264word page registers are utilized as seperate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant saving in power consumption.

**Figure 17. Program Operation with $\overline{CE}$ don't-care.**

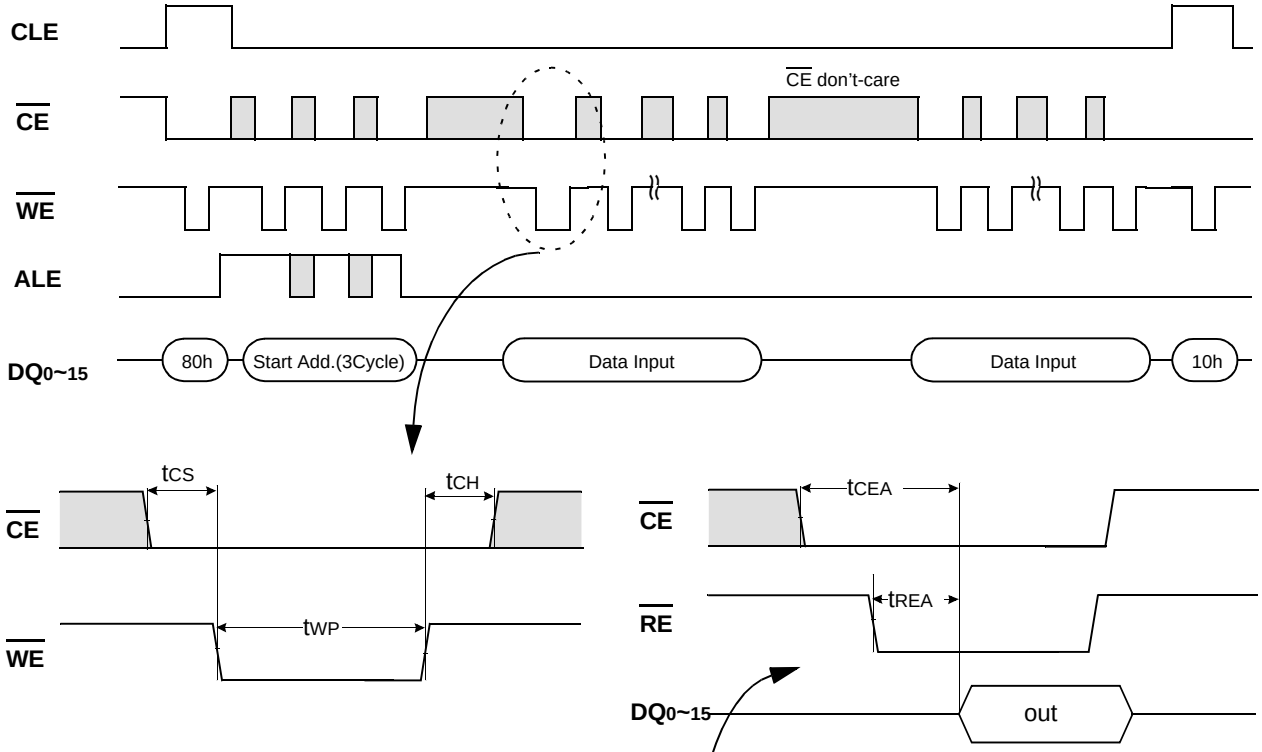
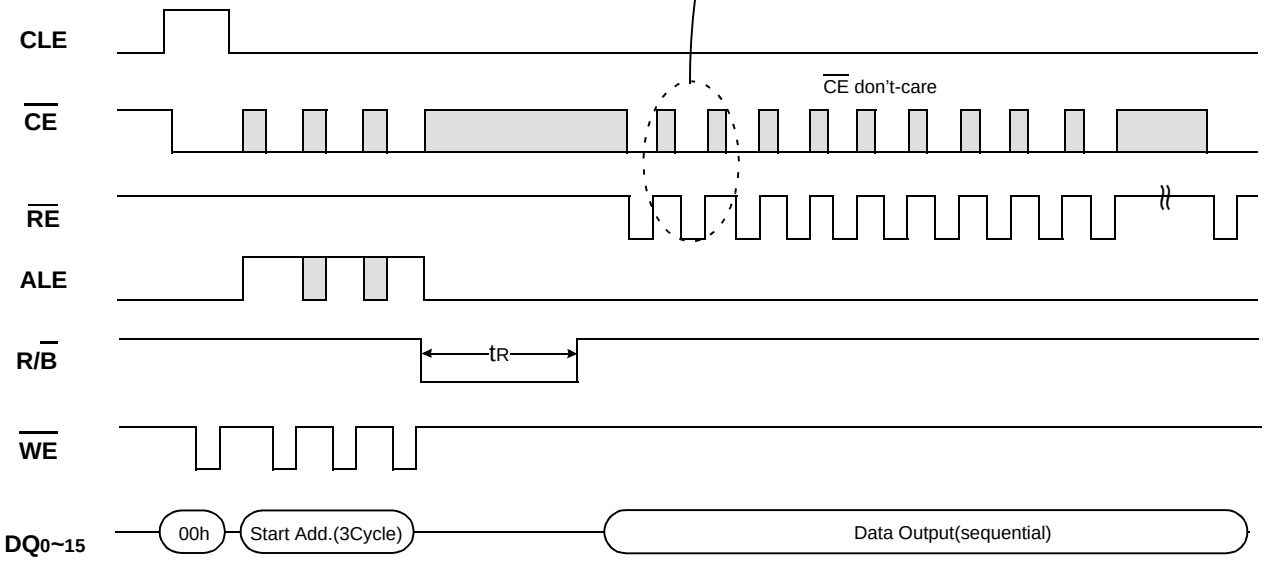



**Figure 18. Read Operation with $\overline{CE}$ don't-care.**



## PACKAGE DIMENSION

### 87-Ball Tape Ball Grid Array Package (measured in millimeters)