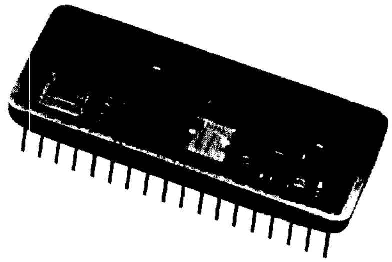
NATEL
HSRD1006

Synchro/Resolver-to-Digital Converter Microprocessor Compatible 16-bit Hybrid

Features

- **Single power supply**
  (5 V-dc nominal)
- **100 mW power dissipation**
  (20 ma @ 5 V)
- **1.3 arc-minute accuracy**
- **8- and 16-bit microprocessor compatible**
- **3-state latched output**
  (inhibit does not interrupt tracking)
- **Built-in-Test**
- **Internal reference synthesizer**
  (for improved dynamic accuracy)
- **Automatic gain control**
  (allows 2:1 signal variation)
- **Pin-programmable for synchro or resolver inputs**
- **Pin-programmable for 14-bit output**
- **3600°/sec tracking rate in 14-bit mode**
- **TTL and CMOS compatible**
- **Analog velocity and error voltage outputs**
- **Single 36-pin hybrid DDIP package**
- **MIL-STD-883 Processing is Available**
- **Priced at $595/USA price**
  (HSRD1006-149S)



ACTUAL SIZE

Applications

Avionics systems
Antenna monitoring
Servo systems
Coordinate conversion
Fire control systems
Axis rotation
Engine controllers
Industrial control systems
Simulation
Robotics
Machine tool control systems
Solar panel control systems

Description

The HSRD1006, packaged in a standard 36-pin DDIP hybrid, offers the most advanced performance features that have ever been available in Synchro/Resolver-to-Digital Converters. Additionally it operates from a single 5 V-dc power supply and consumes only 20 mA of current. The low power dissipation of 100 mW not only makes the Natel converter run cool, but it puts less strain on the user's power supply, thereby improving system MTBF. The low-power consumption and added features have been made possible by incorporating Natel designed monolithic integrated circuits in the converter. Offering high accuracy of ±1.3 arc-minutes, the converter is pin-programmable for both Synchro and Resolver inputs. Using a high accuracy differential signal conditioner for the Resolver input and resistive scott-tee for the Synchro-input, the converter provides common mode rejection in excess of 70 dB. This technique also permits resistor programming for non-standard input voltages.

Model 1006 is a Type-II tracking converter with zero velocity lag error. A programming pin is available to increase the velocity tracking of the converter to 10 rps (3600 degrees/sec) by operating it in the 14-bit mode. An internal reference synthesizer permits improved dynamic accuracy by reducing the effects of "speed voltages," at high rotational speeds. The accuracy of the converter is maintained with signal-to-reference phase shifts up to ± 45 degrees. Transferring data from the 1006 is eased through the use of a transparent latch with tri-state outputs configured as two independently enabled 8-bit bytes. Not only does this allow data to be read without interrupting converter tracking, it also permits memory-mapped data interface and control with the most popular 8- and 16-bit microprocessors and single-board computers. Logic inputs and outputs are TTL and CMOS compatible at 5 V-dc. Digital data outputs can drive one 54/74 gate load or four 54LS/74LS gate loads.

A built-in-test (BIT) feature provides a logic one when the tracking error exceeds ±1°. Monitoring of converter dynamics is facilitated through the availability of analog signals corresponding to converter tracking velocity and instantaneous tracking error.

An AGC (automatic-gain-compensation) circuit is incorporated in the converter design, which allows signal voltage variations of ± 30% without any degradation in accuracy or change in converter hysteresis.

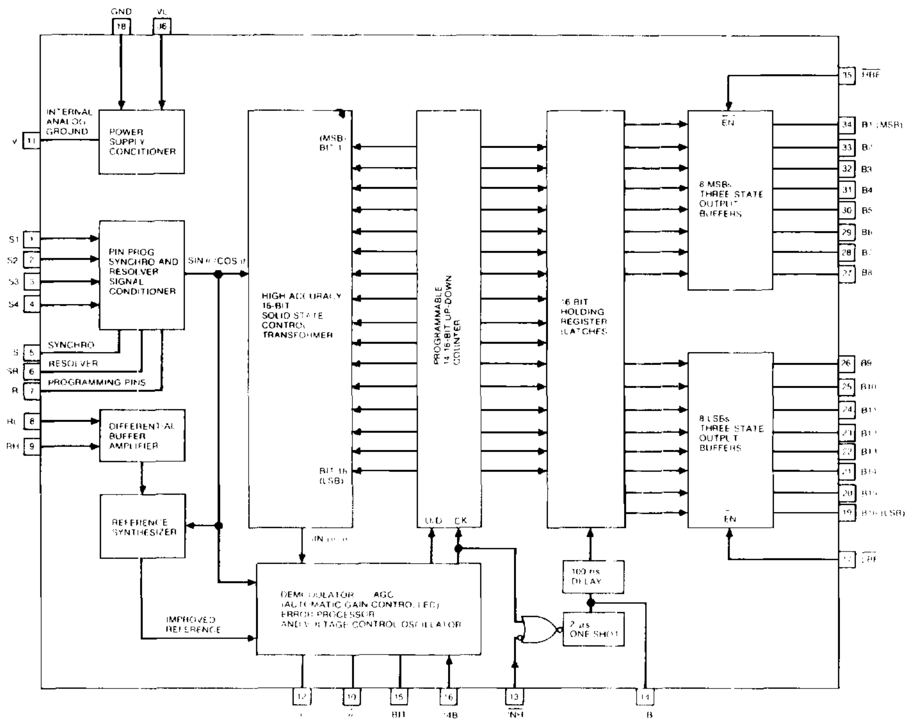


FIGURE 1 1006 Block Diagram

Theory of Operation

The operation of the Model HSRD1006 is illustrated in the functional block diagram of figure 1. The HSRD1006 is a high gain Type II tracking converter exhibiting zero error for a constant velocity input. The basic conversion process consists of continuously comparing the digital output angle (ϕ) and the Synchro (or Resolver) input angle (θ). An up-down counter, containing the feed-back angle, is changed (increased or decreased) until the feed-back angle equals the input angle. Once synchronized, the output angle tracks the input angle continuously and the data is always fresh and always available (except during transitions). The input signal conditioner accepts either a Synchro or Resolver input and converts it into low level signals $\sin\theta$ and $\cos\theta$. The feed-back loop consisting of an error processor, voltage-controlled oscillator and a 16-bit up-down counter produces a 16-bit digital angle (ϕ). The input and feed-back signals are combined in a solid state control transformer to obtain an error voltage, (e) according to the following trigonometric identity:

$$\text{"e"} = \sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

When the error voltage goes to null, $\sin(\theta - \phi)$ is zero, which makes the angle θ equal to the angle ϕ. Thus, the digital output represents the input shaft angle. The error voltage (e) is an ac signal proportional to the instantaneous error between the input angle and the feed-back angle. This error voltage is synchronously demodulated with the "synthesized reference" signal. The demodulated output is a dc signal proportional to the tracking error ($\theta - \phi$). The dc error is integrated to produce a voltage proportional to the converter's tracking velocity. The velocity signal (available at pin 10) is the control input to a voltage-controlled oscillator. The VCO output changes the up-down counter, which contains the feed back angle, ϕ. The up-down counter functions as the second integrator in the tracking loop. The output of the counter is then supplied to a holding register and dual 8-bit tri-state buffers for output interface.

Output Interface

The output interface circuit consists of a 16-bit holding register (latches) and dual 8-bit three-state buffers. This not only imparts a versatile interface capability (data multiplexing on 8- or 16-bit data bus) to the HSRD1006, but also enables the $\overline{INH}$ (inhibit) control to be used without opening the converter loop. This feature is important since synchro/resolver-to-digital converters typically disable the up-down counter during data transfer causing severe transients in the output data when the converter is re-enabled (inhibit removed) and the tracking loop is forced to re-synchronize.

When $\overline{INH}$ is at logic "high" or open, each clock pulse from the VCO changes the up-down counter by 1 LSB and triggers a one-shot to generate a 1.5-μsec pulse at CB (pin 14). The busy pulse enables the 16-bit holding register to accept the angle data from up-down counter. When CB goes "low," the data is latched in the holding register.

The outputs of the holding register are buffered with two 8-bit three-state buffers with separate enable controls. When $\overline{HBE}$ is at logic "low," the 8 MSBs (B1 through B8) are enabled. When $\overline{LBE}$ is at logic "low," the 8 LSBs (B9 through B16) are enabled. When $\overline{HBE}$ and/or $\overline{LBE}$ are at logic "high" the corresponding bits are in the high impedance state (disabled) and the data-bus sees an essentially open line.

Note that applying inhibit to the converter will latch the data in the 16-bit holding register (and will prevent it from being updated)...but will not interfere with the continuous operation of the conversion process.

Enable controls $\overline{HBE}$ and $\overline{LBE}$ operate only on three-state buffers and do not affect the converter loop.

Reference Synthesizer

To maintain the highest accuracy under both static and dynamic conditions, the HSRD1006 utilizes a monolithic "reference synthesizer" to correct for a phase difference between the signal and reference inputs of up to ±45°.

Conventional tracking synchro/resolver-to-digital converters use a phase sensitive demodulator to detect the phase and amplitude of the error voltage, sin $(\theta-\phi)$. A phase sensitive demodulator rejects any resultant quadrature signal (signal 90° out of phase) only if the synchro input and its reference are exactly in phase. A quadrature signal results from dynamic synchro operation that is referred to as the "speed voltage," and is proportional to the shaft rotational speed. Although most converter specifications discuss dynamic lag error, and ignore the error due to "speed voltages," this error is very real. For a 60 Hz synchro with a 5° phase shift rotating at 2 rps (720°/sec), the dynamic error due to speed voltage would be 0.17 degree or 10 arc-minutes!

Natel's model 1006 greatly reduces the effects of this error by creating a synthetic reference. The sine and cosine voltages from the signal conditioner are combined to obtain an in-phase internal reference. Together with the external reference voltage (to determine phase) this synthesized reference is used for demodulating the error voltage.

Built-in-Test (BIT)

A BIT signal (pin 15) provides an over-velocity or fault indication output signal. The error voltage of the converter is monitored continuously, and when the tracking error exceeds 1 degree (over-velocity or failure), a logic "1" signal is generated to indicate invalid data. Under normal operation the BIT output is at logic "0." Possible conditions that will cause the BIT output to show fault indication are:

- Power-turn-on --- BIT output will return to logic "0" when converter synchronizes to correct input angle ±1°.
- Step-input --- Instantaneous input changes greater than ±1° until the converter synchronizes.
- Synchro malfunction --- one or more open stator lines or a missing reference input.
- Converter malfunction --- any converter failure which prevents synchronization to the input angle.

From above discussion it is apparent that the BIT output not only serves to self-test the converter but also provides an indication of the operation of the synchro transmission system as well.

Improving settling time (without loss of Resolution)

Connecting the BIT output (pin 15) to 14B (pin 16) provides an interesting method for reducing settling time while maintaining 16-bit resolution during tracking. At power turn-on or for a large step input, the BIT output would be at logic "high," forcing the converter to operate in the 14-bit mode (x4 tracking rate). As soon as the output is synchronized to within ±1° of the input angle, the converter automatically reverts to 16-bit mode.

This technique, also, can be used in applications where input speeds are variable and the converter must not lose synchronization at high-speed shaft rotations.

Automatic Gain Compensation

An AGC circuit incorporated within the HSRD1006 allows the converter to maintain its high accuracy over a wider range (2 to 1) of signal amplitudes than previously possible for synchro-to-digital converters. The hysteresis of the converter is kept constant over this range.

In theory, the accuracy of an S/D or R/D converter is not affected by signal amplitude variations because the conversion process is ratiometric and therefore not dependent on the magnitude of the input. In practice, however, the necessity of providing hysteresis to prevent hunting or jitter in the least significant bit (LSB) introduces a controlled inaccuracy in the converter. In most analog-to-digital converters ≥0.5LSB hysteresis is introduced. In synchro-to-digital converters this has to be increased to approximately 0.9LSB as the error voltage is a non-linear function $[e=K\sin(\theta-\phi)]$ of the input shaft angle. Previous converters derived this hysteresis level as a fixed threshold at nominal input signal amplitude. Thus the conversion accuracy would vary directly with synchro input signal amplitude . . . becoming degraded for the lower amplitudes and creating excessive jitter for higher amplitudes.

The HSRD1006 monitors the input signals continuously and effectively modifies the gain of the error voltage as a function of input signal amplitude.

Resolution Programming

To allow speed-vs-resolution tradeoff, the HSRD1006 can be programmed for either 14-bit or 16-bit resolution. This programming function is accomplished by control 14B (pin 16). A logic "high" or an open pin at 14B makes the converter operate in the 14-bit mode (bits 15 and 16 are forced to logic "low"). A logic "low" or ground at pin 14B allows the converter to operate in the 16-bit mode. The loop gain of the converter is automatically compensated in both 14-bit and 16-bit modes, providing stable operation in both modes.

Although resolution is reduced in the 14-bit mode, the tracking speed and the acceleration constant are increased by a factor of 4 (see specifications on pages 6 and 7 for details).

Power Supply

One of the most outstanding features of Model 1006 is the single power supply requirement. The power supply voltage range depends on the desired output logic. For standard TTL operation the nominal power supply required is +5 V-dc. For CMOS logic with higher output, power supplies of up to 9 V-dc can be used. All internal circuitry is designed to operate with a power supply voltage of as low as 4.5 V-dc. This is made possible by using high signal-to-noise ratio amplifiers and a unique design approach. No performance specification is sacrificed due to low voltage power supply operation. In fact, the 1006 offers the most advanced design features ever available in any synchro/resolver-to-digital converter.

Operating with a 5 V-dc supply, the converter typically requires only 20 mA of current. 100 mW of power consumption by the converter is almost 80% less than any other converter available today, without all the performance features of 1006.

Analog Outputs

The analog outputs from the 1006 converters are $\dot{\theta}$ (pin 10) ---velocity, and e (pin 12)---the error voltage. Both $\dot{\theta}$ and e outputs are referenced to bias voltage, V_B (pin 11)---the internal ground. Both outputs can swing ±1.5 V for power supply voltage of 5 V-dc.

The bias voltage V is equal to ½ (V_L-0.7). For a power supply voltage of 5 V-dc, the bias voltage is 2.15 V-dc.

e is an ac voltage proportional to the error between synchro input angle θ and digital output angle ϕ. A 1 V-rms error signal corresponds to an error of 1°.

$\dot{\theta}$ is a dc voltage proportional to the velocity of the input shaft angle (and output digital angle). The voltage goes negative for increasing digital angle and goes positive for decreasing digital angle. A 1.1 V-dc signal corresponds to the maximum tracking rate of the converter (see specifications on pages 6 and 7). In a closed loop servo system, the velocity voltage output can be used in place of a tachometer. Scaling of both e and $\dot{\theta}$ analog outputs is independent of power supply voltage V_L.

The analog outputs are by-products of the technique used in mechanizing the conversion process and are made available. They are not closely controlled or characterized functions.

If a bipolar signal is required for either the e or $\dot{\theta}$ output, a difference circuit, as shown in figure 2, may be used. The output can be scaled to a desired value by selecting the gain of the circuit. Also if reverse polarity output is desirable, the bias and signal connections to the difference amplifier should be reversed.

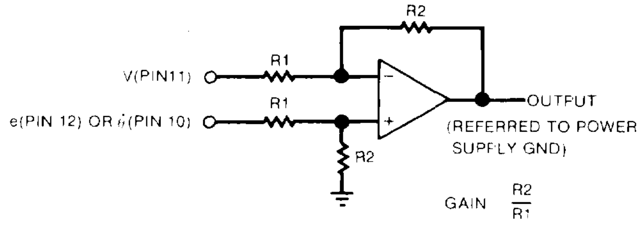


FIGURE 2 Difference Circuit for Bipolar Analog Outputs

Dynamic Performance

The HSRD1006 design incorporates the proven Type II tracking design ($K_V=\infty$) and has been configured to provide superior dynamic performance independent of power supply voltage over the range of 4.5 V-dc to 9.0 V-dc.

The converter will track the input angles up to specified tracking rates (see specifications, pages 6 and 7) with no lag error. The acceleration constant (K_A) for the converter is 190,000°/sec². Both small and large signal response for all models are shown in figure 5.

The ***Large Signal*** transient response is dependent solely on the maximum velocity (ω_{max}) and the maximum acceleration (α_{max}) of which the converter is capable. The large signal parameters are defined in figure 3. The synchronizing time (t_{SYNC}) for large signals can be partitioned into three distinct intervals, Acceleration time (t_{ACC}) Slew time (t_{SLEW}) and Overshoot time (t_{OS}).

Acceleration time is the time interval from application of the step-input to the point at which the converter reaches its maximum velocity.

Slew time is the time interval from the point at which maximum velocity is obtained to the point at which the output angle is first equal to the input angle.

Overshoot time is the time interval from the point at which the converter output angle first equals the input angle (and applies constant acceleration in the opposite direction) to the point at which the output angle again reaches the input angle.

At the end of overshoot time, the small signal response becomes dominant and the converter will settle to the final value according to its small signal transient response function.

The ***Small Signal*** settling time (t_S) is specified for step inputs of less than 1.4 degrees. For small signal steps, the settling time is a function of the transient response of the converter. The transfer functions for both 60 Hz and 400 Hz models in both 14-bit and 16-bit modes are shown in figure 4.

Typical values for all dynamic parameters for different carrier frequencies and operating modes are given in specifications on pages 6 and 7, under dynamic characteristics.

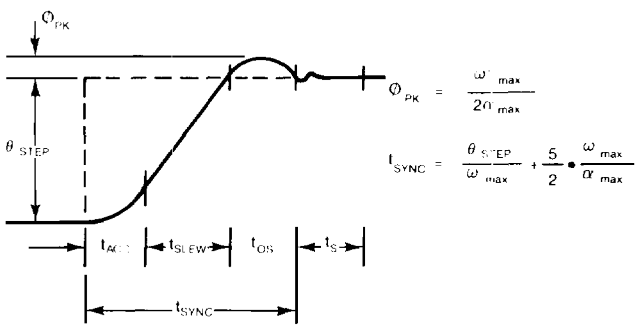
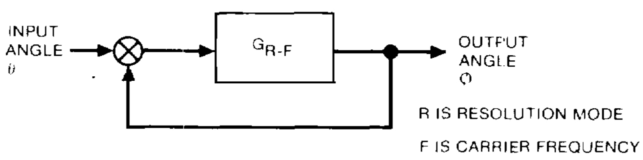


FIGURE 3 Large Signal (≥1.4°) Response Parameters



R IS RESOLUTION MODE

F IS CARRIER FREQUENCY

$$G_{14-400} = \frac{441^2\left(1+\frac{S}{100}\right)}{S^2\left(1+\frac{S}{1000}\right)} \qquad G_{14-60} = \frac{88^2\left(1+\frac{S}{20}\right)}{S^2\left(1+\frac{S}{200}\right)}$$

$$G_{16-400} = \frac{221^2\left(1+\frac{S}{100}\right)}{S^2\left(1+\frac{S}{1000}\right)} \qquad G_{16-60} = \frac{44^2\left(1+\frac{S}{20}\right)}{S^2\left(1+\frac{S}{200}\right)}$$

FIGURE 4 Transfer Functions for HSRD1006

Dynamic Performance of HSRD1006

V_L=+5V-dc , T_a=25° c

Small Signal Input Step = 0.7 Degrees

Large Signal Input Step = 179 Degrees

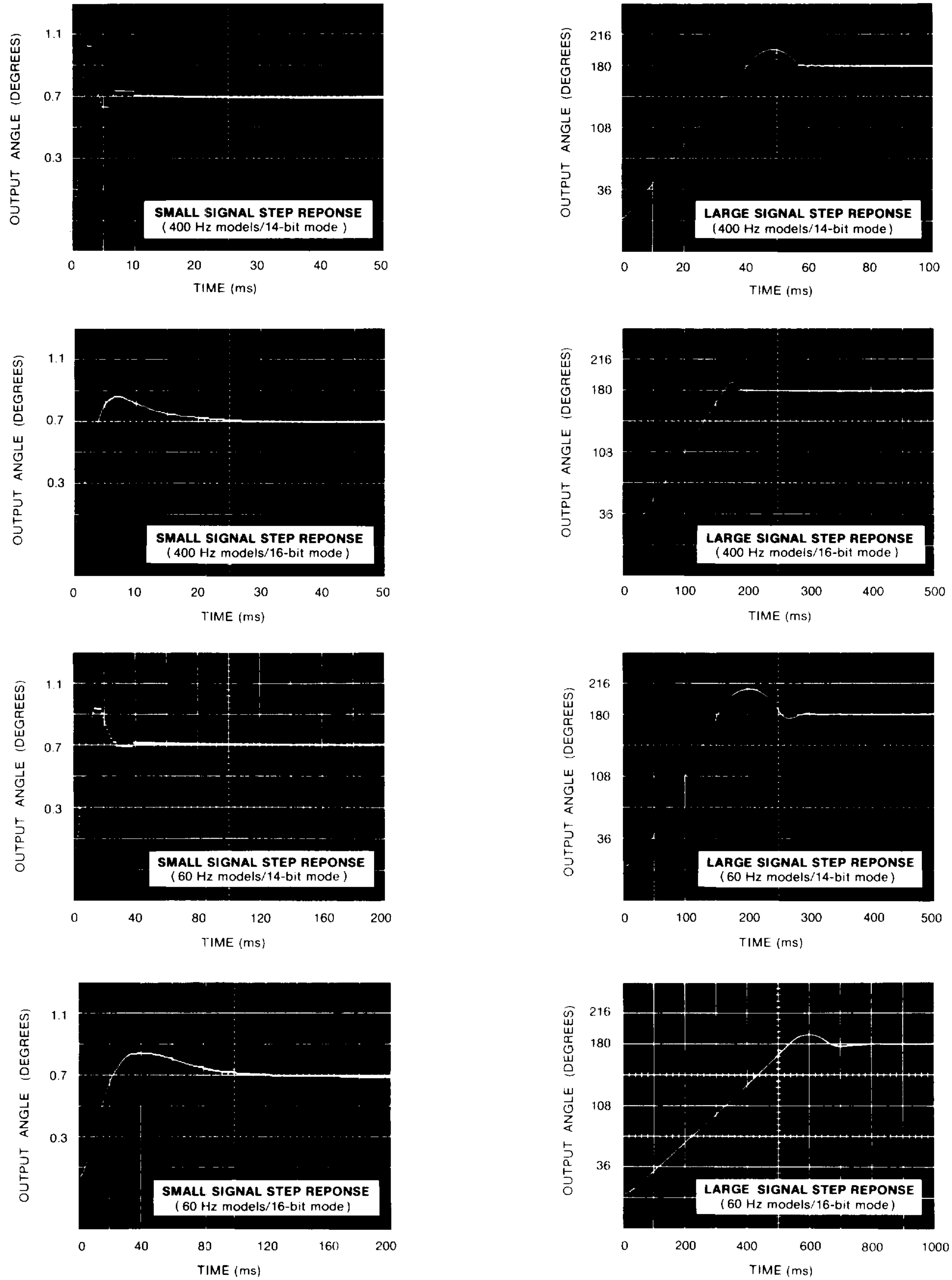


FIGURE 5 Dynamic Characteristics

Specifications

PARAMETER	VALUE	REMARKS
Digital Output Resolution	16-bits (0.33 arc-minute)	Pin-programmable for 14-bits for higher tracking speed
Accuracy	±5.2 arc-minutes (option S) ±2.6 arc-minutes (option H) ±1.3 arc-minutes (option V)	Accuracy applies over operating temperature range range and includes hysteresis
Reference Input		
Voltage	20 to 150 V-rms	
Frequency	360 to 1000 Hz 47 to 1000 Hz	400 Hz Models 60 Hz Models
Input Impedance	200 kΩ Single Ended 400 kΩ Differential	
Common Mode Range	±250 V peak maximum	dc plus recurrent ac peak
Synchro/Resolver Inputs		
Input Voltages (Line-to-Line)	11.8 V-rms ±30% 26 V-rms ±30% 90 V-rms ±30%	Accuracy of the converter is maintained with ±30% variation in signal voltages
Input Impedance	Differential / Line-to-GND 60 kΩ / 30 kΩ 150 kΩ / 75 kΩ 500 kΩ / 250 kΩ	11.8 V-rms L-L models 26 V-rms L-L models 90 V-rms L-L models
Impedance Unbalance	0.1% maximum	For all models
Common Mode Range	±30 V peak ±60 V peak ±180 V peak	11.8 V-rms models 26 V-rms models 90 V-rms models
Common Mode Rejection Ratio	70 dB minimum	dc to 1000 Hz
Harmonic Distortion	10% maximum	Without degradation in accuracy specification
Digital Inputs		CMOS transient protected
Voltage Levels Logic "0" Logic "1"	 -0.3 V-dc to 0.2 V_L 0.5 V_L to 1.0 V_L	
Input Currents $\overline{INH}$, 14B	-15 µA typical, "active" pull-up to power supply (V_L)	When not used, may be left unconnected
$\overline{HBE}$, $\overline{LBE}$	15 µA typical "active" pull-down to ground (GND)	When not used may be left unconnected
Digital Input Controls		
$\overline{INH}$	Logic "1" Logic "0"	Digital output follows analog input signals Output data latched in holding register. (Does not interrupt converter tracking-loop.)
14B	Logic "0" Logic "1"	16-bit resolution 14-bit resolution
$\overline{HBE}$	Logic "0" Logic "1"	8 MSBs are enabled 8 MSBs are in high impedance state of 3-state output
$\overline{LBE}$	Logic "0" Logic "1"	8 LSBs are enabled 8 LSBs are in high impedance state of 3-state output
Digital Outputs		
Logic Type	TTL/CMOS compatible	Depends on supply voltage (V_L)
Drive Capability Data Bits (B1-B16) CB BIT	 1 Standard TTL 1 Standard TTL 1 LSTTL or 2 LPTTL	For 5 V-dc supply voltage

PARAMETER	VALUE	REMARKS
Digital Outputs Continued		
Data Bits (B1-B16)	Natural Binary Angle	Positive Logic
CB	Logic "0" Logic "1" (1.5 μsec pulse for every LSB change)	Output angle not changing Output angle changing (Leading edge initiates output change)
BIT	Logic "0" Logic "1"	Digital output tracking analog input Fault indication (Tracking error ≥ ±1° typical)
Analog Outputs		Typical values unless otherwise specified.
V (Bias Voltage)	$(V_L - 0.7)/2$	+2.15 V-dc for +5 V-dc power supply
e (Error Voltage)	1 V-rms/1° of error	ac voltage referenced to V
$\dot{\theta}$ (Velocity Output)	1.1 V-dc/3600° per sec 1.1 V-dc/900° per sec 1.1 V-dc/720° per sec 1.1 V-dc/180° per sec	400 Hz models/14-bit mode 400 Hz models/16-bit mode 60 Hz models/14-bit mode 60 Hz models/16-bit mode
Drive Capability	1 mA maximum	
Dynamic Characteristics		Typical values unless otherwise specified.
Maximum Tracking Rate (Error < ¼ LSB)	±10 rps (3600° per sec) minimum ±2.5 rps (900° per sec) minimum ±2 rps (720° per sec) minimum ±0.5 rps (180° per sec) minimum	400 Hz models/14-bit mode 400 Hz models/16-bit mode 60 Hz models/14-bit mode 60 Hz models/16-bit mode
Maximum Acceleration	300,000°/sec² 75,000°/sec² 12,000°/sec² 3,000°/sec²	400 Hz models/14-bit mode 400 Hz models/16-bit mode 60 Hz models/14-bit mode 60 Hz models/16-bit mode
Acceleration for 1 LSB error (0.0055°/16-bit mode) (0.022°/14-bit mode)	4,200°/sec² 240°/sec² 170°/sec² 10°/sec²	400 Hz models/14-bit mode 400 Hz models/16-bit mode 60 Hz models/14-bit mode 60 Hz models/16-bit mode
Settling Time to 1 LSB (for 179° step change)	90 msec 264 msec 444 msec 1.32 sec	400 Hz models/14-bit mode 400 Hz models/16-bit mode 60 Hz models/14-bit mode 60 Hz models/16-bit mode
Settling Time to 1 LSB (small signal step ≤ 1.4°)	10 msec 35 msec 45 msec 175 msec	400 Hz models/14-bit mode 400 Hz models/16-bit mode 60 Hz models/14-bit mode 60 Hz models/16-bit mode
Reference Synthesizer Phase-shift between Input Signals and Input Reference	±45° Guaranteed ±60° Typical	Without any degradation of converter accuracy
Power Supply (V_L)		
Voltage	4.5 V-dc to 9.0 V-dc	5 V-dc ±10% for TTL compatible output
Current	20 mA typical 30 mA maximum	For 5 V-dc supply
Physical Characteristics		
Type	36 PIN Double DIP	3 standoffs are added to the package to insulate it from printed circuit board traces (standoffs included in 0.21 inch height dimension)
Size	0.78 x 1.9 x 0.21 inch (20 x 48 x 5.3 mm)	
Weight	0.6 oz (17 g) max	

Pin Designations

V_L — Power Supply Voltage
Logic Voltage
5 V-dc (For TTL compatible output)
5 V-dc to 9 V-dc (For CMOS compatible output)

GND — Power Supply Ground
Digital Ground

B1 - B16 — Parallel Output Data Bits -
B1 is MSB = 180 degrees
B16 is LSB = 0.0055 degree

S1, S2, S3, S4 — Input Analog Signals
Leave S4 unconnected for synchro-input

S, SR, R — Synchro/Resolver Programming-pins
Synchro Input - connect S to SR, leave R unconnected
Resolver Input - connect R to SR, leave S unconnected

RH, RL — Reference Voltage Input

$\dot{\theta}$ — Velocity Output -
dc analog voltage proportional to rotational speed of the input shaft angle.
Output is referenced to bias voltage (V)

V — Bias Voltage -
Internally regulated reference voltage serves as reference ground for all analog outputs.

e — Error Voltage -
ac analog voltage proportional to instantaneous tracking error of the converter.
Output is referenced to bias-voltage (V)

$\overline{INH}$ — Inhibit Function -
A logic "low" freezes the digital angular output. Internal loop keeps tracking the analog input. All other outputs keep following the input. For continuous operation this pin may be left unconnected. Internal active pull-up will apply V_L to the pin.

CB — Converter Busy -
A 1.5 μs pulse which occurs during updating of the holding register.
Output data can be transferred at the trailing edge of the CB pulse.
When converter output is not changing CB is at logic "low."

S1	1	36	V_L
S2	2	35	$\overline{HBE}$
S3	3	34	B1
S4	4	33	B2
S	5	32	B3
SR	6	31	B4
R	7	30	B5
RL	8	29	B6
RH	9	28	B7
$\dot{\theta}$	10	27	B8
V	11	26	B9
e	12	25	B10
$\overline{INH}$	13	24	B11
CB	14	23	B12
BIT	15	22	B13
14B	16	21	B14
$\overline{LBE}$	17	20	B15
GND	18	19	B16

FIGURE 6 HSRD1006 Pin Assignments

BIT — Built-in-Test -
A Logic "high" output indicates that output is not tracking the input analog signal within ±1°.

14B — Output Resolution Control -
Allows 4 times tracking speed in 14 bit-mode.
Logic "low" or ground = 16-bit output
Logic "high" or unconnected = 14-bit output
(Bits 15 and 16 will be at Logic "low")

$\overline{HBE}$ — High Byte Enable -
Data bits B1 through B8 are enabled (low-impedance state of 3-state output) when $\overline{HBE}$ is set to a logic "low." When $\overline{HBE}$ is set to a logic "high," the data bits B1 through B8 are disabled (high-impedance state of 3-state output)

$\overline{LBE}$ — Low Byte Enable -
Data bits B9 through B16 are enabled when $\overline{LBE}$ is set to a logic "low." When $\overline{LBE}$ is set to a logic "high," the data bits B9 through B16 are disabled.

Note: For continuous 16-bit parallel output $\overline{HBE}$ and $\overline{LBE}$ may be left open. Internal active pulldown to ground will apply logic "low" to these pins thus enabling all data bits B1 through B16.

Absolute Maximum Ratings

Signal Inputs	Twice Normal Voltage
Reference Inputs	200 V-rms
Supply Voltage (V_L)	+10 V-dc
Digital Inputs	-0.3 V-dc to V_L
Storage Temperature	-65° to +135° C

When installing on or removing the converter from printed circuit boards or sockets, it is recommended that the power supply and input signals be turned off. Decoupling capacitors are recommended on the power supply V_L. A 1 μF tantalum capacitor in parallel with 0.01 μF ceramic capacitor should be mounted as close to the supply pin (36) as possible.

Synchro/Resolver Connections and Phasing

The connections for synchro and resolver inputs are shown in figure 7. The input signal conditioner of the 1006 converter can be pin-programmed to accept either synchro or resolver inputs. In addition it uses differential amplifiers and matched precision resistors to provide a high common-mode rejection ratio. This eliminates the need for external transformers for most applications. The programmable input signal conditioner performs two functions. For both synchro and resolver format inputs it serves as a precision attenuator reducing the amplitude of high level ac input signals to levels which can be processed by the converter. For a synchro input, this network transforms three wire synchro information into resolver format (sin$\theta$and cosθ).

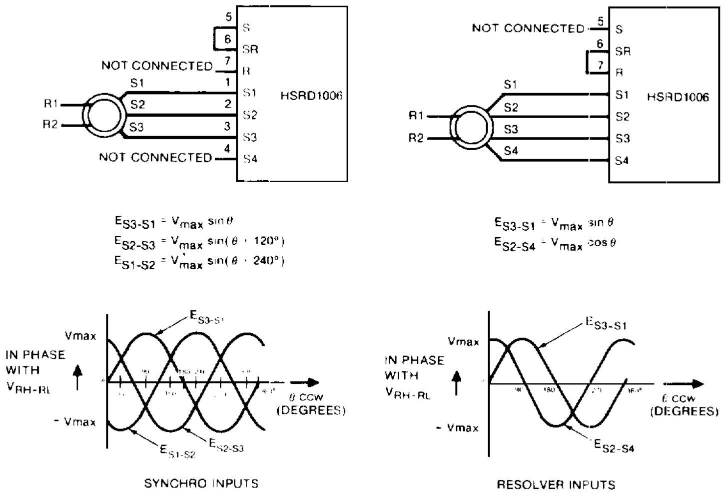


FIGURE 7 Synchro/Resolver Inputs

Resistor Programming for Non-standard Input Voltages

Non-standard input signal voltages are accommodated with the addition of external resistors connected in series with the stator input pins. The circuit configuration for resistor programming is shown in figure 8. The formula for determining the values of external resistors and the converter model numbers are shown in the table. The absolute value of the external resistors is not critical (±2%). But . . . in order to maintain converter accuracy, all resistors must be matched to within 0.01%. Also, the resistors used must have a low temperature coefficient ratio (TCR). A ratio mismatch error of 0.1% will cause a 2.1 arc-minute conversion error.

For Input Voltages, V_{in} (Line-to-Line)	Use Model Number	Resistor Value R1
11.8 V-rms to 26 V-rms	HSRD1006 - TF **1** A	R1=(3Vin-35)kΩ
26 V-rms to 90 V-rms	HSRD1006 - TF **2** A	R1=(3Vin-78)kΩ
Greater than 90 V-rms	HSRD1006 - TF **9** A	R1=(3Vin-270)kΩ

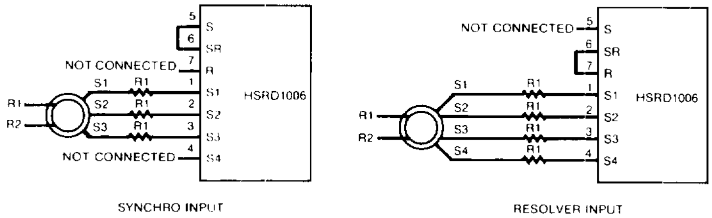


FIGURE 8 Resistor Programming for Non-Standard Inputs

Asynchronous Data Transfer

Asynchronous data transfer from the HSRD1006 is shown in figure 9. Control functions $\overline{HBE}$ and $\overline{LBE}$ have internal pull-down circuitry, permitting these pins to be left open. The data is continuously available at the output pins, but it may be changing at any specific time. In order not to transfer data during transition times, the inhibit function should be used. There are two methods available for transferring data. One method is to monitor the CB output and transfer data at the trailing edge of the CB pulse. The preferred method is on command signal. Set the $\overline{INH}$ input to logic "low" for not less than 400 ns. When the $\overline{INH}$ line goes "high," a 1.5μs busy pulse is generated. The 16-bits of output data may then be transferred on the trailing edge of CB output. For applications requiring less than 16-bit outputs, the unused lower bits should be left unconnected.

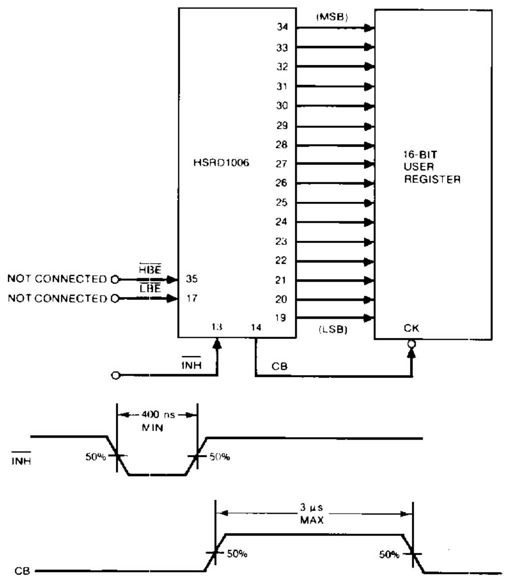


FIGURE 9 Circuit Configuration for Asynchronous Data Transfer

Dynamic Electrical Characteristics

$T_a = 25°C$ $R_L = 200\,k\Omega$ Input t_r, t_f = 20 ns V_L = 5 V-dc C_L = 50 pF

CHARACTERISTIC	LIMITS			UNITS
	MIN	TYP	MAX	
INHIBIT PULSE WIDTH, t_{PI}	400	—	—	ns
DELAY TIME, t_{PIB}	—	250	400	ns
BUSY PULSE WIDTH, t_{PB}	0.8	1.5	3.0	µs
ENABLE PULSE WIDTH, t_{PE} (HBE OR LBE)	400	—	—	ns
HIGH Z TO LOGIC "1", t_{PZH}	—	150	220	ns
HIGH Z TO LOGIC "0", t_{PZL}	—	200	300	ns
LOGIC "1" TO HIGH Z, t_{PHZ}	—	150	220	ns
LOGIC "0" TO HIGH Z, t_{PLZ}	—	200	300	ns
TRANSITION TIMES				
LOW TO HIGH, t_{TLH}	—	250	375	ns
HIGH TO LOW, t_{THL}	—	50	75	ns

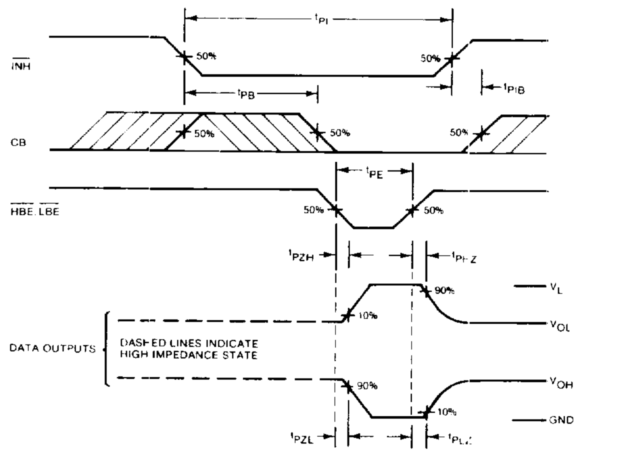


FIGURE 10 Interface Timing Diagram

Two-Byte Data Transfer On 8-Bit Data-Bus

The circuit configuration for transferring the 16-bit output of the HSRD1006 to an 8-bit data-bus is shown in figure 11. Note that INH signal, a logic "low," is applied for the entire data transfer cycle to prevent updating of internal holding register (latches). After INH is applied, wait for CB to go "low" before transferring any data. When HBE is at logic "0," the 8 MSBs are transferred to the data-bus. When LBE is at logic "0" the 8 LSBs are transferred to data-bus. Note that for the data transfer, HBE and LBE can be applied in any order.

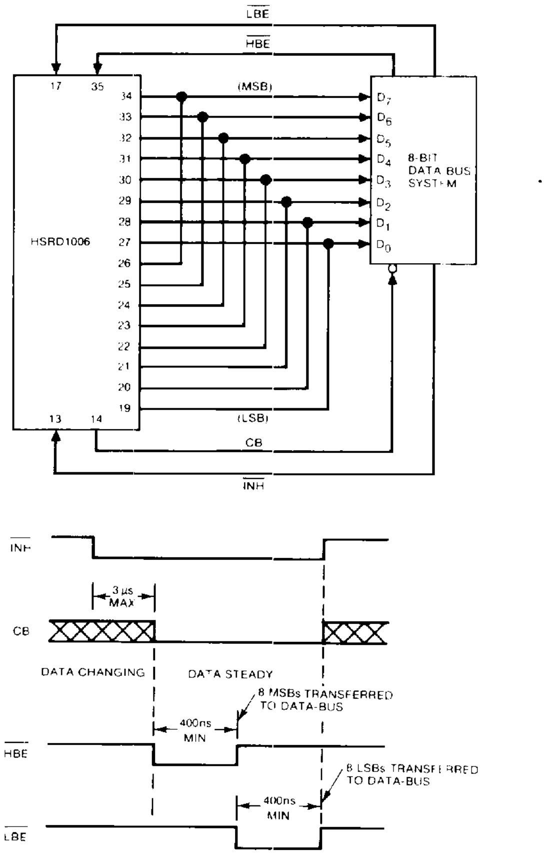


FIGURE 11 Digital Connections and Timing for Two-Byte Data Transfer

Single-Byte Data Transfer

The circuit configuration for transferring the output of the HSRD1006 to a 16-bit data-bus is shown in figure 12. Apply logic "low" to INH input. Wait for CB output to go "low" and then apply a logic low to enable inputs (HBE and LBE).

Note that as soon as the inhibit is removed, updated accurate data is latched and available for the next cycle of data transfer. This is made possible as the INH does not interrupt the conversion process. Only the holding register (latches) are prevented from updating during the time INH is at logic "low."

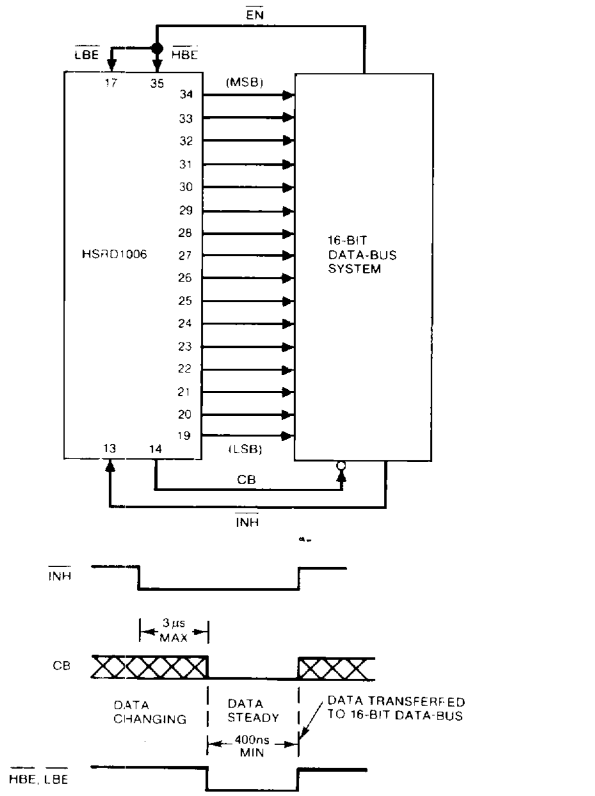


FIGURE 12 Digital Connections and Timing for Single-Byte Data Transfer

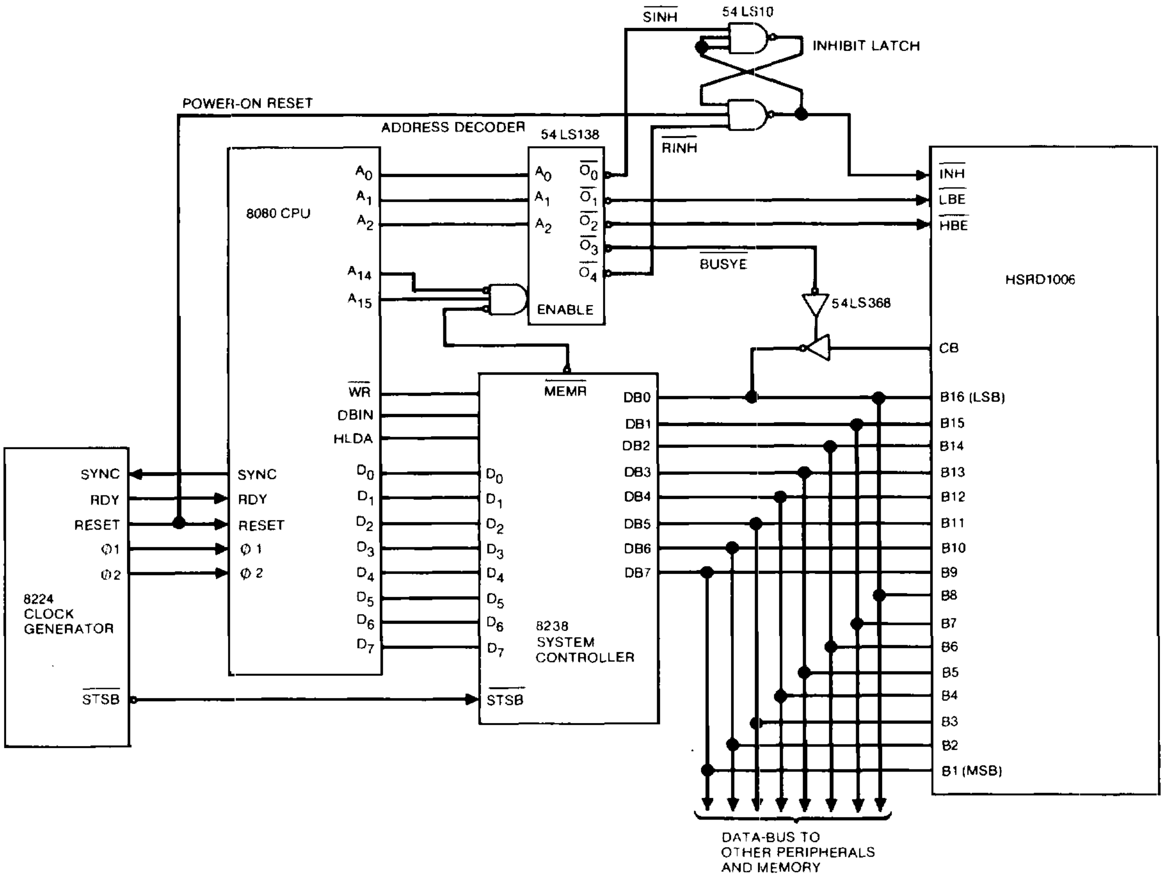


FIGURE 13 HSRD1006 Interface with 8080 μP System

```
SINH      EQU 8000H    ; ADDRESS OF INH LATCH SET
BUSYE     EQU 8003H    ; ADDRESS OF BUSYE
LBE       EQU 8001H    ; ADDRESS OF LBE
RINH      EQU 8004H    ; ADDRESS OF INH LATCH RESET
SDC IN    LXIH, INH    ; POINT H AND L TO INH AND
                       ; SET INHIBIT LATCH
          LXIH, BUSYE  ; POINT H AND L TO BUSYE
LOOP      MOV A, M     ; LOAD BUSY STATUS
          ANI, OIH     ; MASK ACCUMULATOR FOR STATUS
          JZ LOOP      ; TEST BUSY FOR "I"
          LHLD, LBE    ; LOAD H AND L WITH SDC DATA
          XCHG         ; LOAD D AND E WITH SDC DATA
          LXIH, RINH   ; POINT H AND L TO RINH AND
                       ; RESET INHIBIT LATCH
          RET          ; RETURN TO CALLING PROGRAM
```

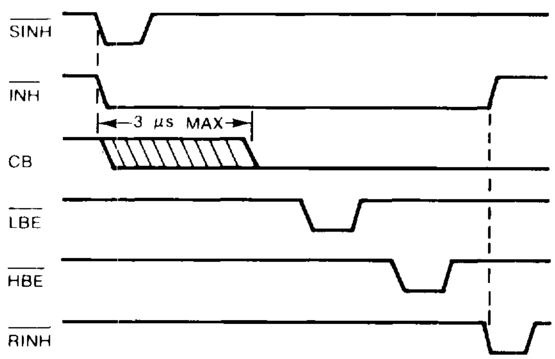
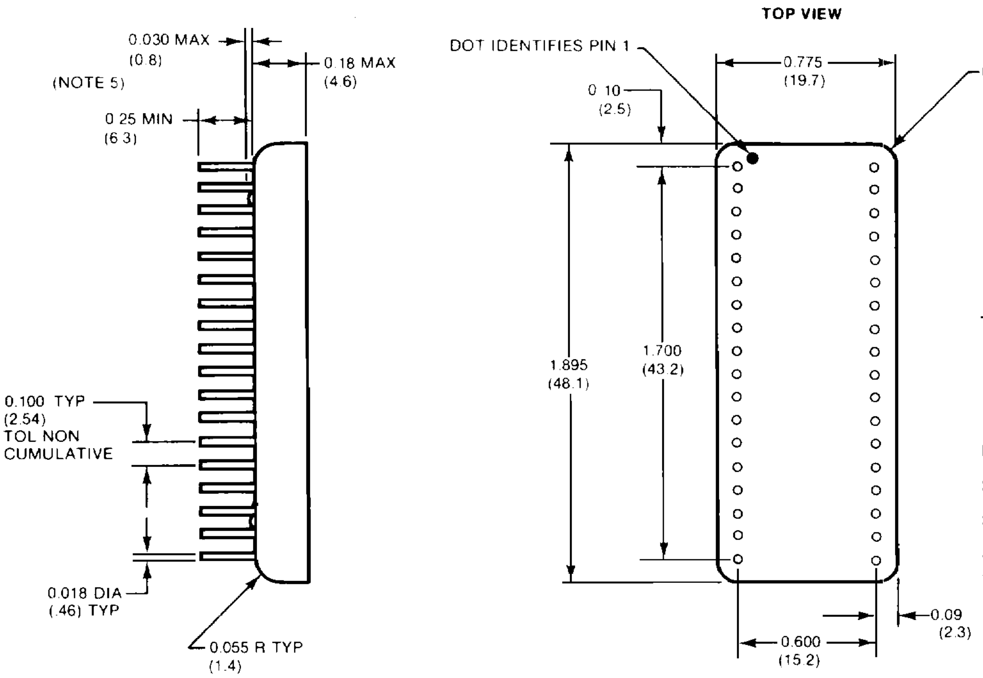


FIGURE 14 8080/HSRD1006 Interface Timing Diagram and Subroutine

8080 CPU Interface-Design Technique

A typical interface configuration for the HSRD1006 operating with an 8080 μP chipset is shown in figure 13. A typical subroutine to control the data transfer sequence is illustrated in figure 14. For simplicity this example assumes that the HSRD1006 is memory-mapped and occupies addresses 8000H through 80FFH (location 32768 through 33023). Address lines A14 and A15 enable the address decoder and successive memory locations access the converter command functions (e.g. 8003 is used to enable the CB output). In this example the μP applies an inhibit set pulse ($\overline{SINH}$) which causes the INHIBIT LATCH to set for the duration of the data transfer. A test loop is utilized that monitors the CB output of the converter. When the CB line is detected in a logic "0" condition, a 2-byte load is executed, transferring 16 bits of data into the μP's H and L registers. Since the H and L registers must be used once more to execute the reset for the INHIBIT LATCH ($\overline{RINH}$), an XCHG instruction is executed that transfers the 16 data bits to the D and E registers. The INHIBIT LATCH is then reset and the sub-routine returns execution to the calling program.

The address decoding scheme shown in figure 13 is only one of many possible alternatives. The use of more decoders will allow selection of more converters for multiple synchro applications and to more conservatively allocate portions of the memory map for memory and/or other peripherals. A 4-to-16 line decoder, for example, could more efficiently select up to 16 HSRD1006's and/or other peripherals by decoding address lines A12 through A15 into sixteen individual select lines.



TOLERANCES:

.XX = ± .01 (± .25)

.XXX = ± .005 (± .13)

NOTES:

1. CASE IS ELECTRICALLY FLOATING
2. PINS ARE KOVAR WITH GOLD PLATING: (50µINCH MIN).
3. PACKAGE IS KOVAR WITH ELECTROLESS NICKEL PLATING.
4. DIMENSIONS SHOWN IN INCHES AND (MM).
5. STANDOFFS (3) CERAMIC OR GLASS

MECHANICAL OUTLINE (36 PIN DOUBLE DIP)

Ordering Information

HSRD1006 - T F I A

Temperature Range (T)
1 = 0° C to + 70° C
2 = -25° C to + 85° C
3 = -55° C to +125° C

Frequency Range (F)
4 = 360 Hz to 1000 Hz
6 = 47 Hz to 1000 Hz

Input Signal (I)
1 = 11.8 V-rms
2 = 26 V-rms
9 = 90 V-rms
0 = Ext. Signal XFMRS
5 = Ext. Signal and Reference XFMRS

Accuracy (A)
S = ±5.2 arc-minutes
H = ±2.6 arc-minutes
V = ±1.3 arc-minutes

MIL-STD-883 COMPLIANT HYBRIDS AVAILABLE
Contact Natel Engineering for Delivery

Other Hybrid products now in 36 pin DDIP size:

- 16-bit microprocessor-compatible digital to synchro/resolver converter with double buffered inputs and 1 arc-minute accuracy (HDSR2006).
- 14-bit digital-to-synchro/resolver converter that is pin-compatible with existing designs with transformation and angular accuracy improvement of a factor of 2 to 4 (HDSR2504)

Other Hybrid products to be introduced in the next six months:

- 14-bit synchro/resolver-to-digital converters pin-compatible with existing designs, but with superior performance
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