HARRIS SEMICONDUCTOR

HS-6514RH

Radiation Hardened 1024 x 1 CMOS RAM

December 1992

Features

- Total Dose 1 x 10^5 RAD (SI)
- Data Upset > 10^8 RAD (SI)/s
- Latch-Up Free To > 1 x 10^{12} RAD (SI)/s
- Low Power Standby 1100µW Max
- Low Power Operation 38.5mW/MHz Max
- Fast Access Time 150ns Typ
- Single Event Upset Immune Option
- TTL Compatible Output
- Common Data I/O
- Three-State Outputs
- Standard JEDEC Pinouts
- 18 Pin Package for High Density
- On-Chip Address Register
- Military Temperature Range -55°C to +125°C

Description

The HS-6514RH is a synchronous 1024 x 1 static CMOS RAM fabricated using the radiation hardened guard band ring, self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices. On-chip latches are provided for addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

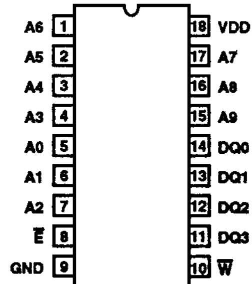
The HS-6514RH is a fully static RAM and may be maintained in any state for an indefinite period of time. A single event upset immune version of the HS-6514RRH is also offered.

JAN

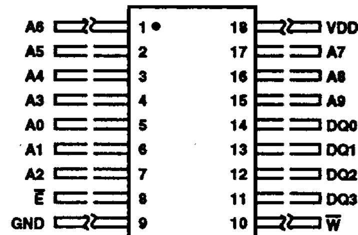
On January 28, 1987, Harris received JAN line certification as a Rad-Hard Class S fabrication facility for the HS-6514RH. Specifications can be found in JAN 38510/245 under device type 04.

Pinouts

HS1-6514RH 18 PIN CERAMIC DIP
CASE OUTLINE D-6, CONFIGURATION 3
TOP VIEW



TOP VIEW
HS9-6514RH 18 LEAD FLATPACK
INTERNAL PACKAGE CODE "HRF"
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DQ	Data In/Out

8 MEMORIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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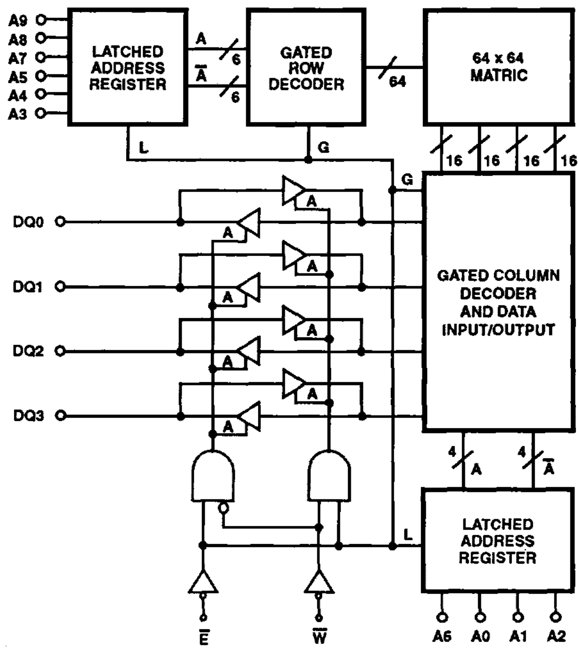
File Number 3029

Functional Diagram



All Lines Active High - Positive Logic
Three-State Buffers: A High Output Active
Address Registers: Latch on Rising Edge of L
Gated Decoders: Gate on Rising Edge of G

Absolute Maximum Ratings

Supply Voltage -(VDD-GND) .... -0.3 to +7.0V
Input or Output Voltage Applied .... GND-0.3V to VDD +0.3V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering 10s).................... +300°C
Typical Derating Factor........... 3.0mA/MHz Increase in IDDOP
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
18 Pin Ceramic DIP Package	73°C/W	10°C/W
18 Lead Flatpack Package	62°C/W	10°C/W

Maximum Package Power Dissipation at +125°C
18 Pin Ceramic DIP Package 0.68W
18 Lead Flatpack Package 0.80W
Gate Count .... 6672 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range .... +4.5V to +5.5V
Operating Temperature Range................. -55°C to +125°C
Input Rise and Fall Time .... 40ns Max

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Standby Supply Current	IDDSB	IO = 0, VI = GND or VDD	-	200	µA
Operating Supply Current (Note 1)	IDDOP	f = 1MHz, IO = 0, VI = VDD or GND	-	7	mA
Data Retention Supply Current	IDDDR		-	100	µA
Data Retention Supply Voltage	VDDDR		-	3.0	V
Input Leakage Current	II	GND ≤ VI ≤ VDD	-1.0	+1.0	µA
Output Leakage Current	IOZ	GND ≤ VO ≤ VDD	-10	+10	µA
Input Low Voltage	VIL		0.0	0.8	V
Input High Voltage	VIH		VDD -2.0	VDD	V
Output Low Voltage	VOL	IOL = 2.0mA	-	0.4	V
Output High Voltage	VOH	IOH = -1.0mA	2.4	-	V

NOTE:
1. Operating Supply Current (IDDOP) is proportional to Operating Frequency.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Chip Enable Access Time	TELQV	Note 1	-	225	ns
Address Access Time	TAVQV	Note 1	-	235	ns
Chip EnableTime	TELEH	Note 1	225	-	ns
Chip Disable Time	TEHEL	Note 1	75	-	ns
Address Setup Time	TAVEL	Note 1	10	-	ns
Address Hold Time	TELAX	Note 1	50	-	ns
Write Enable Pulse Width	TWLWH	Note 1	225	-	ns
Write Enable Setup Time	TWLEH	Note 1	225	-	ns
Write Enable Hold Time	TELWH	Note 1	225	-	ns
Data Setup Time	TDVWH	Note 1	190	-	ns
Data Hold Time	TWHDZ	Note 1	50	-	ns

NOTE:
1. Inputs TRISE = TFALL ≤ 20nsec: Outputs : 1TTL load and 50pF. All timing measurements at 1/2 VDD.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed but not tested)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Input Capacitance	CI	VI = VDD or GND	-	8.0	pF
Output Capacitance	CO	VO = VDD or GND, f = 1MHz	-	10.0	pF
Chip Enable/Output Enable Time	TELQX	Note 1	5	-	ns
Chip Enable/Output Disable Time	TEHQZ	Note 1	-	75	ns
Write Enable/Output Disable Time	TWLQZ	Note 1	-	75	ns
Early Output High Z Time	TWLEL	Note 1	0	-	ns
Late Output High Z Time	TEHWH	Note 1	0	-	ns
Read or Write Cycle Time	TELEL	Note 1	300	-	ns

NOTE:

1. Inputs TRISE = TFALL ≤ 20nsec: Outputs : 1TTL load and 50pF. All timing measurements at 1/2 VDD.

TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 0.08V
Output High Voltage	VOH	± 0.48V
Input Leakage Current	II	± 0.20µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test 1 and 2		100%/5004	1, 7, 9	N/A
PDA 1 and 2		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

Absolute Maximum Ratings

Supply Voltage -(VDD-GND) .... -0.3 to +7.0V
Input or Output Voltage Applied ....GND-0.3V to VDD +0.3V
Storage Temperature Range .... -65°C to +150°C
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Lead Temperature (Soldering 10s)................... +300°C
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Thermal Resistance	θ_{ja}	θ_{jc}
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CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

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Operating Temperature Range.................. -20°C to +80°C
Input Rise and Fall Time .... 40ns Max

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Write Enable Setup Time	TWLEH	Note 1	225	-	ns
Write Enable Hold Time	TELWH	Note 1	225	-	ns
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TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
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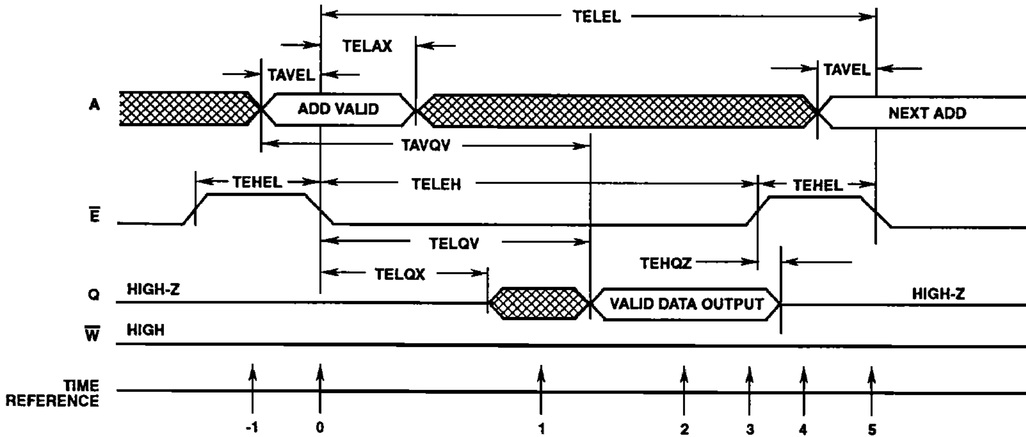
Interim Test 1 and 2		100%/5004	1, 7, 9	N/A
PDA 1 and 2		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

Timing Waveforms

READ CYCLE



TRUTH TABLE

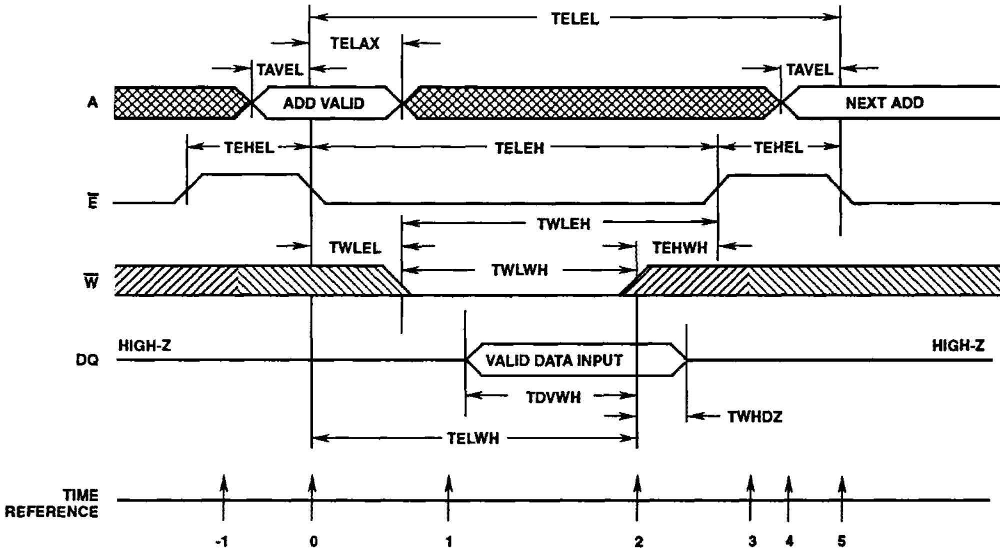
TIME REFERENCE	INPUTS			OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	DQ	
-1	H	X	X	Z	Memory Disabled
0	↓	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↑	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but the data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

NOTE: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Timing Waveforms (Continued)

WRITE CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	OUTPUT DQ	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↘	X	V	Z	Cycle Begins, Addresses are Latched
1	L	L	X	Z	Write Period Begins
2	L	↗	X	V	Data In is Written
3	↗	H	X	Z	Write Completed
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the addrss information in the on chip registers. There are two basic types of write cycle, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls.

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before $\overline{E}$. The RAM outputs will disable (three-state) after $\overline{E}$ rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rises.

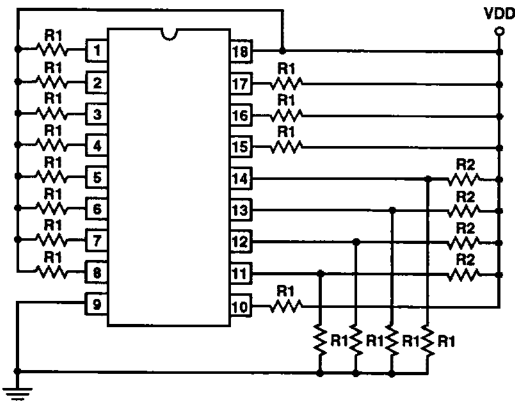
This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data output will stay disable throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDZ become TDVEH and TEHDZ. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ and $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

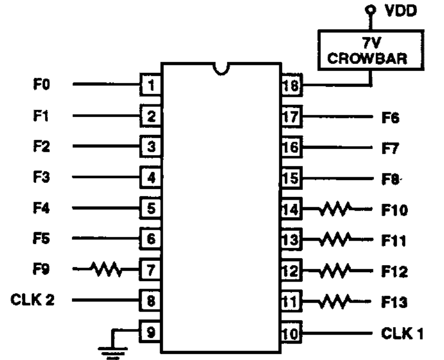
NOTE: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

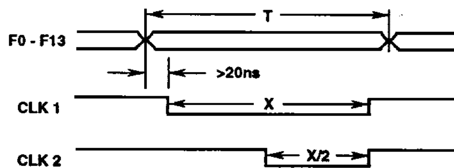
Burn-In Circuits



STATIC CONFIGURATION

NOTES:
VDD = 6.0V ± 0.5V
R1 = 1K
R2 = 1.5K
Minimum Ambient Temperature = +125°C

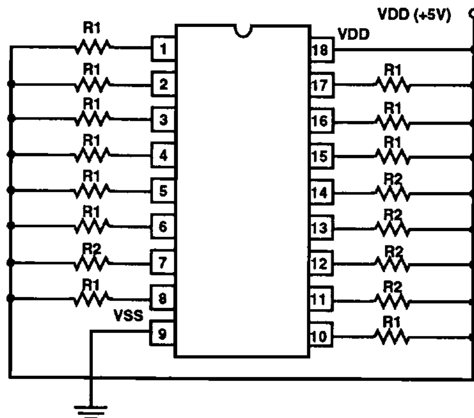




DYNAMIC CONFIGURATION

NOTES:
VDD = 6.0V ± 0.5V
All Resistors = 27KΩ
Minimum Ambient Temperature = +125°C
VDD must be applied before or at the same time as input signals
x > 700ns, T = 5μs
F0 = 100kHz
F1 = F0/2
F2 = F0/4
F3 = F0/8 . . . F13 = F0/8192

Irradiation Circuit



NOTES:
VDD = 5V
VSS = 0V
All Inputs = 5V
MONITOR: IDD at 5V
R1 = 47KΩ and R2 = 2.7KΩ

Harris - Space Level (-Q) Product Flow (Note 1)

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection Method 2010, Condition A
Gamma Radiation Assurance Tests Method 1019
Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 2)
Temperature Cycling Method 1010, Condition C
Constant Acceleration Method 2001, Condition E Min, Y1
Particle Impact Noise Detection Method 2020, Condition A
Electrical Tests (Harris' Option)
Serialization
X-Ray Inspection Method 2012
Electrical Tests - Subgroup 1; Read and Record (T0)
Static Burn-In Method 1015, Condition B, 72 Hrs, +125°C Min.
Interim 1 Electrical Tests - Subgroup 1; Read and Record (T1)
Burn-In Delta Calculation (T0 -T1)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Dynamic Burn-In Method 1015, Condition D, 240 Hrs, +125°C (Note 3)
Interim 2 Electrical Tests - Subgroup 1; Read and Record (T2)
Alternate Group A - Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Electrical Tests - Subgroup 3; Read and Record
Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1
Marking
Electrical Tests - Subgroup 2; Read and Record
Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1
Gross Leak Tests Method 1014, 100%
Fine Leak Tests Method 1014, 100%
Customer Source Inspection (Note 2)
Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters: B-5 - Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11; B-6 - Subgroups 1, 7, 9
Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9
External Visual Inspection Method 2009
Data Package Generation (Note 5)

NOTES:
1. The notes of Method 5004, Table 1 shall apply; Unless Otherwise Specified.
2. These steps are optional, and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015.
4. For Group D, Subgroup 3 inspection of package configurations which utilizes a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (Including SEM Report)
   X-Ray Report and Film
   Test Variables Data

Harris -8 Product Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010, Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In Method 1015, Condition D, 160 Hrs, +125°C
+25°C Electrical Tests - Subgroups 1, 7, 9
PDA Calculation 5% Subgroups 1, 7
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:
1. These steps are optional, and must be negotiated as part of order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper)

Metallization Topology

DIE DIMENSIONS:
Die Size: 155 x 237 mils
Die Thickness: 14 ±1 mils

METALLIZATION:
Type: Al, 14kÅ ± 2kÅ
Back: Gold

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold
Temperature: Sidebrazed Ceramic DIP - 460°C±10°C (Max)
Braze Seal Flatpack - 460°C ± 10°C (Max)

WORST CASE CURRENT DENSITY: 4.37×10^4 A/cm^2

SUBSTRATE POTENTIAL: VDD

Metallization Mask Layout

HS-6514RH