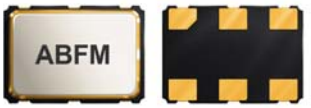
CERAMIC SMD CRYSTAL CLOCK OSCILLATOR



5.0 x 7.0 x 1.8mm

ABFM SERIES : PRELIMINARY

FEATURES:

- Based on a proprietary analog multiplier
- Tri-State Output
- Ultra low Phase Jitter
- 125MHz, 156.25MHz, 187.5MHz, and 212.5MHz applications
- 2.5V to 3.3V +/- 10% operation
- Ceramic SMD, low profile package

APPLICATIONS:

- Fiber Channel
- 12Gbit SERDES
- 10Gbit SERDES
- PCI Express

STANDARD SPECIFICATIONS:

PARAMETERS	
Frequency Range	150 MHz to 280 MHz
Operating Temperature	0°C to + 70°C (see options)
Storage Temperature	- 55°C to + 125°C
Overall Frequency Stability	± 50 ppm max. (see options)
Supply Voltage (Vdd)	2.25V - 3.63 V
Jitter (12KHz - 20MHz)	RMS phase jitter < 0.3pS period jitter < 20pS peak to peak typical
Low Phase Noise	-130 dBc/Hz @ 1kHz Offset from 212.5MHz -140 dBc/Hz @ 10kHz Offset from 212.5MHz -145 dBc/Hz @ 100kHz Offset from 212.5MHz
Aging (PPM/year)	TBD Per Crystal
PECL	
Supply Current (I_{DD})[Fout = 212.50MHz]	85mA max.
Output Clock Duty Cycle @ V_{DD}-1.3V	45% min, 50% typical, 55% max.
Output High Voltage	V_{OH} = (VDD-1.025V min)
Output Low Voltage	V_{OL} = (VDD-1.620V max)
Clock Rise time (t_r) @ 20/80%	0.2ns typical, 0.5ns max,
Clock Fall time (t_f) @ 80/20%	0.2ns typical, 0.5ns max
LVDS	
Supply Current (I_{DD}) [Fout = 212.50MHz]	55mA typical, 60mA max
Output Clock Duty Cycle @ 1.25V	45% min, 50% typical, 55% max
Output Differential Voltage (V_{OD})	247mV min, 355mV typical, 454mV max
VDD Magnitude Change (ΔV_{OD})	-50mV min, 50mV max
Output High Voltage	V_{OH} = 1.4V typical,1.6V max
Output Low Voltage	V_{OL} = 0.9V min, 1.1V typical
Offset Voltage [R_L = 100Ω]	V_{OS} = 1.125V min, 1.2V typical, 1.375V max
Offset Magnitude Voltage[RL = 100Ω]	ΔV_{OS} = 0mV min, 3mV typical, 25mV max
Power-off Leakage (I_{OXD}) [Vout=VDD or GND, VDD=0V]	±1µA typical, ±10µA max
Output Short Circuit Current (I_{OSD})	-5mA typ, -8mA max.
Differential Clock Rise Time (t_r) [R_L=100Ω, CL=10pF]	0.2ns min, 0.5ns typical, 0.7ns max
Differential Clock Fall Time (t_f) [R_L=100Ω, CL=10pF]	0.2ns min, 0.5ns typical, 0.7ns max

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ABFM SERIES : PRELIMINARY

5.0 x 7.0 x 1.8mm

STANDARD SPECIFICATIONS:

CMOS	
Supply Current (I_{DD})[at 100MHz, load 15pF]	16mA typ., 20mA max.
Output Clock Duty Cycle @ 50%V_{DD}	45% min, 50% typical, 55% max.
Output High Voltage (V_{OH}) [I_{OH} = -8.5mA]	2.4 min
Output Low Voltage (V_{OL}) [I_{OL} = 8.5mA]	0.4V max
Output Drive Current (I_{OSD}) [V_{OL} = 0.4V, V_{OH} = 2.4V]	8.5mA typ.
Output Clock Rise/Fall time [10% ~ 90% VDD w/10pF load]	1.2nS typical, 1.6nS max.
Output Clock Duty cycle [Measured @ 50% VDD]	45% min, 50% typical, 55% max.

MARKING:

- TUH — Frequency: T=First "ten" digit of frequency, U=First "unit" of frequency, H=First "tenth" digit of freq, Ex: 100 for 10.0MHz; 143 for 14.31818 MHz)
- ABFM ZYX — (Z: Month, A to L; Y: Year, 5 for 2005; X: Traceability Code)

PIN ASSIGNMENTS:

PIN #	NAME	DESCRIPTION
1	Tri-state	Tri-state
2	NC	No Connect
3	GND	Ground
4	Q	PECL, LVDS
5	$\overline{Q}$	Complimentary PECL, LVDS
6	V_{DD}	VDD Connection

TRI-STATE PIN OPERATION:

OUTPUT TYPE OPTION		PIN 1 LOGIC LEVEL*	OUTPUT STATE
P	PECL	0 (Default)	Enabled
		1	Tri-state
P1	PECL1	1	Enabled
		0	Tri-state
V	LVDS	0	Tri-state
		1 (Default)	Enabled
C	CMOS	0	Tri-state
		1 (Default)	Enabled

*Connect to VDD from logic level "1", connect to ground for logic level "0".

OPTIONS AND PART IDENTIFICATION (Left blank if standard):

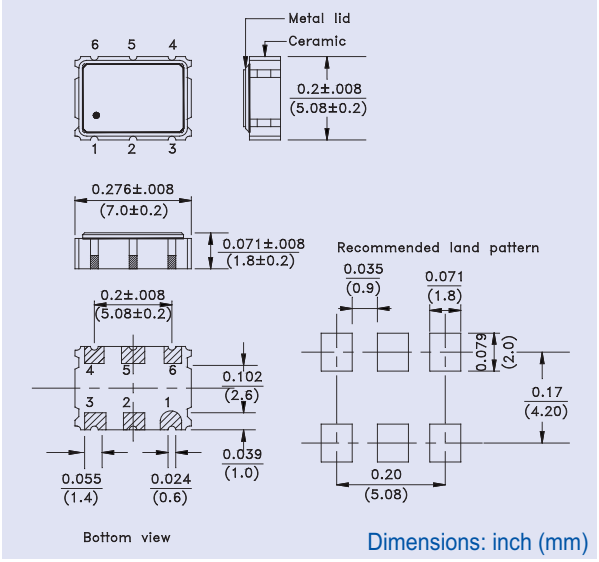
ABFMX - Frequency - Temperature - Frequency Stability - Output - Tri-state pin output - Packaging

Vdd options:
Blank (3.3Vdc±10%V)
1 (2.5Vdc±10%V)

Stability options:
R for ± 25 ppm max

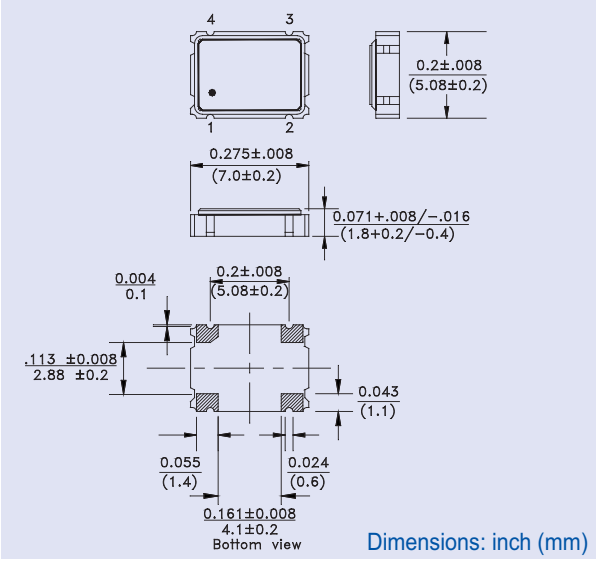
Packaging option:
T for Tape and Reel (1,000pcs/reel)
T5 for Tape and Reel (500pcs/reel)

PECL & LVDS DRAWING:



Dimensions: inch (mm)

CMOS DRAWING:



Dimensions: inch (mm)

PIN #	NAME
1	Tri-state
2	GND/Case
3	Output
4	Vdd

ABRACON CORPORATION

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