



STL10DN15F3

N-channel 150 V, 0.20 Ω typ., 2.8 A STripFET™ III Power MOSFET in a PowerFLAT™ 5x6 double island package

Datasheet — production data

Features

Order code	$V_{DS@T_{Jmax}}$	$R_{DS(on)max}$	I_D
STL10DN15F3	150 V	<0.22 Ω	2.8 A

- Improved die-to-footprint ratio
- Very low profile package (1 mm max)
- Very low thermal resistance
- Low on-resistance

Applications

- Switching applications

Description

This device is an N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

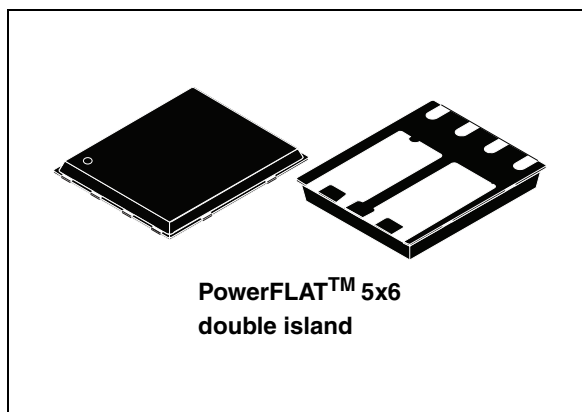


Figure 1. Internal schematic diagram

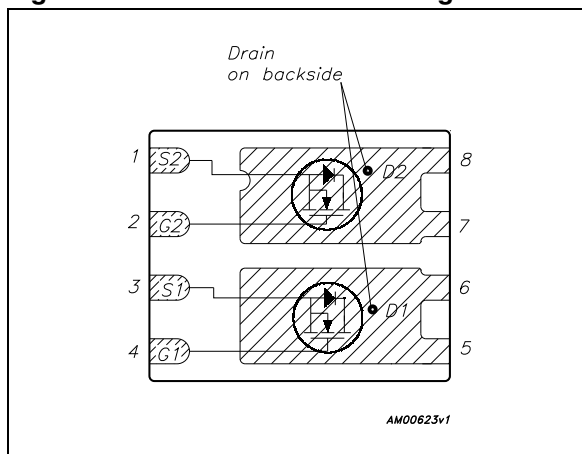


Table 1. Device summary

Order code	Marking	Package	Packaging
STL10DN15F3	10DN15F3	PowerFLAT™ 5x6 double island	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
5	Revision history	13

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	150	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	10	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	2.8	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6.25	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	1.8	A
$I_{DM}^{(3)}$	Drain current (pulsed)	11.2	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	50	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	3.5	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according R_{thj-c}
2. The value is rated according $R_{thj-pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current repetitive or not repetitive, (pulse width limited by $T_{j\text{Max}}$)	1.4	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$, $I_D=I_{AS}$, $V_{DD}=120\text{ V}$)	150	mJ

2 Electrical characteristics

($T_{CASE}=25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	150			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 150\text{ V}$, $V_{DS} = 150\text{ V}$, $T_c=125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 1.4\text{ A}$		0.20	0.22	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f=1\text{ MHz}$, $V_{GS}=0$		330		pF
C_{oss}	Output capacitance		-	60	-	pF
C_{rss}	Reverse transfer capacitance			15		pF
Q_g	Total gate charge	$V_{DD}=75\text{ V}$, $I_D = 2.8\text{ A}$		9.5		nC
Q_{gs}	Gate-source charge	$V_{GS}=10\text{ V}$	-	1.5	-	nC
Q_{gd}	Gate-drain charge	(see Figure 14)		4.3		nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=75\text{ V}$, $I_D = 1.4\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS}=10\text{ V}$ (see Figure 13)		5.5		ns
t_r	Rise time			2.4		ns
$t_{d(off)}$	Turn-off delay time		-	16.1	-	ns
t_f	Fall time			5.5		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		11.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=2.8\text{ A}$, $V_{GS}=0$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD}=2.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=120\text{ V}$, $T_j=150\text{ }^\circ\text{C}$	-	73.5		ns
Q_{rr}	Reverse recovery charge			210		nC
I_{RRM}	Reverse recovery current			5.7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

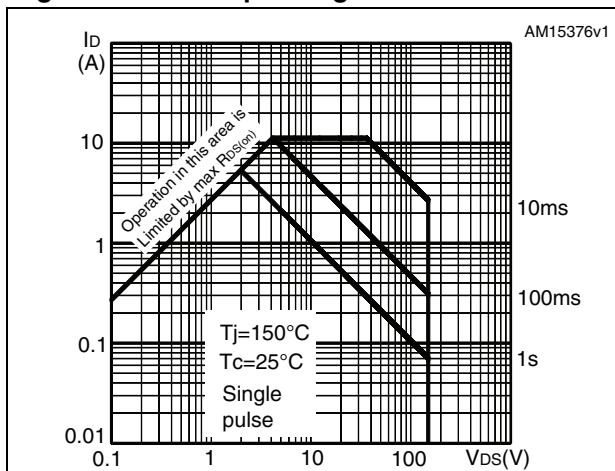


Figure 3. Thermal impedance

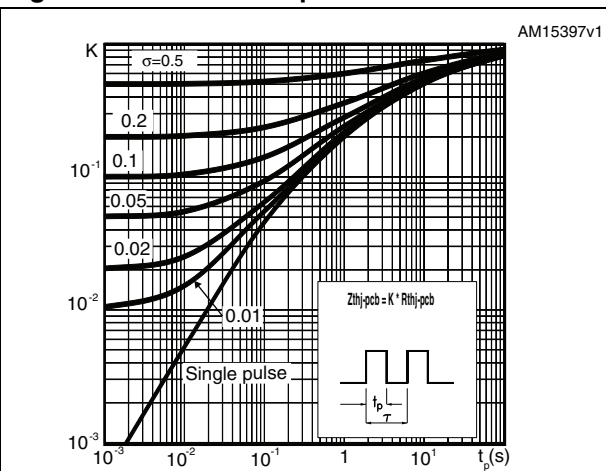


Figure 4. Output characteristics

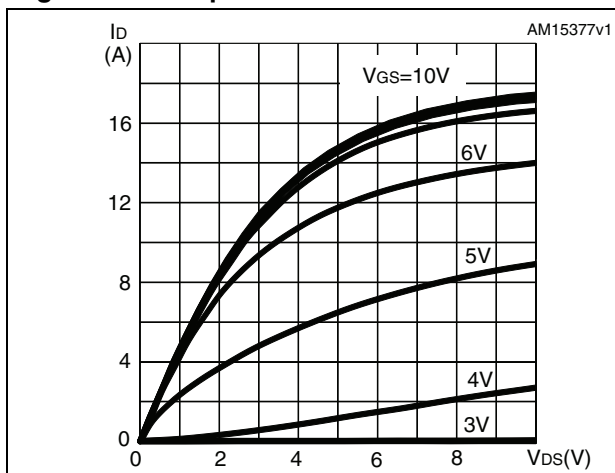


Figure 5. Transfer characteristics

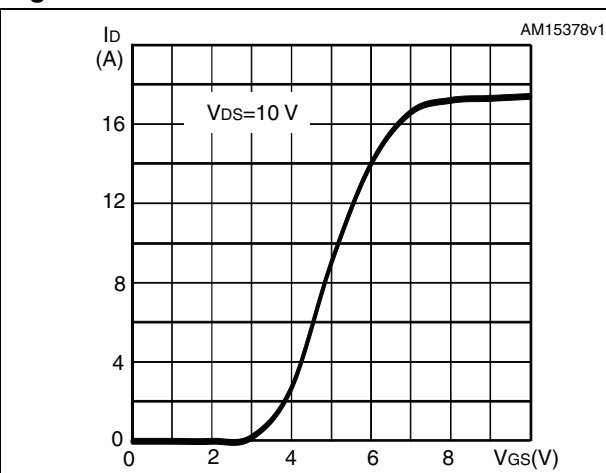


Figure 6. Gate charge vs gate-source voltage

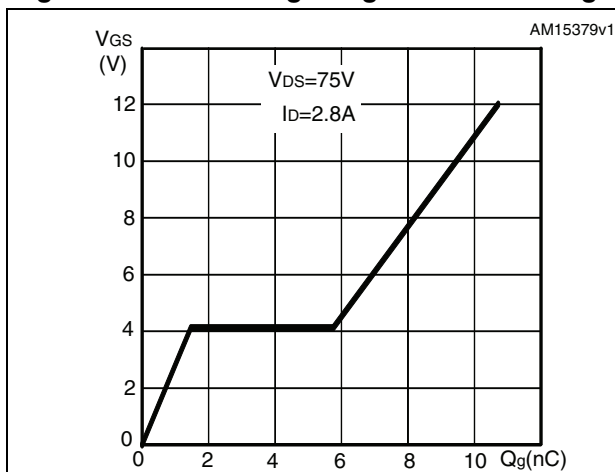


Figure 7. Static drain-source on-resistance

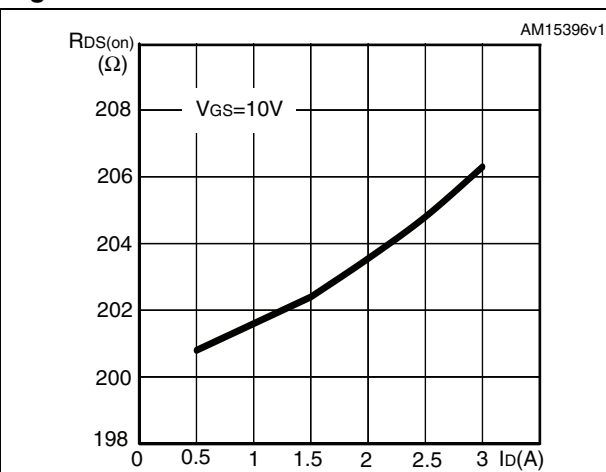


Figure 8. Capacitance variations

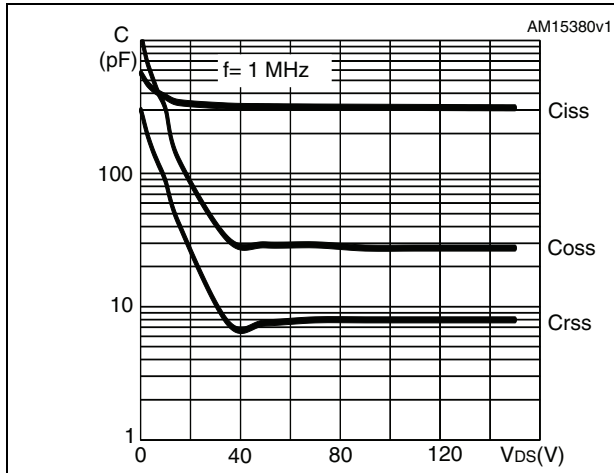


Figure 9. Normalized on-resistance vs temperature

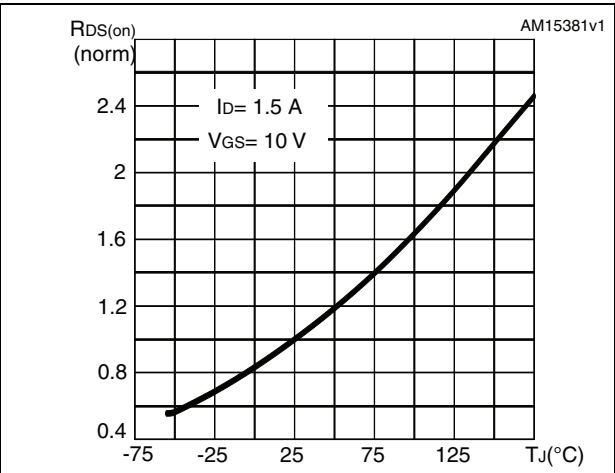


Figure 10. Normalized gate threshold voltage vs temperature

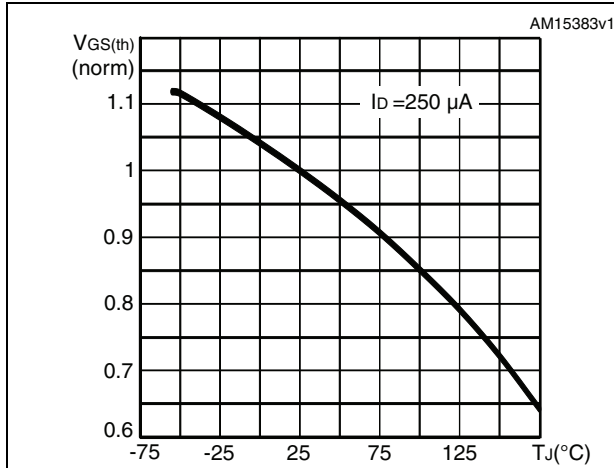


Figure 11. Normalized B_{VDSS} vs temperature

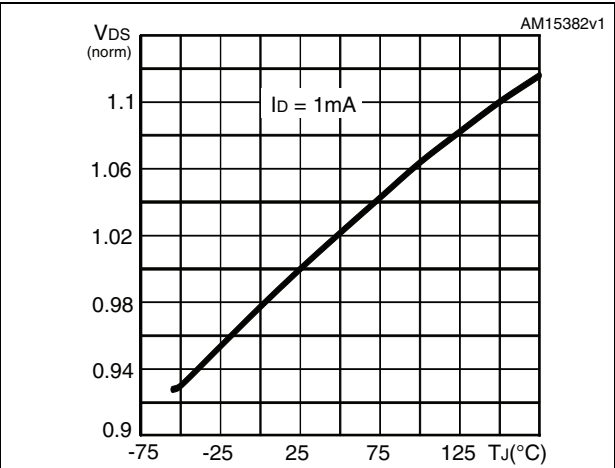
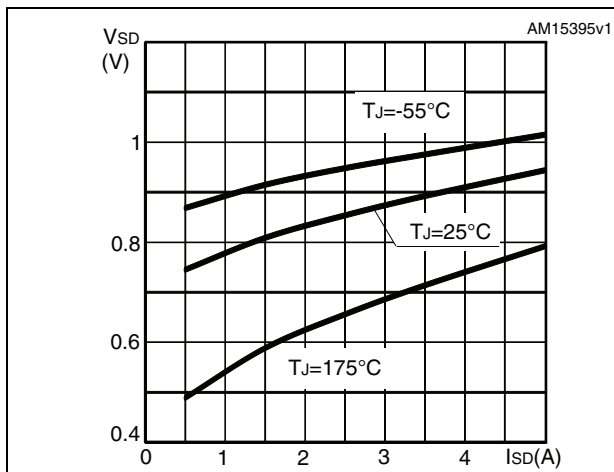


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

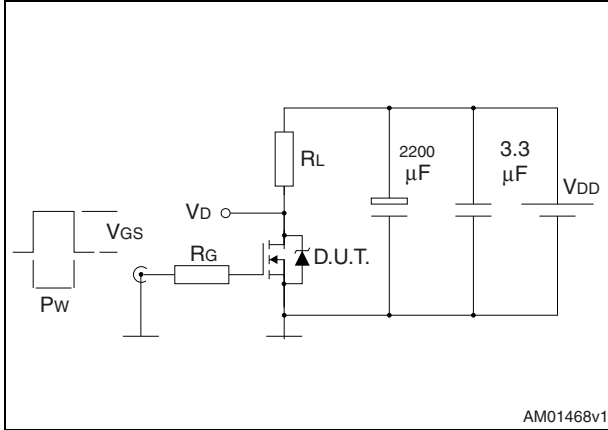


Figure 14. Gate charge test circuit

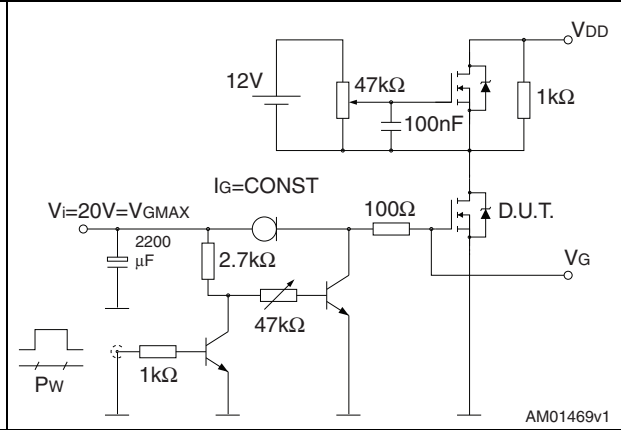


Figure 15. Test circuit for inductive load switching and diode recovery times

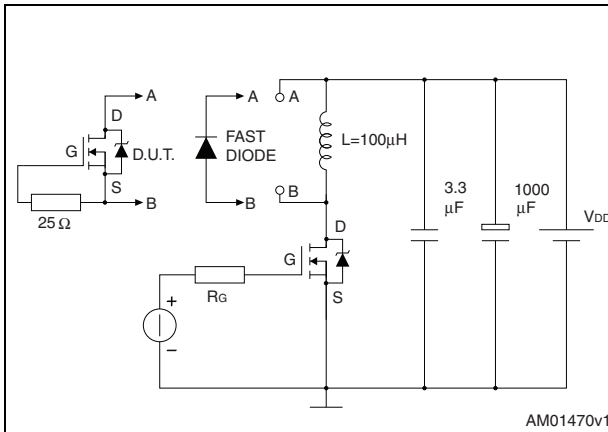


Figure 16. Unclamped inductive load test circuit

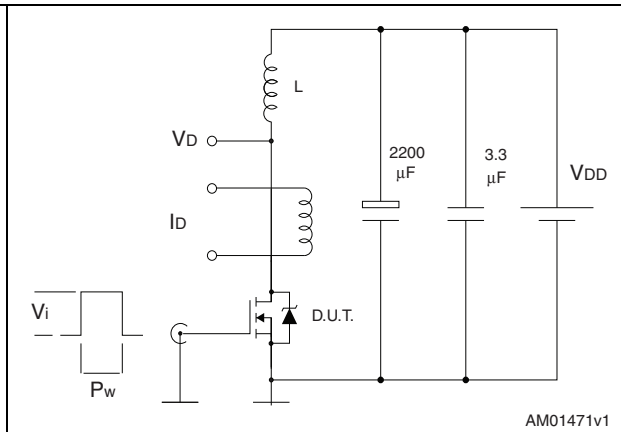


Figure 17. Unclamped inductive waveform

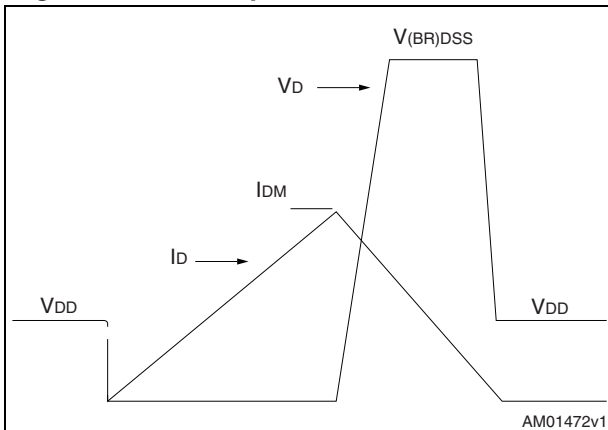
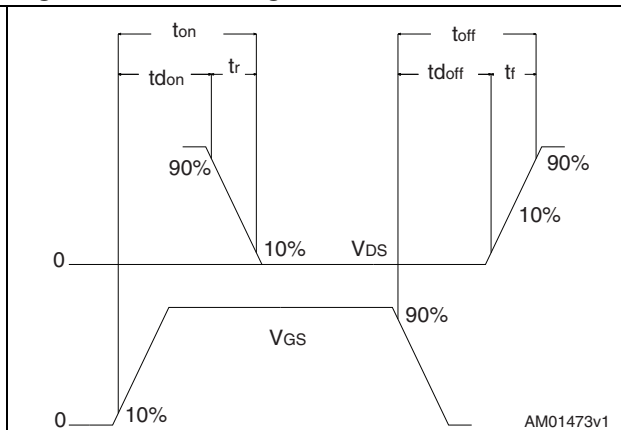


Figure 18. Switching time waveform



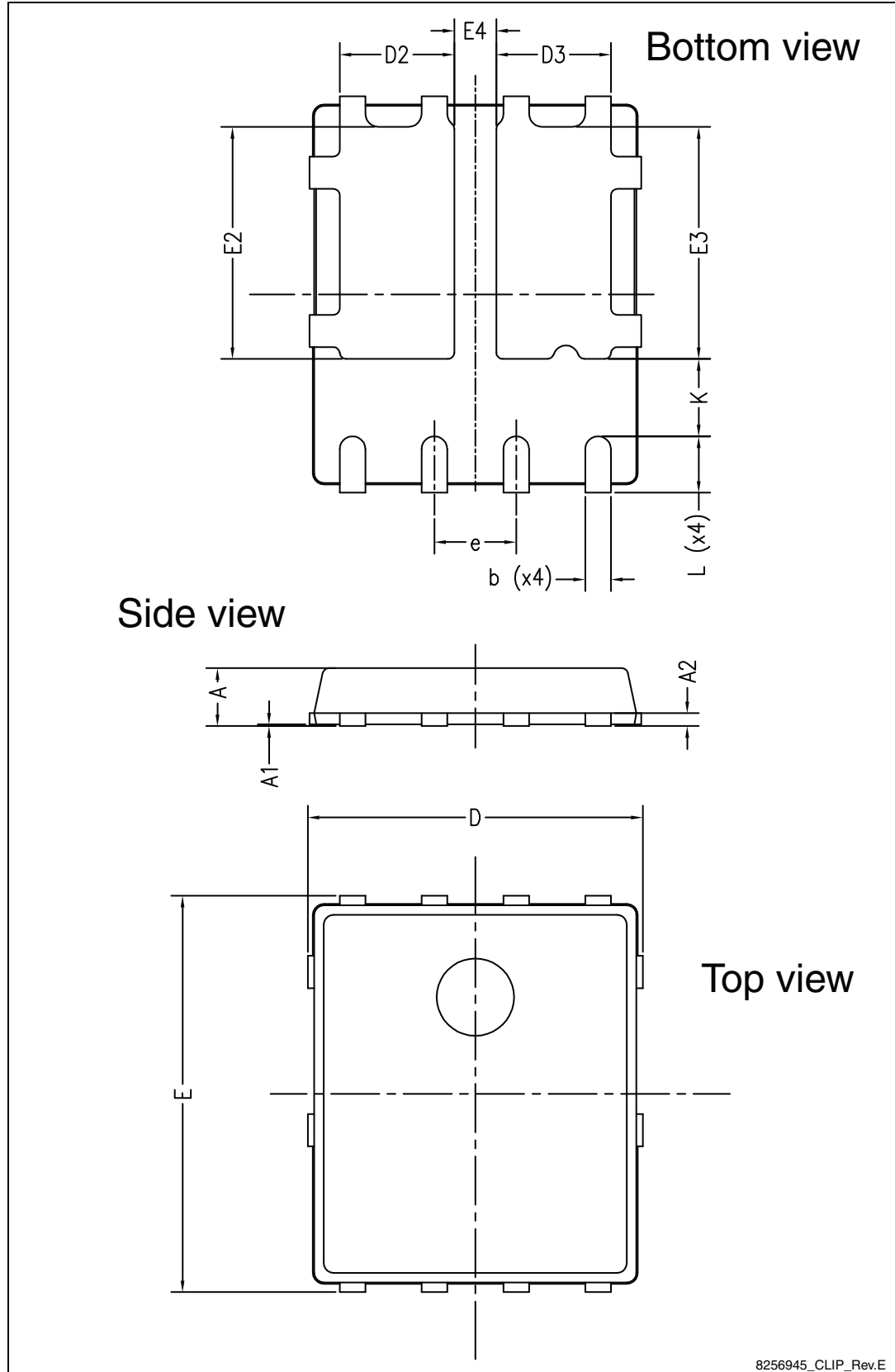
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. PowerFLAT™ 5x6 - 8 leads dual pad (ribbon) mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.725		1.025
K	1.05		1.35

Figure 19. PowerFLAT™ 5x6 - 8 leads dual pad drawing (dimensions are in mm)



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
27-Sep-2012	1	First release.
15-Oct-2012	2	<ul style="list-style-type: none">– $R_{thj-case}$ has been updated in table 3– Updated Section 4: Package mechanical data.– Minor text changes on cover page

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