

CS8363

3.3 V Dual Micropower Regulator with ENABLE and RESET

The CS8363 is a precision Micropower dual voltage regulator with ENABLE and RESET.

The 3.3 V standby output is accurate within $-2%$, $+2.4%$ while supplying loads of 100 mA. Quiescent current is low, typically 140 μ A with a 300 μ A load. The active RESET output monitors the 3.3 V standby output and is low during power-up and regulator dropout conditions. The RESET circuit includes hysteresis and is guaranteed to operate correctly with 1.0 V on the standby output.

The second output tracks the 3.3 V standby output through an external adjust lead, and can supply loads of 250 mA. The logic level lead ENABLE is used to control this tracking regulator output.

Both outputs are protected against overvoltage, short circuit, reverse battery and overtemperature conditions. The robustness and low quiescent current of the CS8363 makes it not only well suited for automotive microprocessor applications, but for any battery powered microprocessor applications.

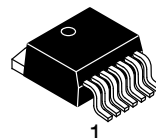
Features

- 2 Regulated Outputs
 - Standby Output 3.3 V $-2%$, $+2.4%$; 100 mA
 - Adjustable Tracking Output; 250 mA
- Operation down to $V_{IN} = 4.5$ V
- RESET for V_{STBY}
- ENABLE for V_{TRK}
- Low Quiescent Current
- Protection Features
 - Independent Thermal Shutdown
 - Short Circuit
 - 60 V Load Dump
 - Reverse Battery



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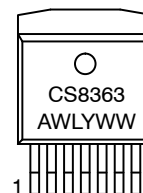
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D²PAK-7
DPS SUFFIX
CASE 936AB

Pin 1. V_{STBY}
2. V_{IN}
3. V_{TRK}
4. GND
5. Adj
6. ENABLE
7. RESET

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION*

Device	Package	Shipping†
CS8363YDPS7	D ² PAK-7	50 Units/Rail
CS8363YDPSR7	D ² PAK-7	750 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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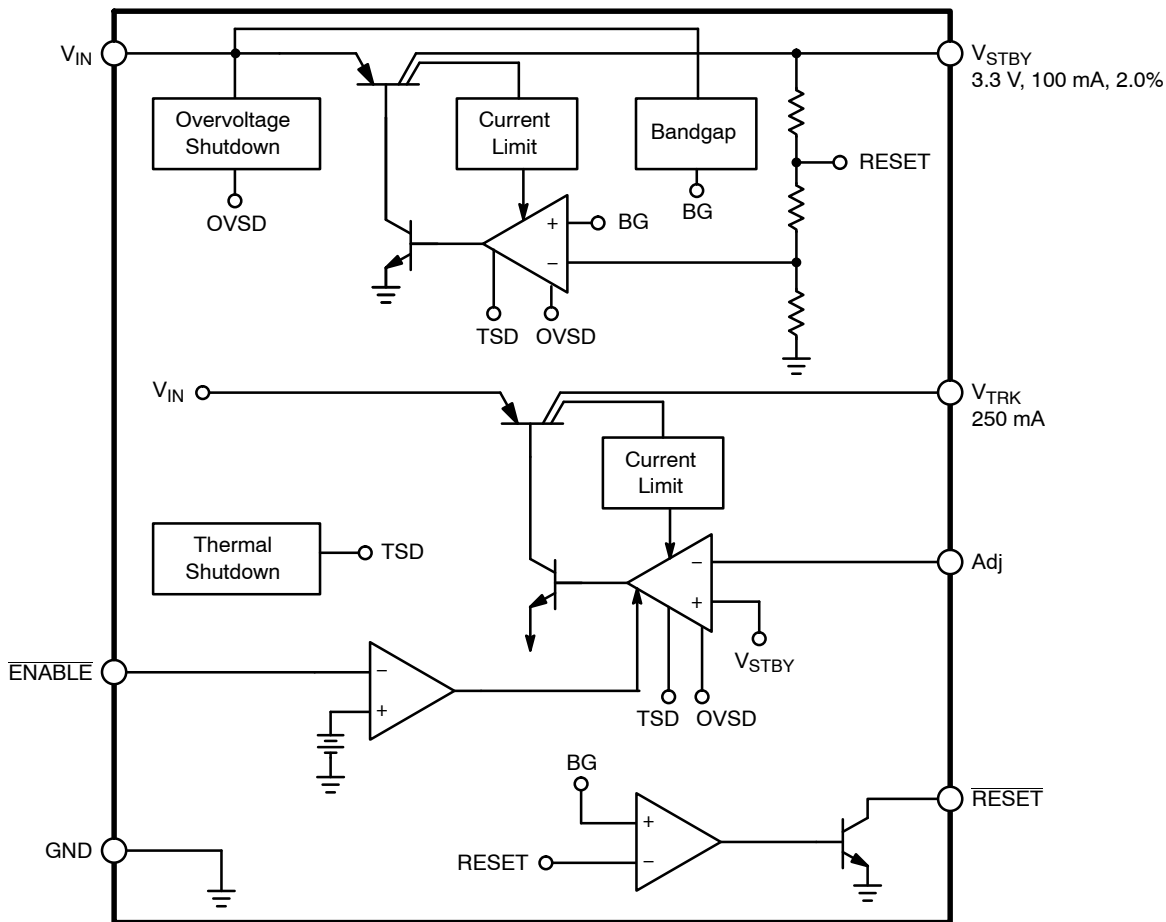


Figure 1. Block Diagram. Consult Your Local Sales Representative for Positive ENABLE Option

ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit	
Supply Voltage, V_{IN}	-16 to 26	V	
Positive Transient Input Voltage, $t_r > 1.0$ ms	60	V	
Negative Transient Input Voltage, $T < 100$ ms, 1.0 % Duty Cycle	-50	V	
Input Voltage Range (ENABLE, RESET)	-0.3 to 10	V	
Junction Temperature	-40 to +150	°C	
Storage Temperature Range	-55 to +150	°C	
ESD Susceptibility (Human Body Model)	2.0	kV	
Lead Temperature Soldering	Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2	260 peak 230 peak	°C °C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 10 seconds max.
2. 60 seconds max above 183°C

*The maximum package power dissipation must be observed.

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ELECTRICAL CHARACTERISTICS ($6.0\text{ V} \leq V_{IN} \leq 26\text{ V}$, $I_{OUT1} = I_{OUT2} = 100\ \mu\text{A}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$;
unless otherwise stated.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Tracking Output (V_{TRK})					
V_{TRK} Tracking Error ($V_{STBY} - V_{TRK}$)	$6.0\text{ V} \leq V_{IN} \leq 26\text{ V}$, $100\ \mu\text{A} \leq I_{TRK} \leq 250\text{ mA}$. Note 3	-25	-	+25	mV
Adjust Pin Current, I_{Adj}	Loop in Regulation	-	1.5	5.0	μA
Line Regulation	$6.0\text{ V} \leq V_{IN} \leq 26\text{ V}$. Note 3	-	5.0	50	mV
Load Regulation	$100\ \mu\text{A} \leq I_{TRK} \leq 250\text{ mA}$. Note 3	-	5.0	50	mV
Dropout Voltage ($V_{IN} - V_{TRK}$)	$I_{TRK} = 100\ \mu\text{A}$. $I_{TRK} = 250\text{ mA}$	-	-	1.05	mV
		-	-	1.05	mV
Current Limit	$V_{IN} = 12\text{ V}$, $V_{TRK} = 3.0\text{ V}$	275	500	-	mA
Quiescent Current	$V_{IN} = 12\text{ V}$, $I_{TRK} = 250\text{ mA}$, No Load on V_{STBY} $V_{IN} = 12\text{ V}$, $I_{TRK} = 500\ \mu\text{A}$, $I_{STBY} = 100\ \mu\text{A}$	-	25	50	mA
		-	145	220	μA
Reverse Current	$V_{TRK} = 3.3\text{ V}$, $V_{IN} = 0\text{ V}$	-	200	1500	μA
Ripple Rejection	$f = 120\text{ Hz}$, $I_{TRK} = 250\text{ mA}$, $7.0\text{ V} \leq V_{IN} \leq 17\text{ V}$	60	70	-	dB

Standby Output (V_{STBY})

Output Voltage, V_{STBY}	$4.5\text{ V} \leq V_{IN} \leq 26\text{ V}$, $100\ \mu\text{A} \leq I_{STBY} \leq 100\text{ mA}$.	3.234	3.3	3.380	V
Line Regulation	$6.0\text{ V} \leq V_{IN} \leq 26\text{ V}$.	-	5.0	50	mV
Load Regulation	$100\ \mu\text{A} \leq I_{STBY} \leq 100\text{ mA}$.	-	5.0	50	mV
Dropout Voltage ($V_{IN} - V_{STBY}$)	$I_{STBY} = 100\ \mu\text{A}$, $V_{IN} = 4.2\text{ V}$ $I_{STBY} = 100\text{ mA}$, $V_{IN} = 4.2\text{ V}$	-	-	1.05	V
		-	-	1.05	V
Current Limit	$V_{IN} = 12\text{ V}$, $V_{STBY} = 3.0\text{ V}$	125	200	-	mA
Short Circuit Current	$V_{IN} = 12\text{ V}$, $V_{STBY} = 0\text{ V}$	10	100	-	mA
Quiescent Current	$V_{IN} = 12\text{ V}$, $I_{STBY} = 100\text{ mA}$, $I_{TRK} = 0\text{ mA}$ $V_{IN} = 12\text{ V}$, $I_{STBY} = 300\ \mu\text{A}$, $I_{TRK} = 0\text{ mA}$	-	10	20	mA
		-	140	200	μA
Reverse Current	$V_{STBY} = 3.3\text{ V}$, $V_{IN} = 0\text{ V}$	-	100	200	μA
Ripple Rejection	$f = 120\text{ Hz}$, $I_{STBY} = 100\text{ mA}$, $7.0\text{ V} \leq V_{IN} \leq 17\text{ V}$	60	70	-	dB

RESET ENABLE Functions

ENABLE Input Threshold	-	0.8	1.2	2.0	V
ENABLE Input Bias Current	$V_{ENABLE} = 0\text{ V to }10\text{ V}$	-10	0	10	μA
RESET Hysteresis	-	10	50	150	mV
RESET Threshold Low (V_{RL})	V_{STBY} Decreasing, $V_{IN} > 4.5\text{ V}$	92.5	95	97.5	% V_{STBY}
RESET Leakage	-	-	-	25	μA
Output Voltage, Low (V_{RLO})	$1.0\text{ V} \leq V_{STBY} \leq V_{RL}$, $R_{RST} = 10\text{ k}\Omega$	-	0.1	0.4	V
Output Voltage, Low (V_{RPEAK})	V_{STBY} , Power Up, Power Down	-	0.6	1.0	V
V_{IN} (V_{RST} Low)	$V_{STBY} = 3.3\text{ V}$	-	4.0	4.5	V

Protection Circuitry (Both Outputs)

Independent Thermal Shutdown	V_{STBY} V_{TRK}	150	180	-	$^\circ\text{C}$
		150	165	-	$^\circ\text{C}$
Overshoot Shutdown	-	30	34	38	V

3. V_{TRK} connected to Adj lead. V_{TRK} can be set to higher values by using an external resistor divider.

PACKAGE PIN DESCRIPTION

PACKAGE PIN #	PIN SYMBOL	FUNCTION
D ² PAK-7		
1	V _{STBY}	Standby output voltage delivering 100 mA.
2	V _{IN}	Input voltage.
3	V _{TRK}	Tracking output voltage controlled by ENABLE delivering 250 mA.
4	GND	Reference ground connection.
5	Adj	Resistor divider from V _{TRK} to Adj. Sets the output voltage on V _{TRK} . If tied to V _{TRK} , V _{TRK} will track V _{STBY} .
6	ENABLE	Provides on/off control of the tracking output, active LOW.
7	RESET	CMOS compatible output lead that goes low whenever V _{STBY} falls out of regulation.

CIRCUIT DESCRIPTION

ENABLE Function

The ENABLE function switches the output transistor for V_{TRK} on and off. When the ENABLE lead voltage exceeds 1.4 V (Typ), V_{TRK} turns off. This input has several hundred millivolts of hysteresis to prevent spurious output activity during power-up or power-down.

RESET Function

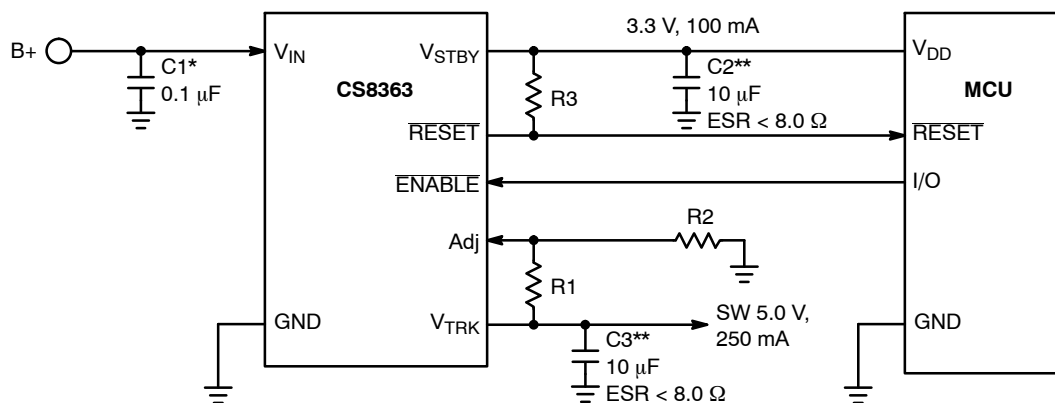
The RESET is an open collector NPN transistor, controlled by a low voltage detection circuit sensing the V_{STBY} (3.3 V) output voltage. This circuit guarantees the RESET output stays below 1.0 V (0.1 V Typ) when V_{STBY} is as low as 1.0 V to ensure reliable operation of microprocessor-based systems.

V_{TRK} Output Voltage

This output uses the same type of output device as V_{STBY}, but is rated for 250 mA. The output is configured as a tracking regulator of the standby output. By using the standby output as a voltage reference, giving the user an external programming lead (Adj lead), output voltages from 3.3 V to 20 V are easily realized. The programming is done with a simple resistor divider, and following the formula:

$$V_{TRK} = V_{STBY} \times (1 + R1/R2) + I_{Adj} \times R1$$

If another 3.3 V output is needed, simply connect the Adj lead to the V_{TRK} output lead.



$$V_{TRK} \sim V_{STBY}(1 + R1/R2)$$

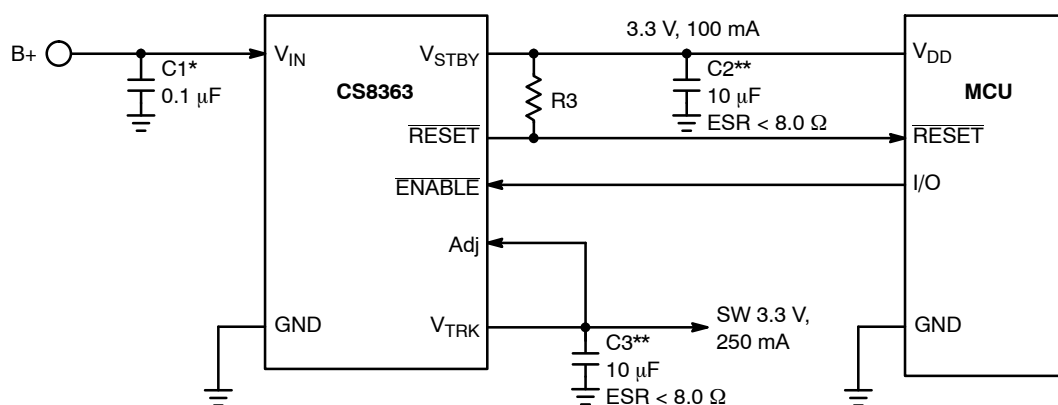
For V_{TRK} ~ 5.0 V, R1/R2 ~ 0.5

*C1 is required if regulator is located far from power supply filter.

**C2 and C3 are required for stability.

Figure 2. Test and Application Circuit, 3.3 V, 5.0 V Regulator

CS8363



*C1 is required if regulator is located far from power supply filter.

**C2 and C3 are required for stability.

Figure 3. Test and Application Circuit, Dual 3.3 V Regulator

APPLICATION NOTES

External Capacitors

Output capacitors for the CS8363 are required for stability. Without them, the regulator outputs will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst-case is determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to -40°C , capacitors rated at that temperature must be used.

More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, "Compensation for Linear Regulators," document number SR003AN/D, available through the Literature Distribution Center or via our website at <http://www.onsemi.com>.

Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 4) is

$$P_{D(\max)} = [V_{IN(\max)} - V_{OUT1(\min)}]I_{OUT1(\max)} + [V_{IN(\max)} - V_{OUT2(\min)}]I_{OUT2(\max)} + V_{IN(\max)}I_Q \quad (1)$$

where:

$V_{IN(\max)}$ is the maximum input voltage,

$V_{OUT1(\min)}$ is the minimum output voltage from V_{OUT1} ,

$V_{OUT2(\min)}$ is the minimum output voltage from V_{OUT2} ,

$I_{OUT1(\max)}$ is the maximum output current, for the application,

$I_{OUT2(\max)}$ is the maximum output current, for the application, and

I_Q is the quiescent current the regulator consumes at both $I_{OUT1(\max)}$ and $I_{OUT2(\max)}$.

Once the value of $P_{D(\max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^{\circ}\text{C} - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C .

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

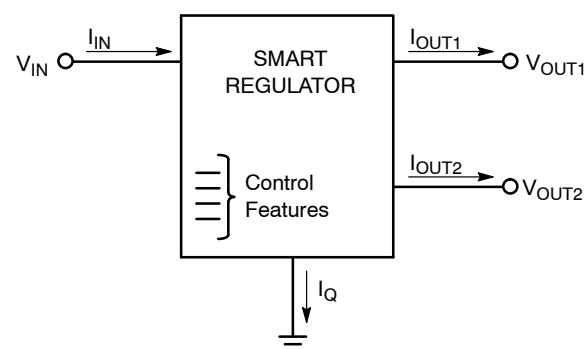


Figure 4. Dual Output Regulator With Key Performance Parameters Labeled.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

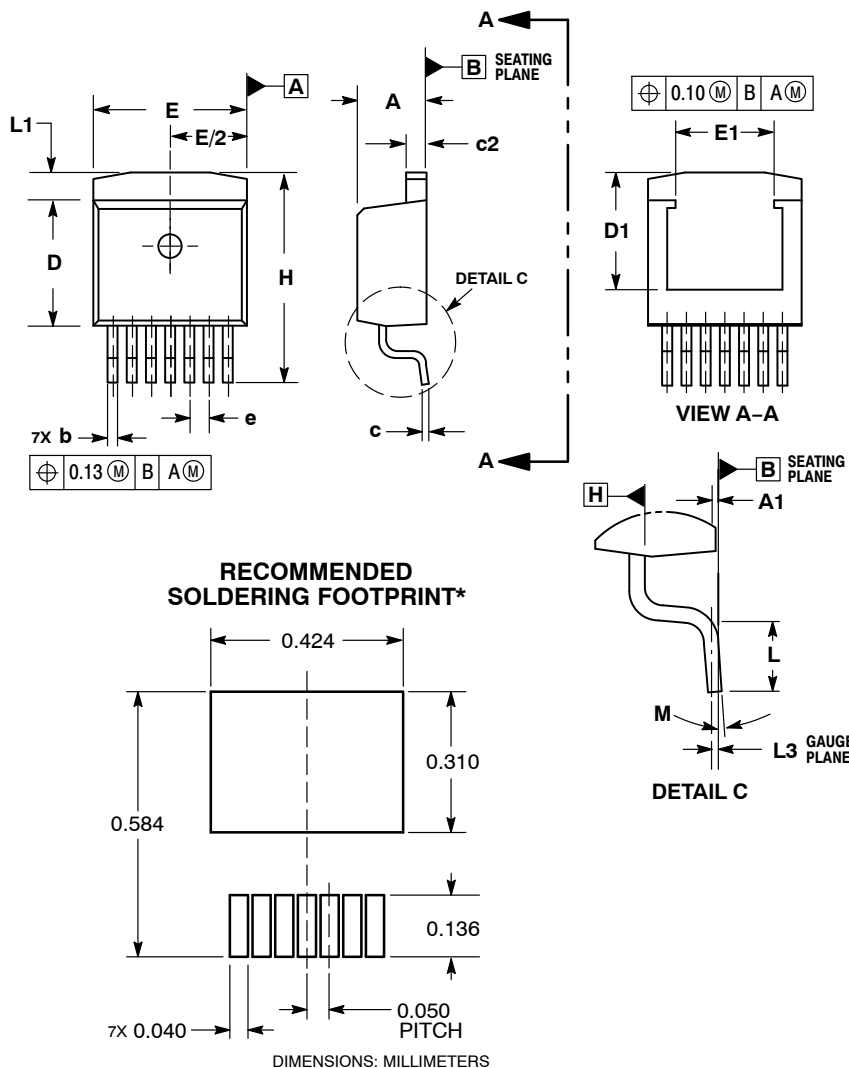
where:

$R_{\theta JC}$ = the junction-to-case thermal resistance,
 $R_{\theta CS}$ = the case-to-heatsink thermal resistance, and
 $R_{\theta SA}$ = the heatsink-to-ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

PACKAGE DIMENSIONS

D²PAK-7 (SHORT LEAD)
DPS SUFFIX
CASE 936AB-01
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.005 MAXIMUM PER SIDE. THESE DIMENSIONS TO BE MEASURED AT DATUM H.
 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1. DIMENSIONS D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THE THERMAL PAD.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.170	0.180	4.32	4.57
A1	0.000	0.010	0.00	0.25
b	0.026	0.036	0.66	0.91
c	0.017	0.026	0.43	0.66
c2	0.045	0.055	1.14	1.40
D	0.325	0.368	8.25	9.53
D1	0.270	---	6.86	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.050 BSC		1.27 BSC	
H	0.539	0.579	13.69	14.71
L	0.058	0.078	1.47	1.98
L1	---	0.066	---	1.68
L3	0.010 BSC		0.25 BSC	
M	0°		8°	


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE THERMAL DATA

Parameter		D ² PAK-7	Unit
R _{θJC}	Typical	3.5	°C/W
R _{θJA}	Typical	10-50*	°C/W

*Depending on thermal properties of substrate. R_{θJA} = R_{θJC} + R_{θCA}.

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