AZPB70

Programmer Board Kit for AZT70/71

www.azmicrotek.com

DESCRIPTION

The AZPB70 programmer board kit is a PC based assembly that enables prototyping and bench testing of the AZT70 and AZT71 Programmable Capacitive Tuning ICs. It may also be used in production to simplify tuning. The AZT70/71 is a digitally programmed capacitor specifically designed to tune a crystal or SAW based oscillator to a desired center frequency. The desired capacitance value for production trimming is set by a serial data stream when placed into a programming mode. They are designed to be a labor and cost saving devices within the oscillator production process.

Using EEPROM technology, the capacitance can be re-tuned as needed during the production process by repeating the programming steps thereby increasing production yield.

FEATURES

- Programmer board kit for AZT70 and AZT71 capacitive tuning ICs
- Reprogrammable through nonvolatile EEPROM storage
- Software to be used with Windows XP SP2, Windows Vista, & Windows 7 operating systems

APPLICATIONS

- Fast production tuning of crystal or SAW oscillators
- Filters requiring capacitive tuning

PACKAGE OPTIONS

- SON8 (1.5mm x 1.0mm)
- TSOT6
  - AZT71 only
- MLP6 (2.0mm x 2.0mm)
  - AZT71 only

INCLUDED HARDWARE

Table 1 – AZPB70 included hardware

Item	Qty	Description	Comments
1	1	AZPB70 Programmer Board	
2	1	Programming Socket Adapter Board (SON8)	TSOT6 & MLP6 adapter boards are optionally available for AZT71
3	1	6 Pin Ribbon Cable	Connects programmer board to socket adapter board
4	1	10' USB Cable (A-B)	Connects programmer board to PC
5	1	USB Drive (AZM Logo)	Contains driver program and PC software

Part Number (PN)	Package	Notes
AZPB70Q	SON8	
AZPB70H	TSOT6	AZT71 only
AZPB70M	MLP6	AZT71 only

HARDWARE OVERVIEW

The AZPB70 programmer board comes with all the hardware listed in Table 1. These hardware parts are necessary to complete the setup shown in Figure 1 which is used to evaluate the AZT70 and AZT71 capacitive tuning ICs. For production programming and measurement, the AZT70/71 should be soldered onto the oscillator PCB board where the 3 programming pins are accessible through the PCB substrate (Figure 2). Figure 3 and Figure 4 detail the top & bottom views of the programmer board, respectively.

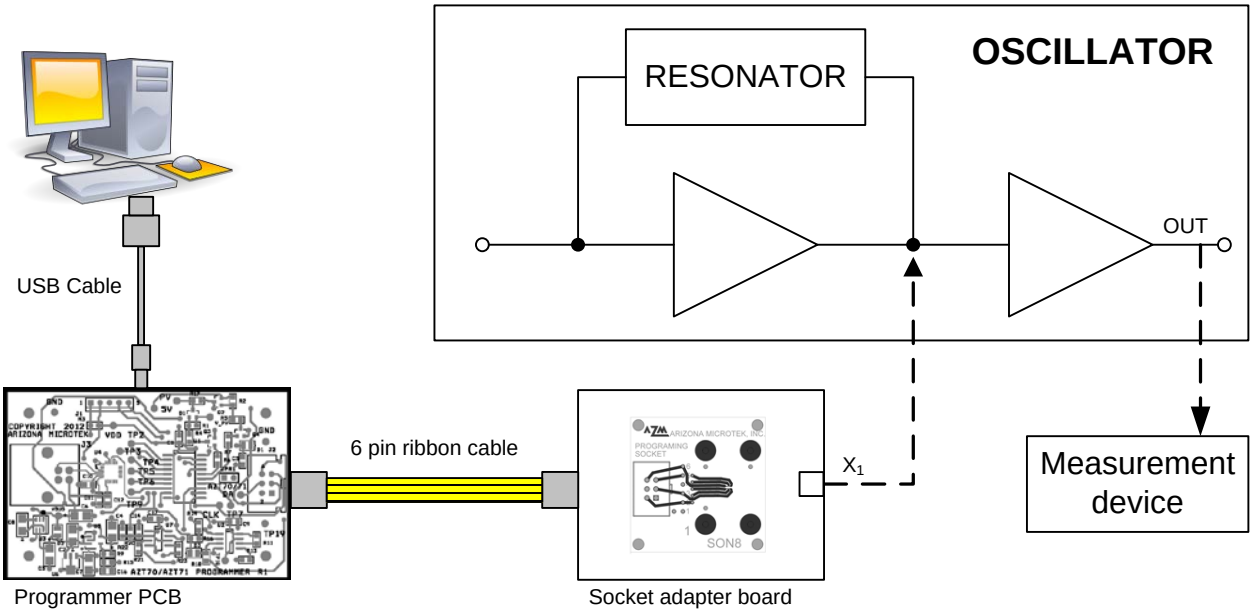

Figure 1 – AZPB70 Hardware setup for evaluation

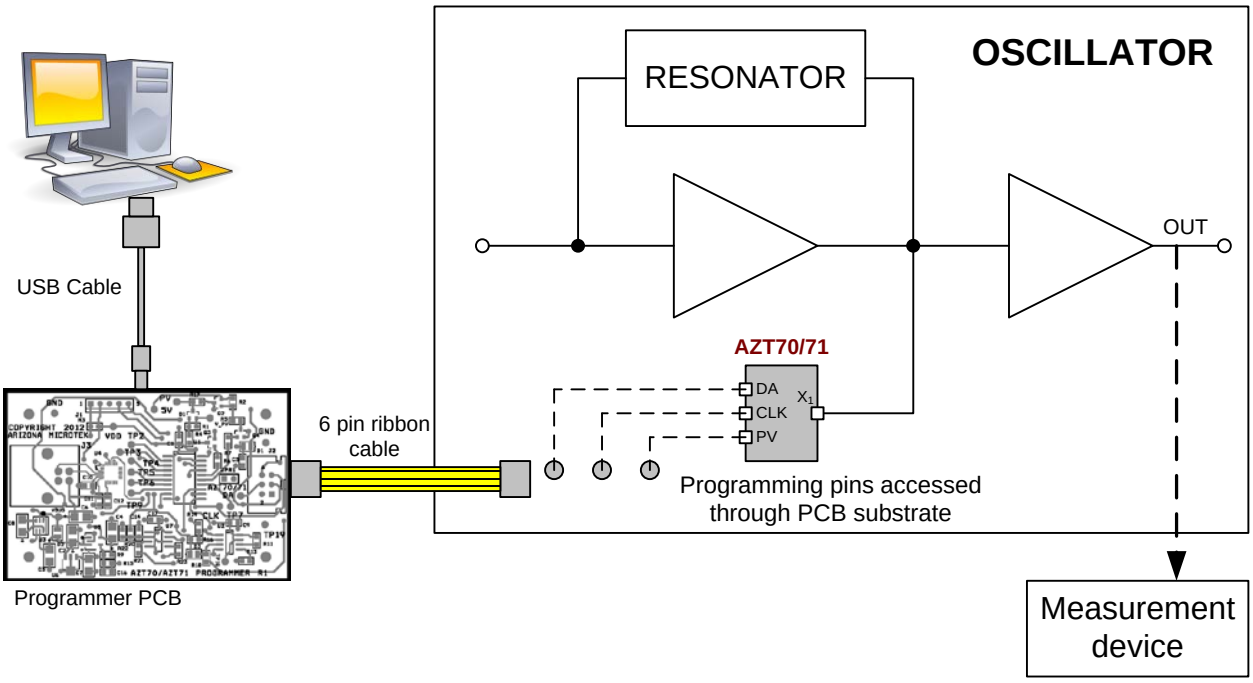

Figure 2 – AZPB70 hardware setup for production

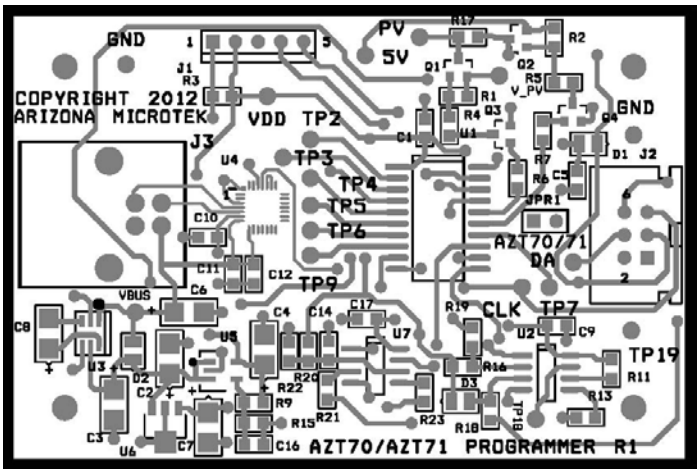

Figure 3 - Programmer PCB Top View

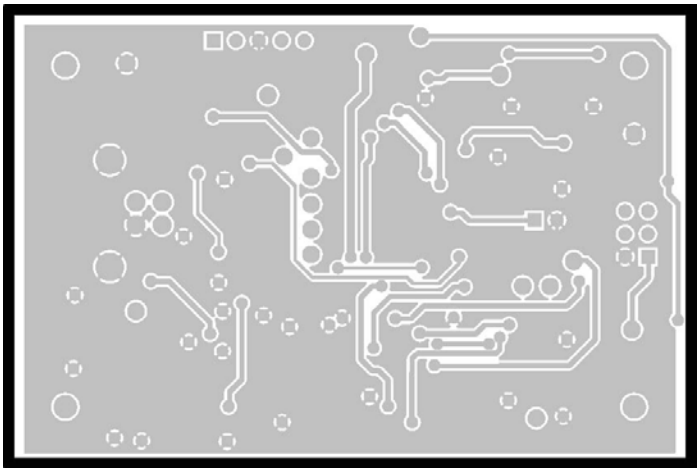

Figure 4 - Programmer PCB Bottom View

The Programmer Board connects to the Programming Socket Adapter Board through a 6-pin ribbon cable. Table 2 details the pin connections between the 2 boards with respect to the packages available for the AZT70/71. Figure 5, Figure 6, and Figure 7 shows the Programming Socket Adapter Boards for the Q package, H package, and M package, respectively.

Table 2 – Programmer Board to Programming Socket Adapter Board Pin Interconnect

	Programmer Board	Programming Socket Adapter Board		
Signal Name	**Ribbon Cable Pin**	**AZT70/71 SON8 Package Pin**	**AZT71 MLP6 Package Pin**	**AZT71 TSOT6 Package Pin**
X_1	1	1	1	1
V_{SS}	2	3	2	2
V_{DD}	3	4	3	6
DA	4	5	4	5
CLK	5	6	5	4
PV	6	8	6	3

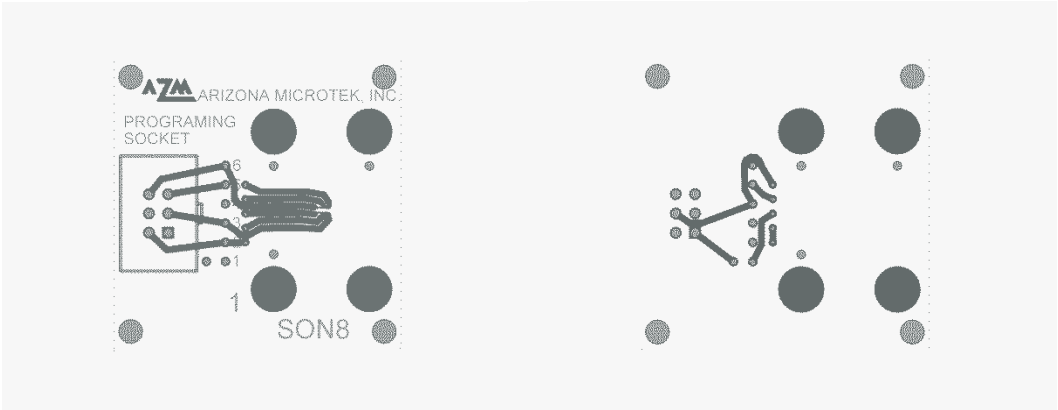

Figure 5 - Q-SON8 Programming Socket Adapter Board (Top & Bottom View)

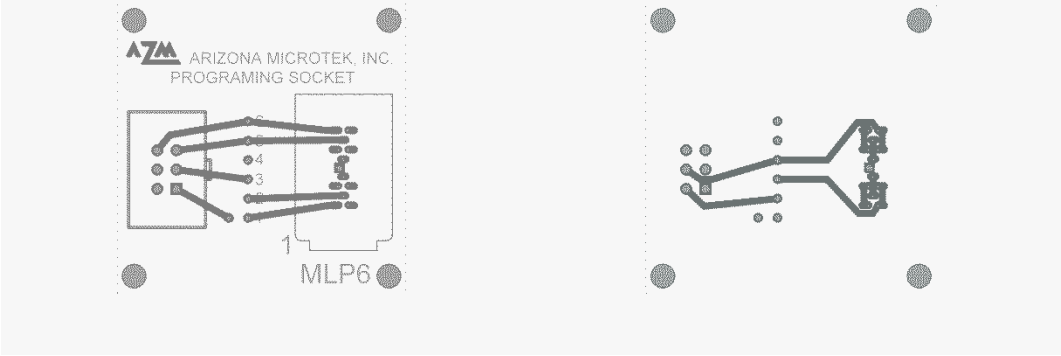

Figure 6 - MLP6 Programming Socket Adapter Board (Top & Bottom View)

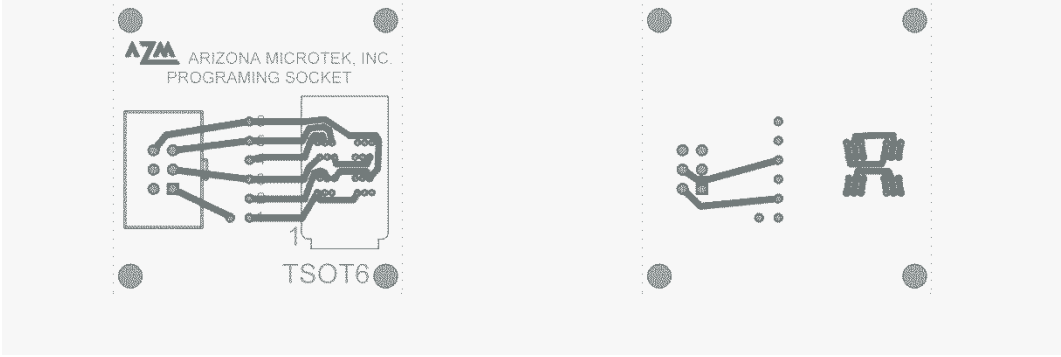

Figure 7 - TSOT6 Programming Socket Adapter Board (Top & Bottom View)

SOFTWARE OVERVIEW

The AZPB70 software operates under Windows XP SP2+, Windows Vista and Windows 7 operating systems. The software package includes a USB driver and a PC based interface program.

DRIVER INSTALLATION

Install the USB software driver before plugging the programmer board into the USB port. *Note – User must have administrator rights to computer. Plug the USB flash drive into an unused USB port on the computer. Run the program entitled "/Software/CP210x_VCP_Win_XP_S2K3_Vista_7.exe" from the USB flash drive and follow the on-screen instructions. After driver installation, plug the programmer board into a USB port on the computer.

PROGRAM INSTALLATION

Copy the file "/Software/AZT70_71Programmer.exe" from the USB flash drive into the desired directory on the computer hard disk.

AZT70/71 MODE SELECTION

Jumper JPR1 on the programming board selects the AZT70 or AZT71 mode. It is located next to the 6-pin ribbon cable connector (Figure 8). The programmer board enters the AZT71 mode without the jumper. The programmer board enters the AZT70 mode when the jumper is installed.

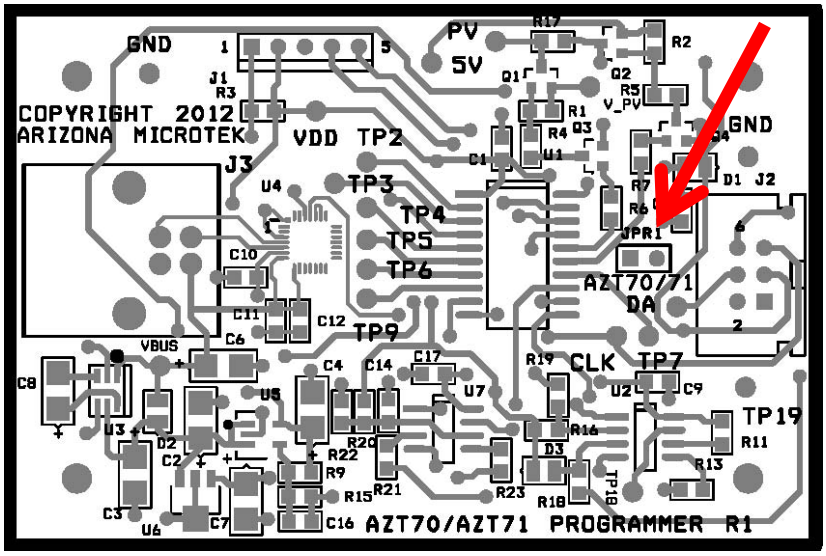

Figure 8 – Programmer board jumper location

PROGRAM OPERATION

Make sure the USB cable is connected to the PC and the programmer board. Start the program by double clicking on the "AZT70_71Programmer.exe" icon. The computer then shows the following window.

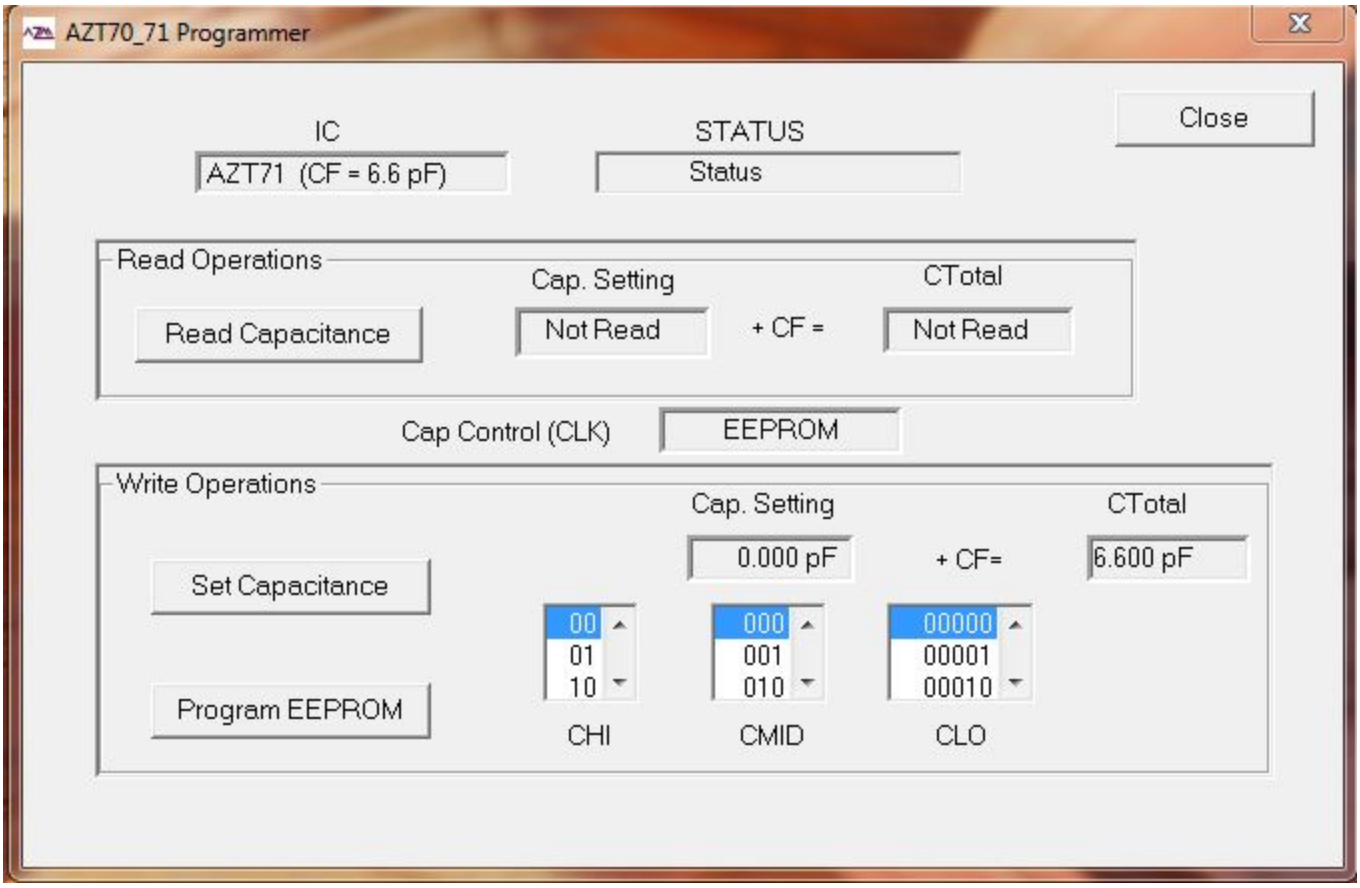

Figure 9 – Program window

The programmer window contains four sections: IC/Status, Read Operations, Cap Control and Write Operations.

IC/STATUS

The 'IC' field shows the chip type selected by jumper on the programming board, either the AZT70 or AZT71. The 'STATUS' field gives the results of the most recent programmer operation.

READ OPERATIONS

Pressing the 'Read Capacitance' button starts a read sequence of each EEPROM bit. The 'Cap. Setting' field shows the equivalent capacitance based on the bit states. The 'CTotal' field adds the fixed capacitance to give the total capacitance seen at the X_1 pin.

CAP CONTROL (CLK)

The logic level of the CLK input controls the source of the capacitance set commands. If the CLK pin is high, the capacitance value follows the register contents selected through the 'Set Capacitance' button. If the CLK pin is low, the capacitance value follows the non-volatile EEPROM contents set through the 'Program EEPROM' button. The 'Cap Control (CLK)' field shows the state of the CLK input, either 'Register' or 'EEPROM.'

WRITE OPERATIONS

Pressing the 'Set Capacitance' button places the contents of the 'C_{hi}', 'C_{mid}', and 'C_{lo}' binary bit fields into the internal AZT70/71 registers. The 'C_{hi}' bit field has no effect for the AZT70 since only the AZT71 contains the C_{hi} selectable capacitor.

Pressing the 'Program EEPROM' button erases the part, and then programs the EEPROM with the contents of C_{hi} (AZT71 only), C_{mid}, and C_{lo}.

PROGRAMMING THE AZT70/71

Programming the AZT70/71 is a simple procedure using the included software and programmer board. The following sections describe the internal functions of the software and programmer board in detail.

CONTROL WORD

The capacitance in the AZT70/71 is controlled by an 11-bit shift register with the data input bit definitions shown in Table 3 and Table 4. The control word data is inputted serially on the rising edge of the CLK signal with bit0 first and bit10 last.

Table 3 - AZT70 Control Word Definition

11-bit Control Word										
bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Not Used	Not Used	C_{mid}			C_{lo}					Not Used
		MSB	---	LSB	MSB	---	---	---	LSB	

Table 4 - AZT71 Control Word Definition

11-bit Control Word										
bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
C_{hi}		C_{mid}			C_{lo}					Not Used
MSB	LSB	MSB	---	LSB	MSB	---	---	---	LSB	

The control word mapping is binary weighted for each of C_{hi}, C_{mid} and C_{lo} where higher number bits are more significant. Figure 10 shows the capacitance value mapping for the AZT70. The detailed Nominal Capacitance Binary Mapping for both the AZT70 and AZT71 can be located on the AZM website.

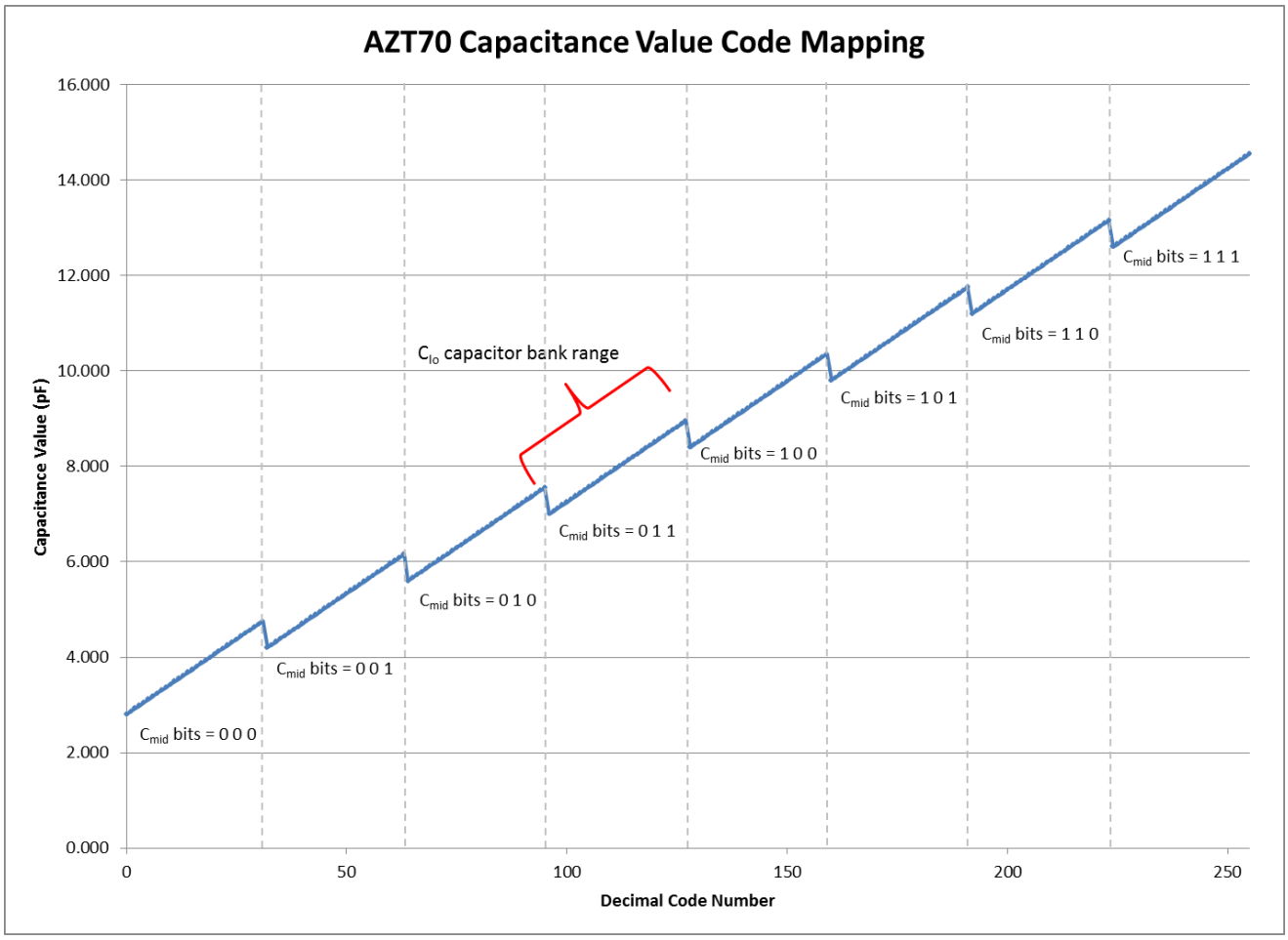

Figure 10 - AZT70 Capacitance Value Mapping

AZT70/71 FUNCTIONAL MODES

The AZT70/71 is designed to be used in 2 functional modes, Programming and Operational.

In the *Programming mode*, the AZT70/71 is used by the manufacturer to set the capacitance value to control the desired center frequency of the oscillator. The programming mode uses either the shift registers or EEPROM (detailed later) and gives the manufacturer access to pins DA, CLK, and PV which allow the AZT70/71 to be programmed with the (AZPB70) along with the included software (Figure 11).

In the *Operational mode*, the EEPROM internal to the AZT70/71 has already been programmed with the desired factory settings. Pins DA, CLK, and PV are to be disconnected, thereby allowing the AZT70/71's internal pull-downs to place the pins at ground potential. In the operational mode, only 3 pins are necessary for hookup (Figure 12).

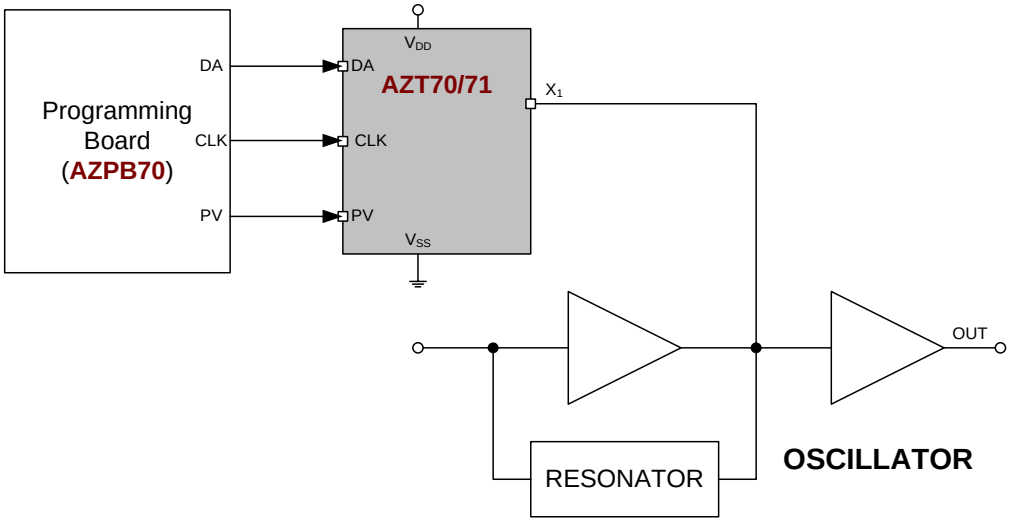

Figure 11 – AZT70/71 in Programming Mode

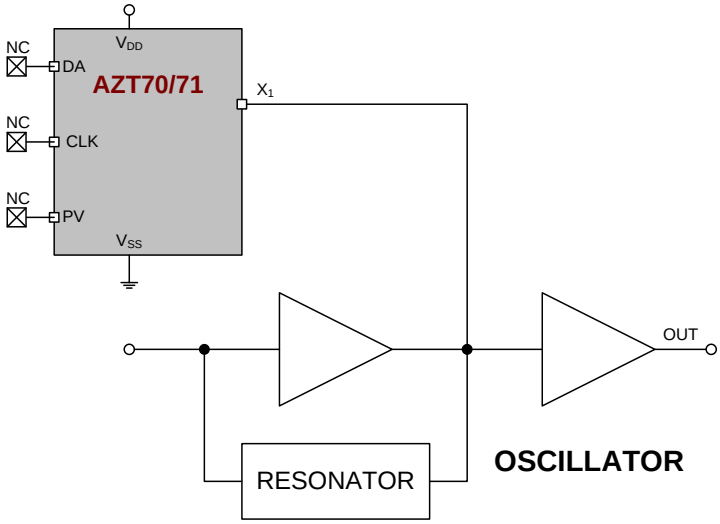

Figure 12 – AZT70/71 in Operational Mode

PROGRAMMING MODES

The AZT70/71 has two capacitance setting modes from which bits are set and the matching capacitors are selected. ***Note that all the following described operations can be simply controlled through the included software and programmer board detailed previously.***

- **Reading directly from the shift register**
  - This is useful for testing the capacitance and subsequent oscillator frequency. This mode is active after the last bit is shifted in and when the CLK pin is left logic high. *For the shift register, capacitors are selected when bits are active HIGH.*

- **Reading from the value contained in the EEPROM**
  - Prevents customer adjustment and retains factory programming and is active when the CLK pin is at logic low or not connected. *For the EEPROM, capacitors are selected when bits are active LOW.*

PROGRAMMING FROM THE SHIFT REGISTER

To initially determine the capacitance value for the desired center frequency of the oscillator one should set the capacitance of the AZT70/71 directly from the active shift register bits. To accomplish this, the CLK pin is left high after the last control word bit has been shifted in. Figure 13 shows the control word 11001100100 has been serially entered into the register. Note that bit0 is the 1st bit to enter and bit10 is the last. In the AZT70, bit0, bit9 & bit10 do not affect the capacitance value but still must be included in the serial bit stream. For the shift register, capacitors are selected when bits are active HIGH.

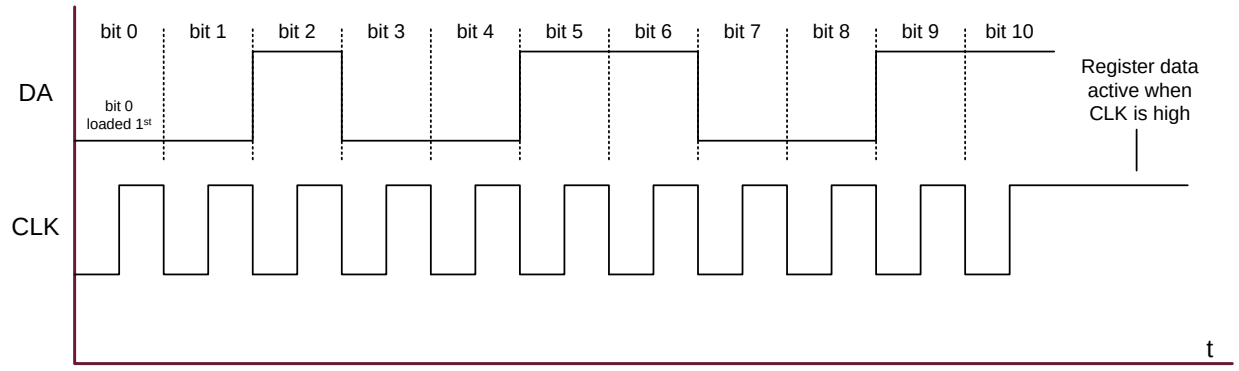

Figure 13 - Shift register programming

WRITING DATA TO THE EEPROM

Once the desired capacitance value has been determined, the digital control word can be written or re-written into the EEPROM. By storing the control word in the EEPROM, the customer is prevented from making adjustments from the factory set programming data. This is accomplished within the AZT70/71 with internal pull-downs on the DA, PV, and CLK pins. The detailed sequence for writing data to the EEPROM within the AZT70/71 is described in Table 5. Note that with EEPROM, capacitors are selected when bits are active LOW.

Table 5 – Data writing sequence for EEPROM

Step	Action
1	Determine the desired capacitor control word with the operational power supply voltage and desired oscillator conditions
2	Set the V_{DD} supply voltage to +5.0V
3	If EEPROM is not already erased, erase EEPROM (see **ERASING THE EEPROM**)
4	Read the current state of the EEPROM bits (see **READING BACK FROM THE EEPROM**)
5	Compare the desired control word to the stored EEPROM control word. Count the number of differences so as to prevent double/redundant writing
6	One bit at a time, load the first desired control word bit (bit selection for EEPROM is active LOW)
7	Set the PV pin to +6V (≥5.6V, ≤6.1V) with the pulse and idle shown in timing diagram (Figure 15)
8	Progress through all necessary control word bits by repeating steps 5 & 6 until all bits are set to the desired control word.
9	Verify the correct EEPROM contents by reading back the individual bits

For an example of writing bits into the EEPROM, suppose the desired capacitance is 3.43pF (AZT70). The control word becomes '00000010100' (Figure 14). Also suppose the EEPROM bits have been erased and therefore logic high (The AZT70/71 is initially shipped in this condition). Since bit0 is the first bit to be loaded, the bit sequence becomes 0-0-1-0-1-0-0-0-0-0-0. However, as described before, selecting bits for the EEPROM are active LOW, which will invert the logical values in the sequence to 1-1-0-1-0-1-1-1-1-1-1 (Figure 15). Note the differences between the EEPROM bits and the converted control word. Since there are 2 differences, two write cycles are required as only 1 bit should be written at a time. Figure 15 shows the timing for bit2 while Figure 16 shows the timing for bit4. ***Note that all the just described operations are internally performed through the included software and programmer board detailed previously.***

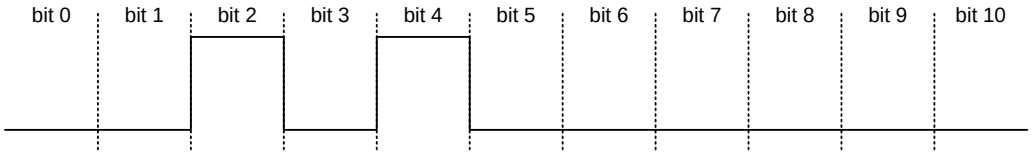

Figure 14 – Desired control word

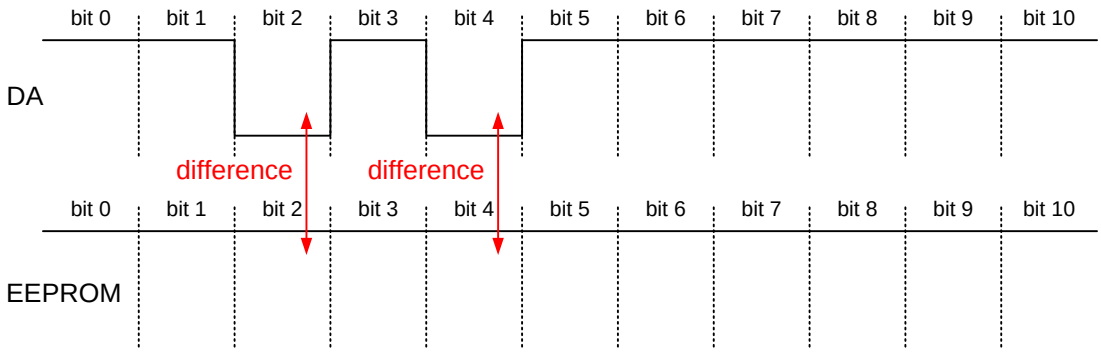

Figure 15 – Converted control word and differences from known EEPROM states

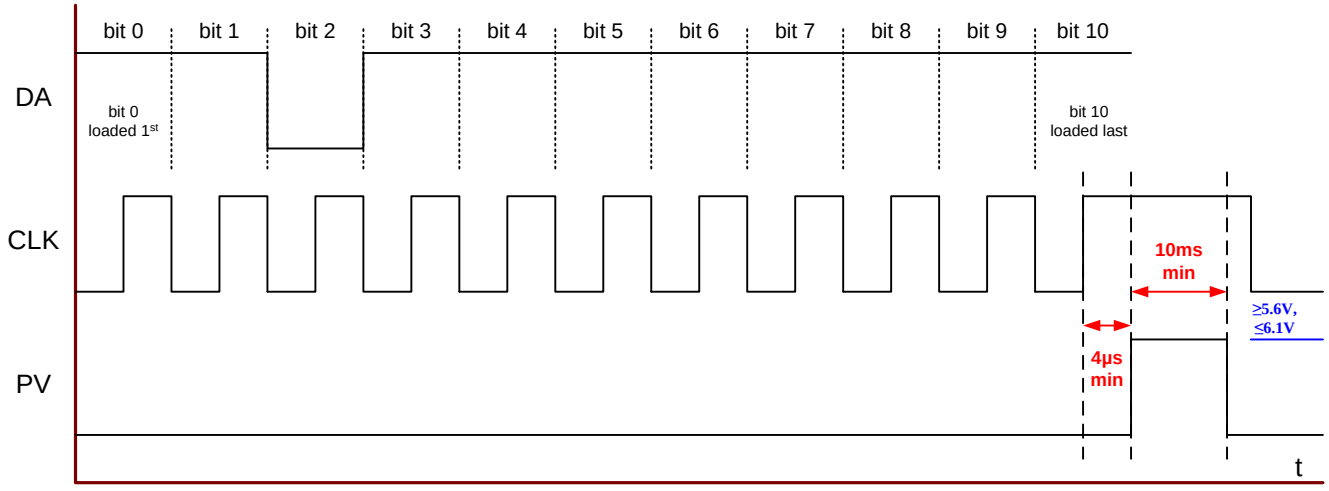

Figure 16 – First programming cycle to program bit2 into the EEPROM

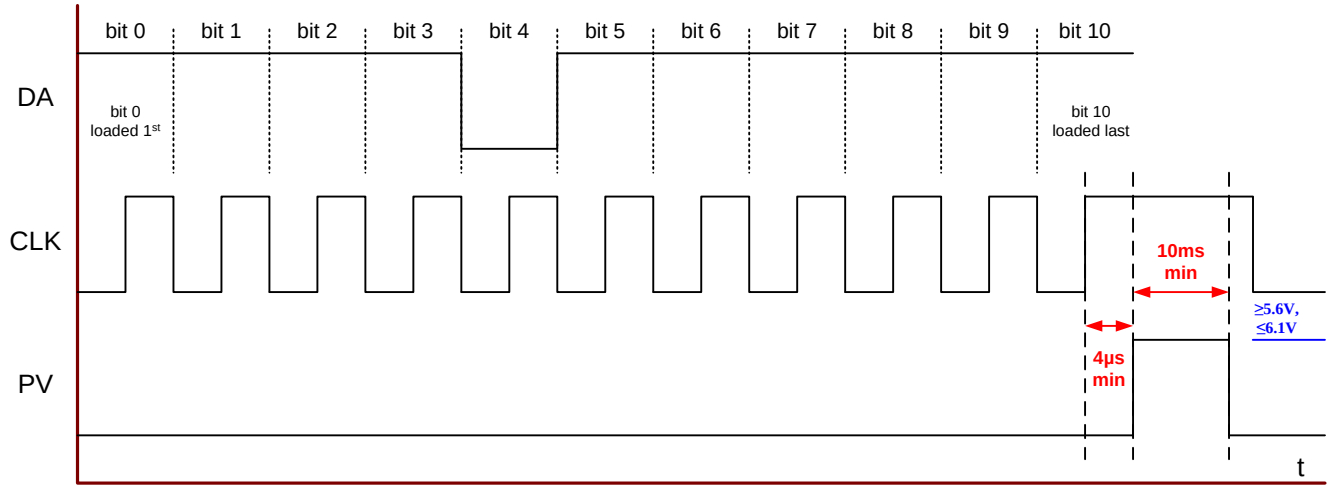

Figure 17 – Second programming cycle to program bit4 into the EEPROM

READING BACK FROM THE EEPROM

During programming, the PV pin is used to program the necessary control bits into the EEPROM. However, it is also used to read the bits currently programmed into the EEPROM. When the PV pin is not used during programming, the AZT70/71 provides a weak pull-up and pull-down on the pin. This allows the EEPROM data to be shifted out to the PV pin and read after the CLK sequence is complete and when the DA & CLK pins are high (Figure 18). Each EEPROM bit is selected by setting the DA signal low (EEPROM selection is active low) during the CLK sequence. With an external 68kΩ resistor pull-up to V_{DD} on the PV pin, a low EEPROM bit produces ≤ 0.4V level while a high EEPROM bit produces a ≥ 0.6*V_{DD} level. ***Note that all the just described operations are internally performed through the included software and programmer board detailed previously.***

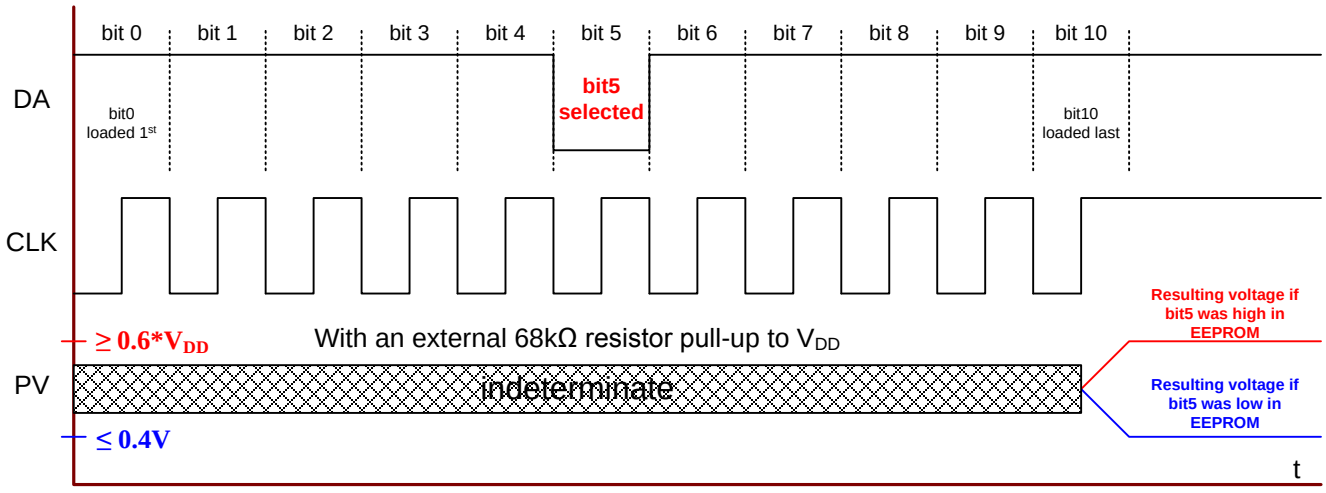

Figure 18 – Timing diagram to read bits from EEPROM

ERASING THE EEPROM

The EEPROM can be erased by initiating a programming cycle with all DA bits set high, including bit9 and bit10. After the programming cycle, all the EEPROM bits are set low (logical high) except for the check bit (bit0), which remains high. ***Note that all the just described operations are internally performed through the included software and programmer board detailed previously.***

Table 6 – Erase sequence for EEPROM

Step	Action
1	Set the V_{DD} supply voltage to +5.0V
2	Load the programming word bits all high.
3	Set the PV pin to +6V (≥5.6V, ≤6.1V) with the pulse and idle shown in timing diagram (Figure 19)
4	Verify the correct EEPROM contents by reading back the individual bits

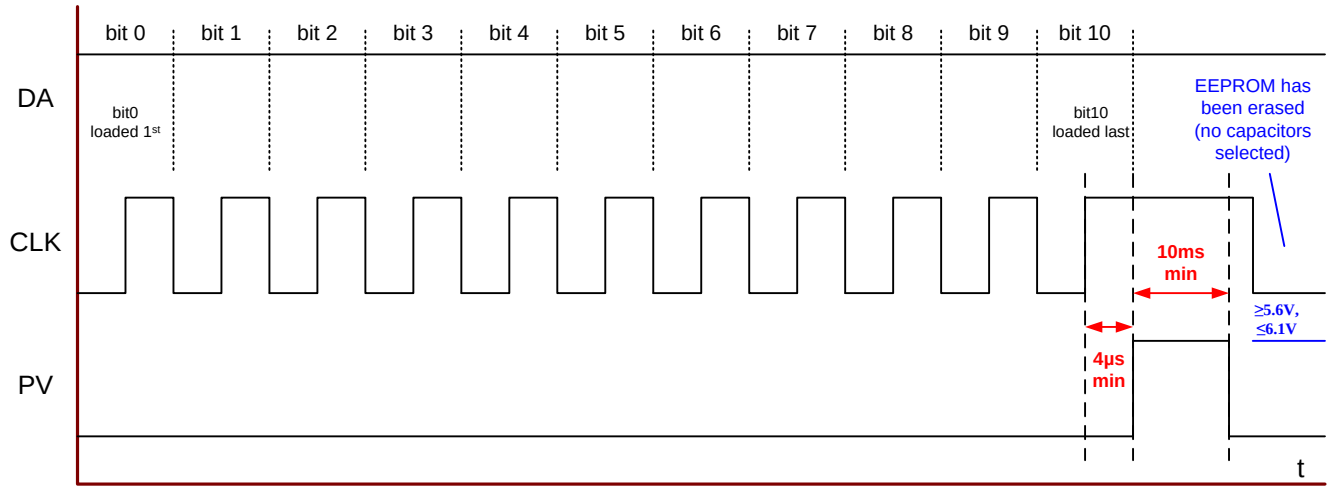

Figure 19 – Programming Sequence for erasing the EEPROM

PROGRAMMING VOLTAGE LIMIT CIRCUIT

Some existing programming circuits use a current source connected to a 6.5 – 8.0 V supply. That circuit produces an excessive voltage on the PV pin, which can damage the AZT70/71. A simple modification eliminates the issue and maintains full programming compatibility with existing programming methods. A 5.6 V, ½ watt Zener, 1N5232B or equivalent, placed between the PV pin and ground will limit the voltage while still allowing the programming circuit to generate the current required for programming fuse link type parts.