

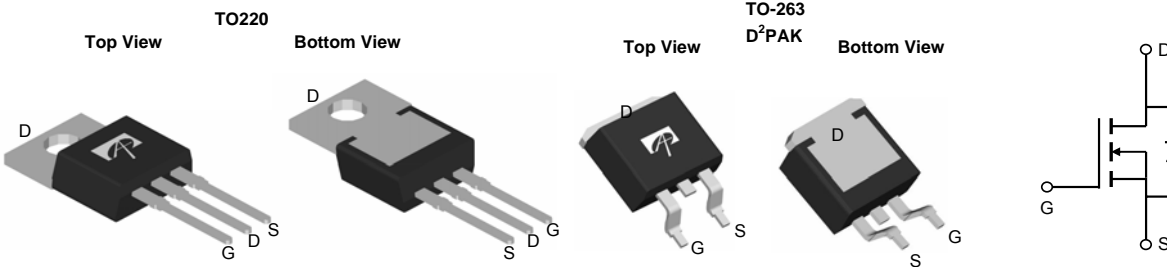
### General Description

The AOT482L/AOB482L is fabricated with SDMOS™ trench technology that combines excellent  $R_{DS(ON)}$  with low gate charge and low  $Q_{tr}$ . The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

### Product Summary

$V_{DS}$	80V
$I_D$ (at $V_{GS}=10V$ )	105A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 7.2m $\Omega$
$R_{DS(ON)}$ (at $V_{GS} = 7V$ )	< 9m $\Omega$

100% UIS Tested  
 100%  $R_g$  Tested



### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	80	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ C$	105
		$T_C=100^\circ C$	82
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	330	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ C$	11
		$T_A=70^\circ C$	9
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	82	A
Avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AS}, E_{AR}$	336	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	333
		$T_C=100^\circ C$	167
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ C$	2.1
		$T_A=70^\circ C$	1.3
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	11	15	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>				
Maximum Junction-to-Case	$R_{\theta JC}$	0.36	0.45	$^\circ C/W$

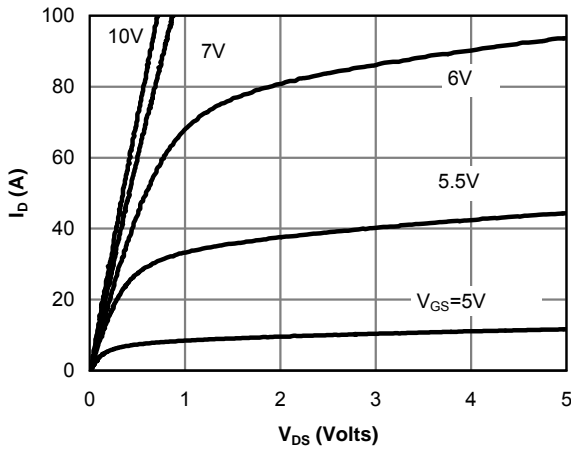
**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	80			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			10 50	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±25V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	2.5	3.1	3.7	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	330			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A TO220 T <sub>J</sub> =125°C		5.9 11	7.2 13	mΩ
		V <sub>GS</sub> =7V, I <sub>D</sub> =20A TO220		6.8	9	
		V <sub>GS</sub> =10V, I <sub>D</sub> =20A TO263		5.6	6.9	mΩ
		V <sub>GS</sub> =7V, I <sub>D</sub> =20A TO263		6.5	8.7	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		50		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.64	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>6</sup>				105	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =40V, f=1MHz	3240	4054	4870	pF
C <sub>oss</sub>	Output Capacitance		320	458	600	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		95	160	225	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.2	0.45	0.7	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =40V, I <sub>D</sub> =20A	53	66.8	81	nC
Q <sub>gs</sub>	Gate Source Charge		16	20.8	25	nC
Q <sub>gd</sub>	Gate Drain Charge		12	20.2	30	nC
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =40V, R <sub>L</sub> =2Ω, R <sub>GEN</sub> =3Ω		26		ns
t <sub>r</sub>	Turn-On Rise Time			18		ns
t <sub>D(off)</sub>	Turn-Off Delay Time			48		ns
t <sub>f</sub>	Turn-Off Fall Time			21		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time		I <sub>F</sub> =20A, dI/dt=500A/μs	18	26	34
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs	75	108	140	nC

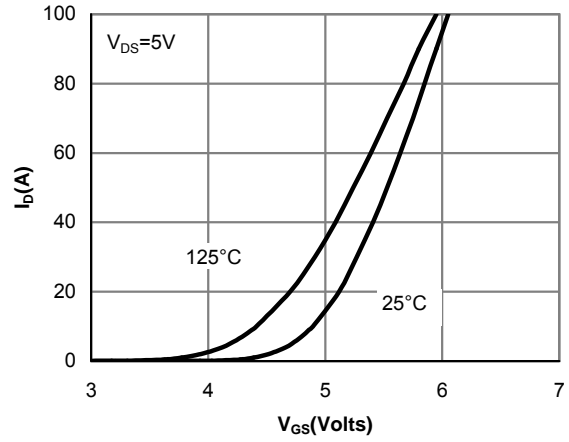
- A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.
- B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.
- D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C. The SOA curve provides a single pulse rating.
- G. The maximum current rating is package limited.
- H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

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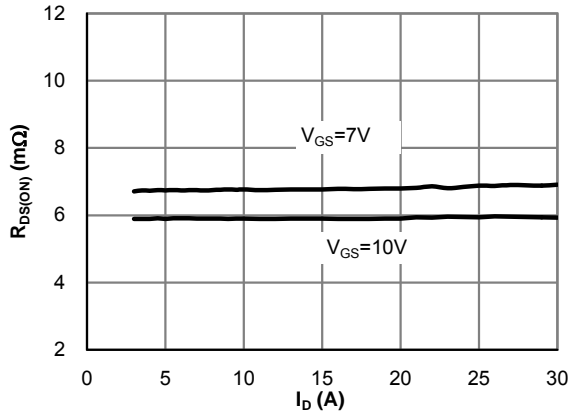
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



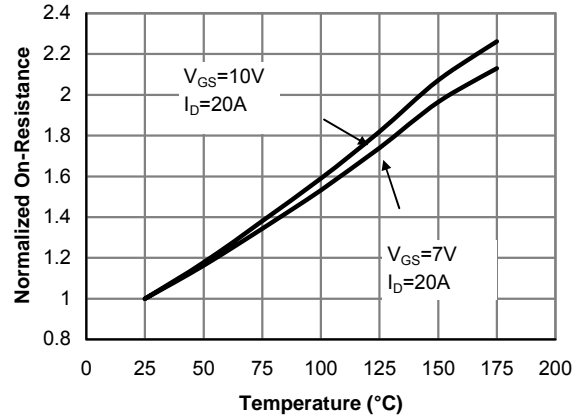
**Fig 1: On-Region Characteristics (Note E)**



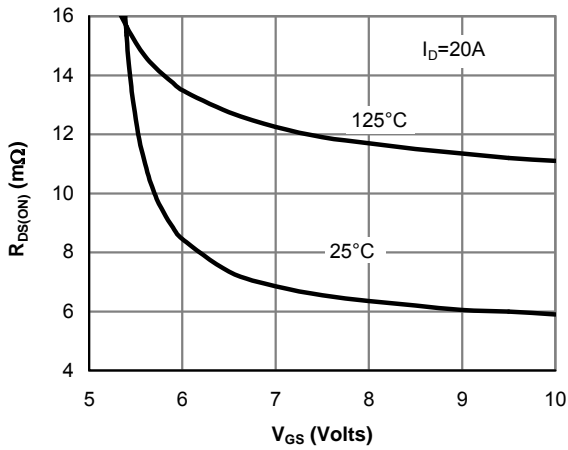
**Figure 2: Transfer Characteristics (Note E)**



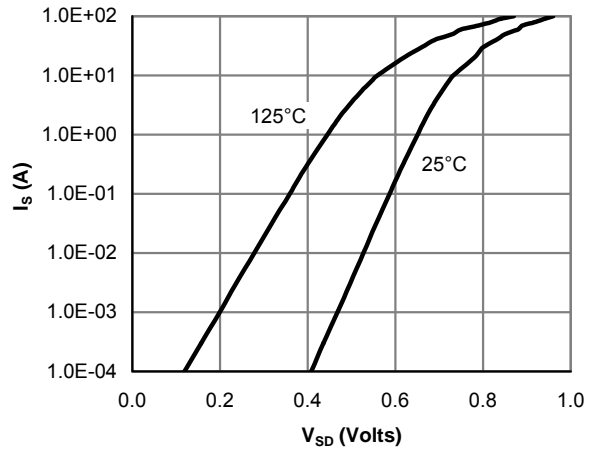
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**



**Figure 6: Body-Diode Characteristics (Note E)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

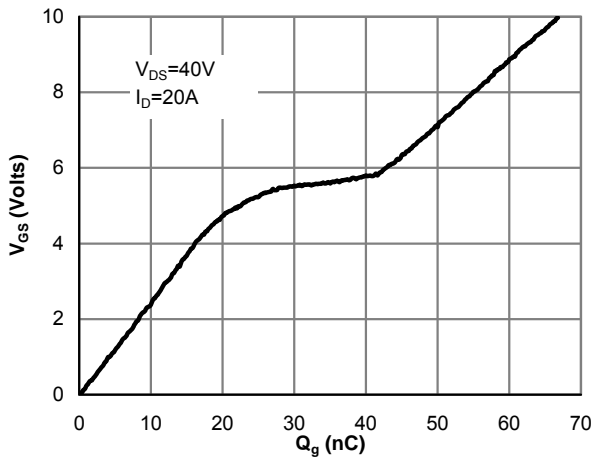


Figure 7: Gate-Charge Characteristics

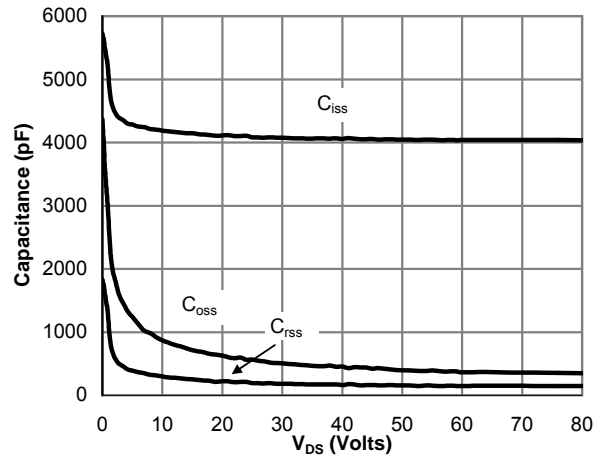


Figure 8: Capacitance Characteristics

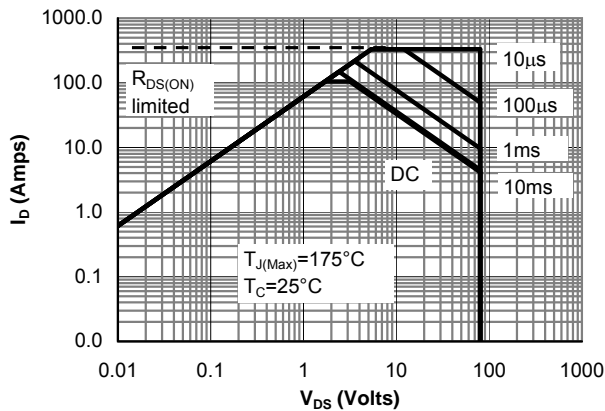


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

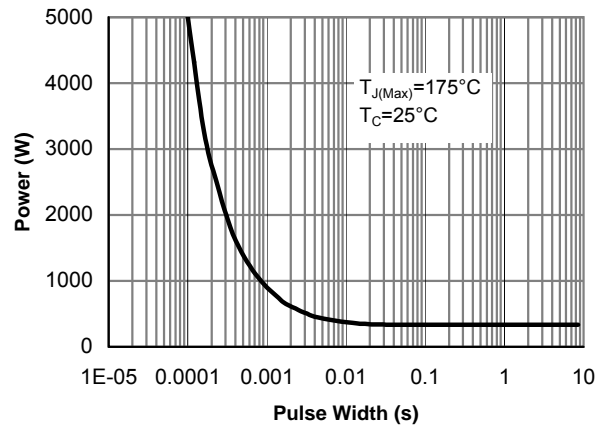


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

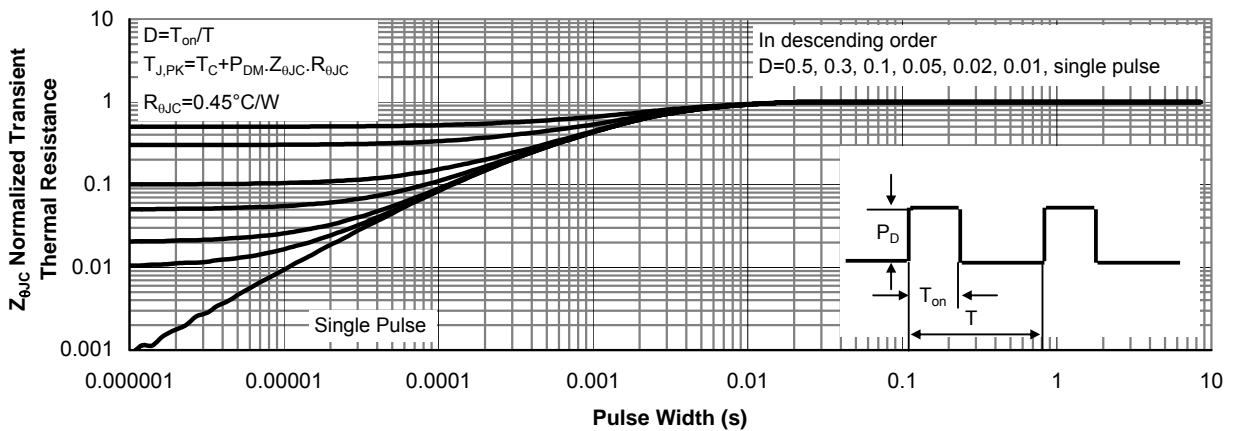
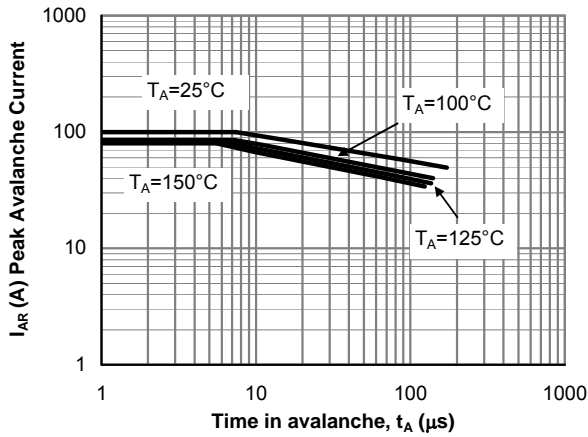
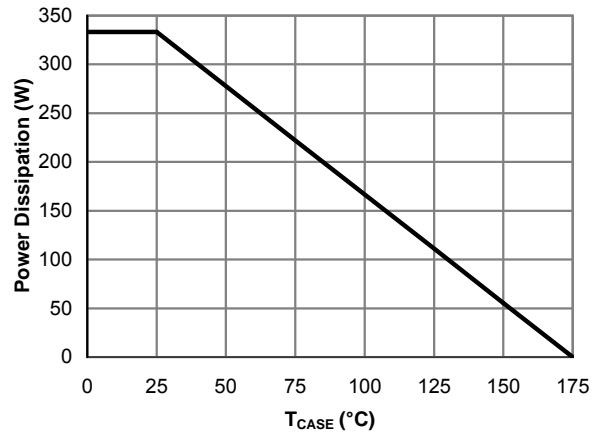


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

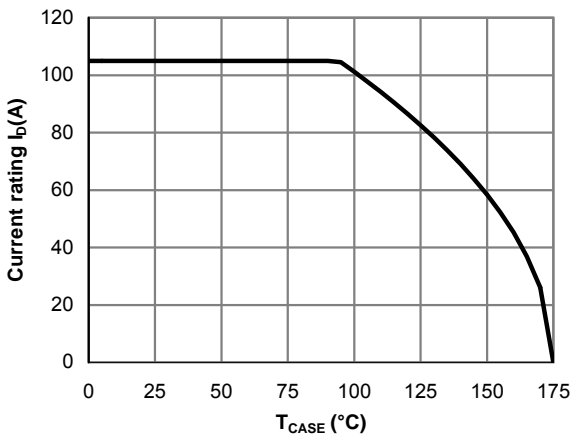
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



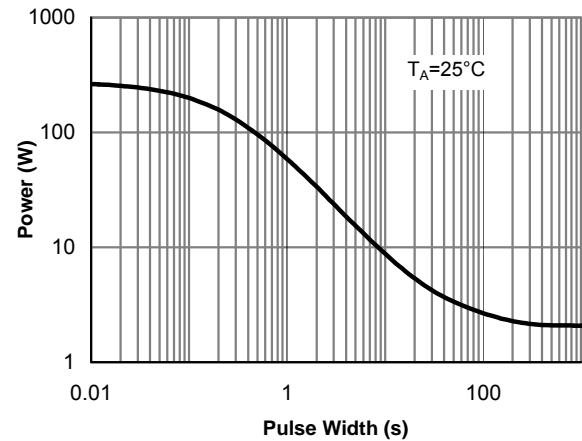
**Figure 12: Single Pulse Avalanche capability (Note C)**



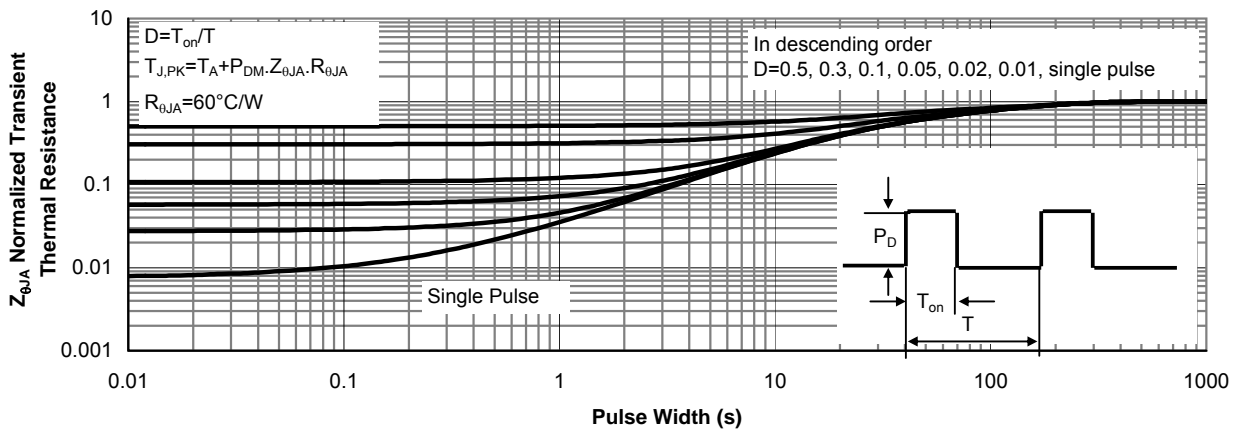
**Figure 13: Power De-rating (Note F)**



**Figure 14: Current De-rating (Note F)**

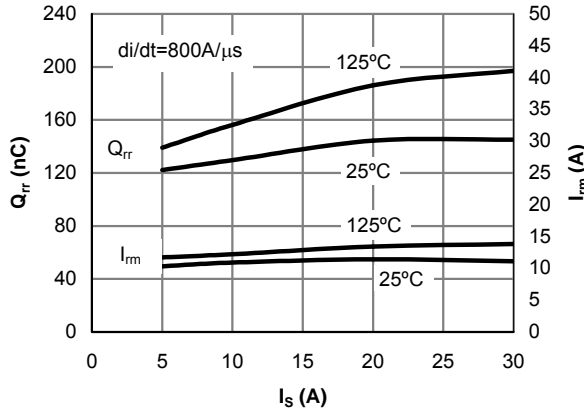


**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

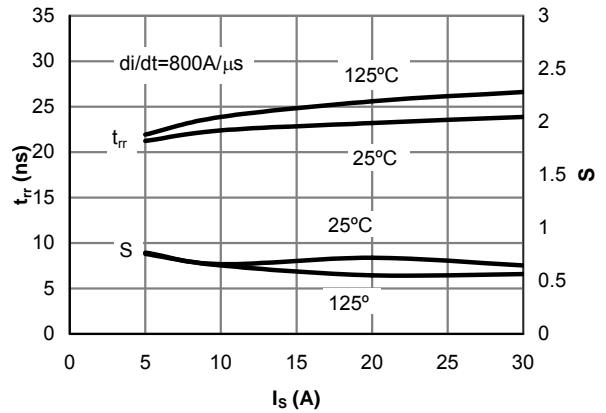


**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

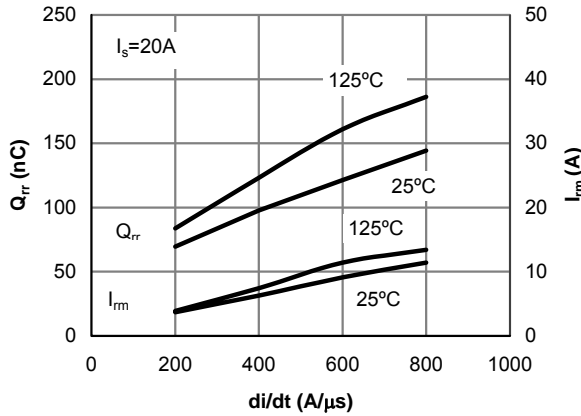
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



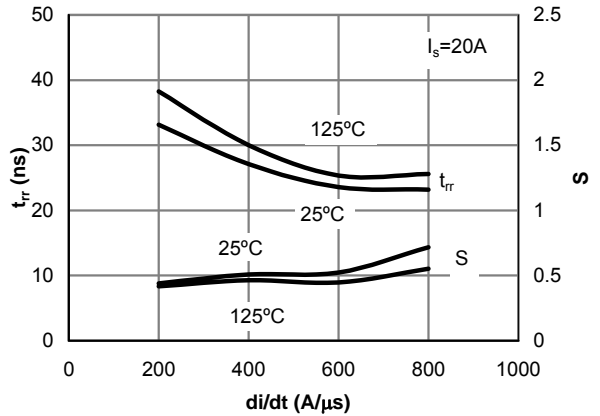
**Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current**



**Figure 18: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current**

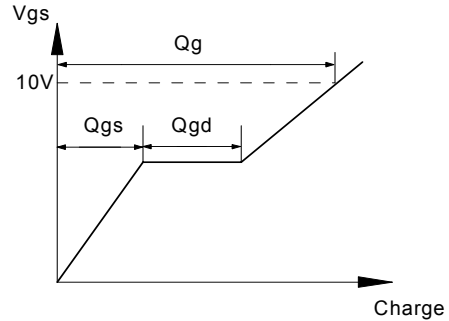
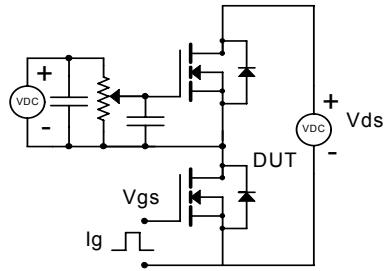


**Figure 19: Diode Reverse Recovery Charge and Peak Current vs. di/dt**

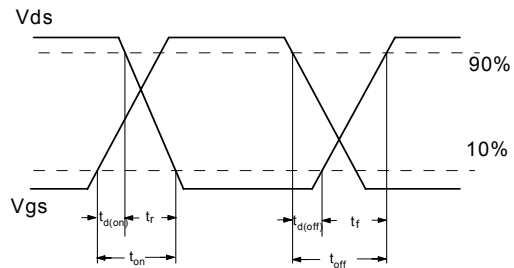
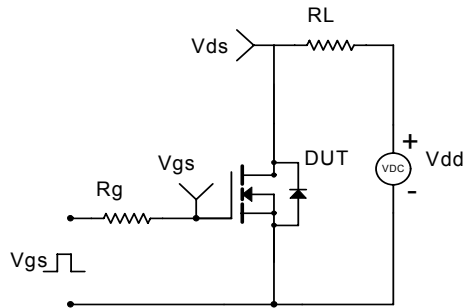


**Figure 20: Diode Reverse Recovery Time and Softness Factor vs. di/dt**

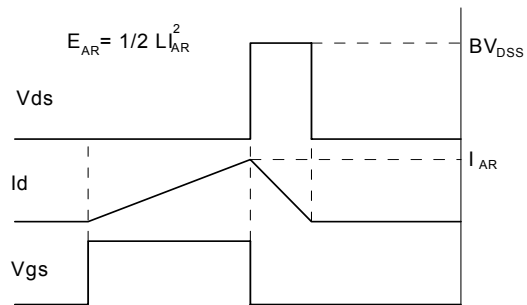
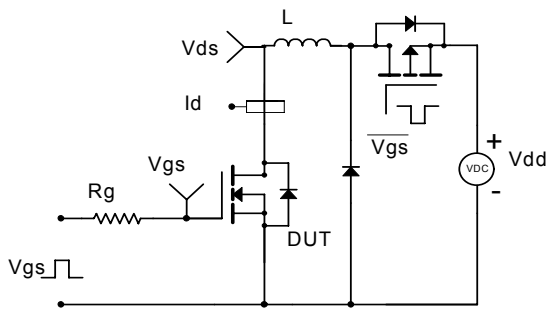
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

