SGS-THOMSON MICROELECTRONICS

ST5080A

PIAFE
PROGRAMMABLE ISDN AUDIO FRONT END

ADVANCE DATA

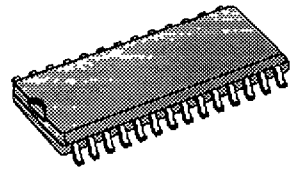
FEATURES:

Complete CODEC and FILTER system including:

- PCM ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS
- POWERFUL ANALOG FRONT END CAPABLE TO INTERFACE DIRECTLY:
  - Microphone Dynamic, Piezo or Electrete
  - Earpiece down to 100Ω or up to 150nF
  - Loudspeaker down to 50Ω or Buzzer up to 600nF.
- TRANSMIT BAND-PASS FILTER
- ACTIVE RC NOISE FILTER
- RECEIVE LOW-PASS FILTER WITH SIN X/X CORRECTION
- MU-LAW OR A-LAW SELECTABLE COMPANDING CODER AND DECODER
- PRECISION VOLTAGE REFERENCE

Phones Features:

- DUAL SWITCHABLE MICROPHONE AMPLIFIER INPUTS. GAIN PROGRAMMABLE: 15 dB RANGE, 1 dB STEP.
- LOUDSPEAKER AMPLIFIER AUXILIARY OUTPUT. ATTENUATION PROGRAMMABLE: 30 dB RANGE, 2 dB STEP.
- SEPARATE EARPIECE AMPLIFIER OUTPUT. ATTENUATION PROGRAMMABLE: 15 dB RANGE, 1 dB STEP
- AUXILIARY SWITCHABLE EXTERNAL RING INPUT (EAIN).
- TRANSIENT SUPRESSION SIGNAL DURING POWER ON.
- INTERNAL PROGRAMMABLE SIDETONE CIRCUIT. ATTENUATION PROGRAMMABLE: 15 dB RANGE, 1 dB STEP.
- INTERNAL RING OR TONE GENERATOR INCLUDING DTMF TONES, SINEWAVE OR SQUAREWAVE WAVEFORMS. ATTENUATION PROGRAMMABLE: 27 dB RANGE, 3 dB STEP.
- COMPATIBLE WITH HANDS-FREE CIRCUIT TEA7540.
- ON CHIP SWITCHABLE ANTI-ACOUSTIC FEED-BACK CIRCUIT (ANTI-LARSEN).



SO28

ORDERING NUMBER: ST5080D

General Features:

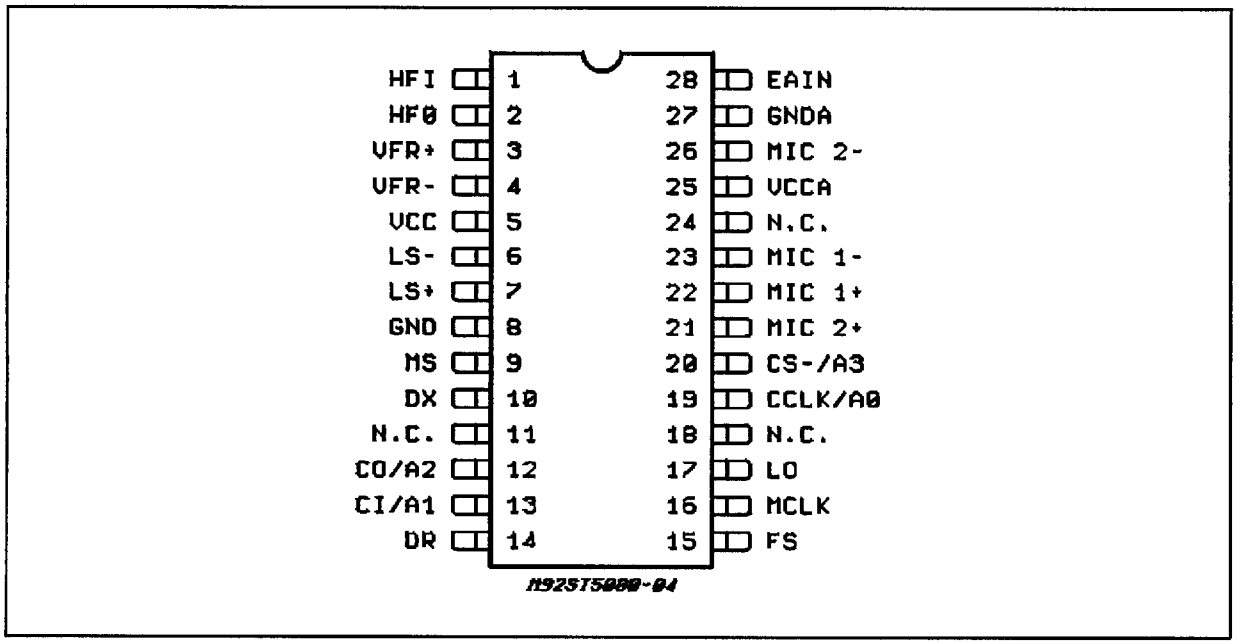
- EXTENDED TEMPERATURE RANGE OPERATION (*) – 40°C TO +85°C.
- EXTENDED POWER SUPPLY RANGE 5V±10%.
- 60 mW OPERATING POWER (TYPICAL).
- 1.0 mW STANDBY POWER (TYPICAL).
- CMOS DIGITAL INTERFACES.
- SINGLE + 5V SUPPLY.
- DIGITAL LOOPBACK TEST MODE.
- PROGRAMMABLE DIGITAL AND CONTROL INTERFACES:
  - Digital PCM Interface associated with separate serial Control Interface MICROWIRE™ compatible.
  - GCI interface compatible.

(*) Functionality guaranteed in the range – 40°C to +85°C; Timing and Electrical Specifications are guaranteed in the range – 25°C to +85°C.

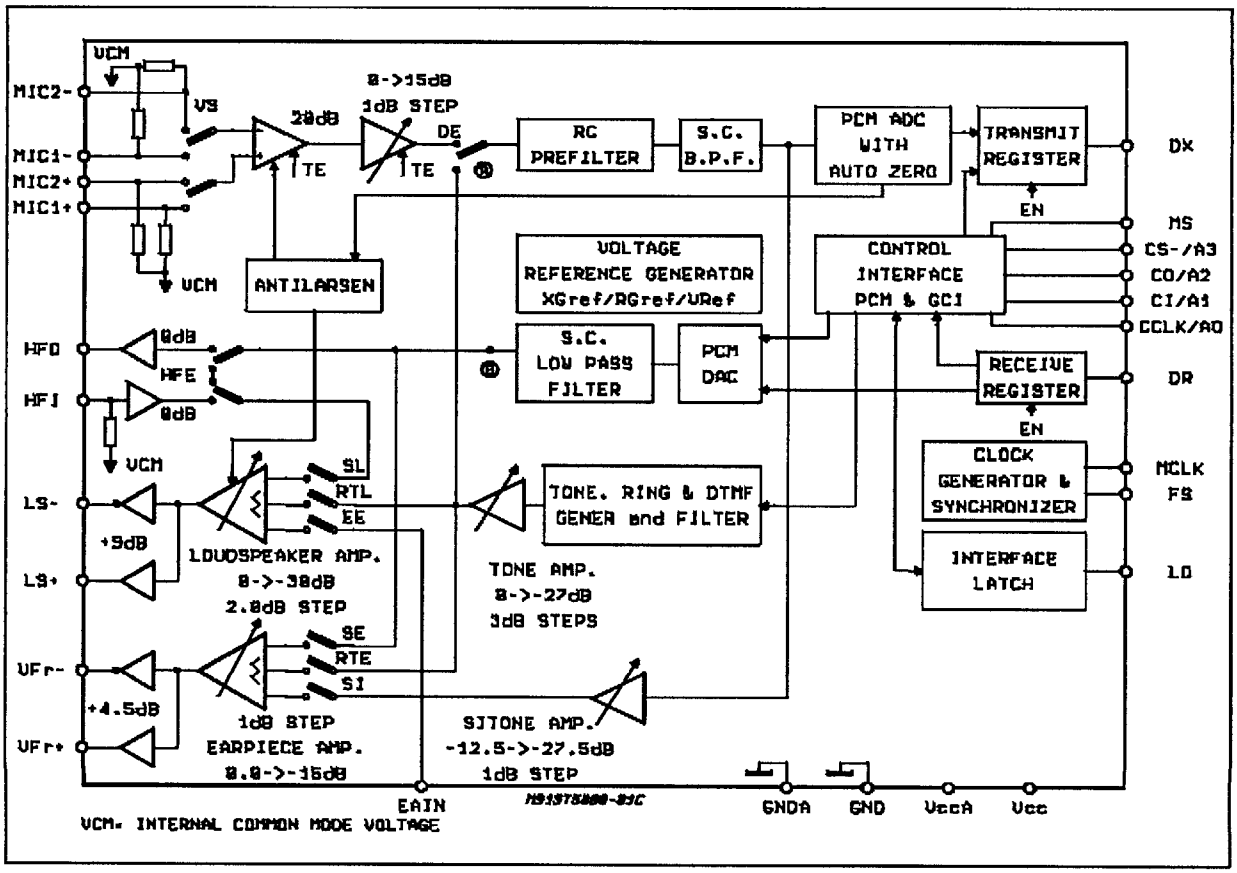
APPLICATIONS:

- ISDN TERMINALS.
- DIGITAL TELEPHONES
- CT2 AND GSM APPLICATIONS

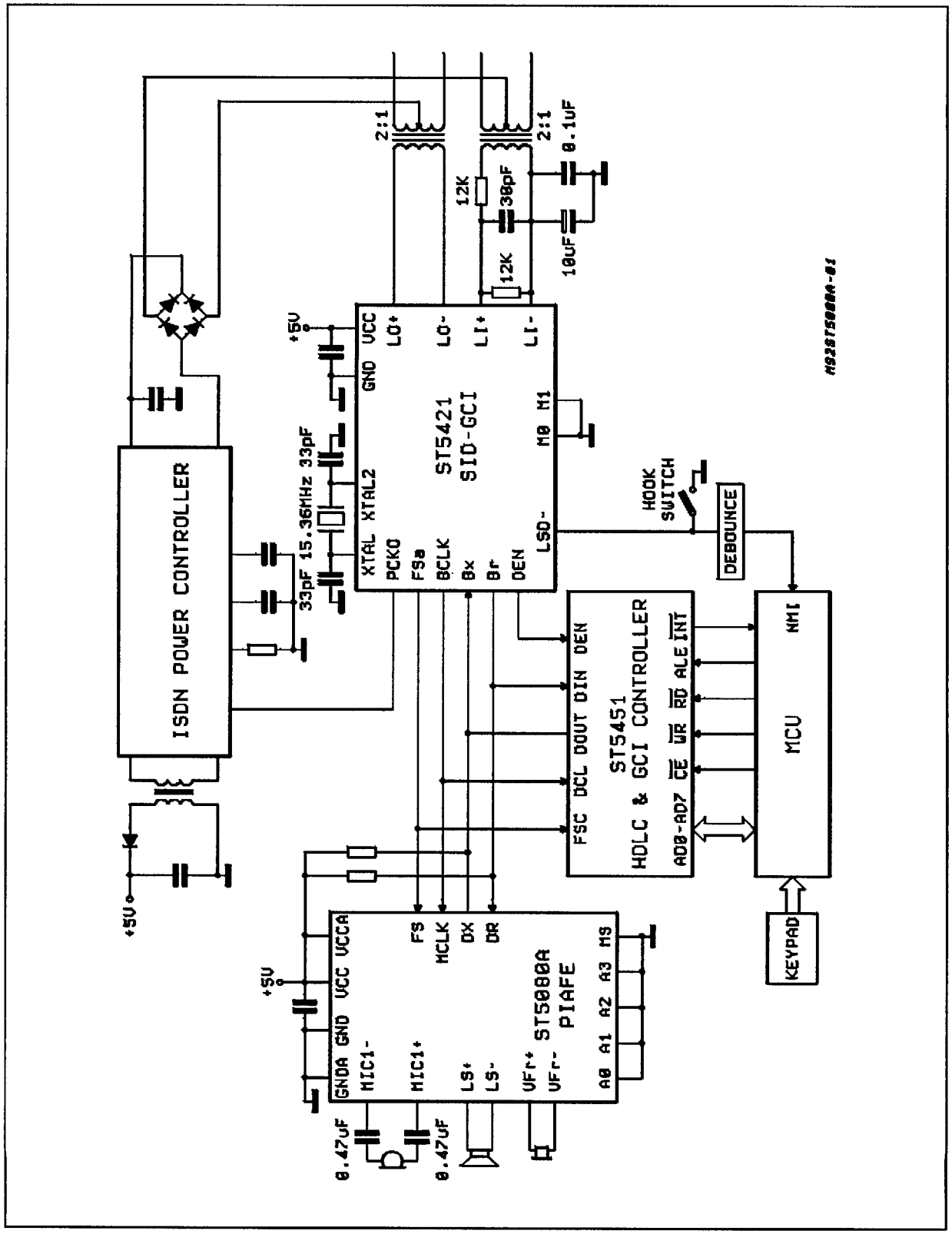
PIN CONNECTIONS (Top view)



BLOCK DIAGRAM



TYPICAL ISDN TELEPHONE SET APPLICATION



GENERAL DESCRIPTION

ST5080A PIAFE is a combined PCM CODEC/FILTER device optimized for ISDN Terminals and Digital Telephone applications. This device is A-law and Mu-law selectable and offers a number of programmable functions accessed through a serial control channel.
Depending on mode selected, channel control is provided by means of a separate serial channel control MICROWIRE compatible or multiplexed with the PCM voice data channel in a GCI compatible format requiring only 4 digital interface pins. When separate serial control interface is selected, PCM interface is compatible with Combo I and Combo II families of devices such as ETC5057/54, TS5070/71.
PIAFE is built using SGS-THOMSON's advanced HCMOS process.
Transmit section of PIAFE consists of an amplifier with switchable high impedance inputs followed by a programmable gain amplifier, an active RC antialiasing pre-filter to provide attenuation of high frequency noise, an 8th order switched capacitor band pass transmit filter and an A-law/Mu-law selectable compandig encoder.
Receive section consist of an A-law/Mu-law selectable expanding decoder which reconstructs the analog sampled data signal, a 3400 Hz low pass filter with sin X/X correction followed by two separate programmable attenuation blocks and two power amplifiers: One can be used to drive an earpiece, and the other to drive a 50 Ω loudspeaker.
Programmable functions on PIAFE include a Ring/Tone generator which provides one or two tones and can be directed to earpiece or to loudspeaker or alternatively a piezo transducer up to 600nF.
A separate programmable gain amplifier allows gain control of the signal injected. Ring/Tone generator provides sinewave or squarewave signal with precise frequencies which may be also directed to the input of the Transmit amplifier for DTMF tone generation.
An auxiliary analog input (EAIN) is also provided to enable for example the output of an external band limited Ring signal to the Loudspeaker. Transmit signal may be fed back into the receive ampifier with a programmable attenuation to provide a sidetone circuitry.
A switchable anti-accoustic feed-back system cancels the larsen effect in speech monitoring application.
Two additional pins are provided for insertion of an external Handfree function in the Loudspeaker receive path.
An output latch controlled by register programming permits external device control.

PIN FUNCTIONS

Pin	Name	Description
1,2	HFI, HFO	Hands free I/Os: These two pins can be used to insert an external Handfree circuit such as the TEA 7540 in the receive path. HFO is an output which provides the signal issued from output of the receive low pass filterwhile HFI is a high impendance input which is connected directly to one of the inputs of the Loudspeaker amplifier.
3,4	V_{Fr+}, V_{Fr-}	Receive analog earpiece amplifier complementary outputs, capable of driving load impedances between 100 and 400 Ω or a piezo up to 150nF. These outputs can drive directly earpiece transductor. The signal at this output can drive be the summ of: - Receive Speech signal from D_R, - Internal Tone Generator, - Sidetone signal.
5	V_{CC}	Positive power supply input for the digital section. +5 V ± 10%.
6,7	LS-,LS+	Receive analog loudspeaker amplifier complementary outputs, intended for driving a Loudspeaker: 80 mW on 50Ω load impedance can be provided at low distorsion meeting specifications. Alternatively this stage can drive a piezo transducer up to 600nF. The signal at these outputs can be the sum of: - Receive Speech signal from D_R, - Internal Tone generator, - External input signal from EAIN input.

PIN FUNCTIONS (continued)

Pin	Name	Description
9	MS	Mode Select: This input selects COMBO I/II interface mode with separate MICROWIRE Control interface when tied high and GCI mode when tied low.
10	D_X	Transmit Data ouput: Data is shifted out on this pin during the assigned transmit time slots. Elsewhere D_X output is in the high impendance state. In COMBO I/II mode, voice data byte is shifted out from TRISTATE output D_X at the MCLK frequency on the rising edge of MCLK. In GCI mode, voice data byte and control bytes are shifted out from OPEN-DRAIN output D_X at half the MCLK. An external pull up resistor is needed.
11	N.C.	No Connected.
14	D_R	Receive data input: Data is shifted in during the assigned Received time slots. In the COMBO I/II mode, voice data byte is shifted in at the MCLK frequency on the falling edges of MCLK. In the GCI mode, PCM data byte and contol byte are shifted in at half the MCLK frequency on the receive rising edges of MCLK. There is one period delay between transmit rising edge and receive rising edge of MCLK.
15	FS	Frame Sync input: This signal is a 8kHz clock which defines the start of the transmit and receive frames. Either of three formats may be used for this signal: non delayed timing mode, delayed timing and GCI compatible timing mode.
16	MCLK	Master Clock Input: This signal is used by the switched capacitor filters and the encoder/decoder sequencing logic. Values must be 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz selected by means of Control Register CR0. MCLK is used also to shift-in and out data. In GCI mode, 2.56 MHz and 512 kHz are not allowed.
17	LO	Open drain output: a logic 1 written into DO (CR1) appears at LO pin as a logic 0 a logic 0 written into DO puts LO pin in high impedance.
18	N.C.	No Connected.
21	MIC2+	Alternative positive high impedance input to transmit pre-amplifier.
22	MIC1+	Positive high impedance input to transmit pre-amplifier for microphone symetrical connection.
23	MIC1-	Negative high impedance input to transmit pre-amplifier for microphone symetrical connection.
24	N.C.	No connected.
25	V_{CCA}	Positive power supply input for the analog section. +5 V $\pm$ 10%. V_{CC} and V_{CCA} must be directly connected together.
26	MIC2-	Alternative negative high impedance input to transmit pre-amplifier.
27	GNDA	Analog Ground: All analog signals are referenced to this pin. GND and GNDA must be connected together close to the device.
28	EAIN	External Auxiliary input: This input can be used to provide alternate signals to the Loudspeaker in place of Internal Ring generator. Input signal should be voice band limited.

Following pin definitions are used only when COMBO I/II mode with separate MICROWIRE compatible serial control port is selected. (MS input set equal one)

PIN FUNCTIONS (continued)

Pin	Name	Description
12	CO	Control data Output: Serial control/status information is shifted out from the PIAFE on this pin when CS- is low on the falling odges of CCLK.
13	CI	Control data Input: Serial Control information is shifted into the PIAFE on this pin when CS- is low on the rising edges of CCLK.
19	CCLK	Control Clock input: This clock shifts serial control information into CI and out from CO when the CS- input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
20	CS-	Chip Select input: When this pin is low, control information is written into and out from the PIAFE via CI and CO pins.

Following pin definitions are used only when the GCI mode is selected. (MS input set equal zero)

PIN FUNCTIONS (continued)

Pin	Name	Description
19,13,12,20	A0,A1,A2,A3	These pins select the address of PIAFE on GCI interface and must be hardwired to either V_{CC} or GND. A0,A1,A2,A3 refer to C4,C5,C6,C7 bits of the first address byte respectively.

FUNCTIONAL DESCRIPTION

Power on initialization:
When power is first applied, power on reset cicuitry initializes PIAFE and puts it into the power down state. Gain Control Registers for the various programmable gain amplifiers and programmable switches are initialized as indicated in the Control Register description section. All CODEC functions are disabled. Digital Interface is configured in GCI mode or in COMBO I/II mode depending on Mode Select pin connection.
The desired selection for all programmable functions may be intialized prior to a power up command using Monitor channel in GCI mode or MICROWIRE port in COMBO I/II mode.

Power up/down control:
Following power-on initialization, power up and power down control may be accomplished by writing any of the control instructions listed in Table 1 into PIAFE with "P" bit set to 0 for power up or 1 for power down.
Normally, it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or in a separate single byte instruction.
Any of the programmable registers may also be modified while ST5080A is powered up or down by setting "P" bit as indicated. When power up or down control is entered as a single byte instruction, bit 1 must be set to a 0.
When a power up command is given, all de-activated circuits are activated, but output D_X will remain in the high impedance state on B time slots until the second Fs pulse after power up, even if a B channel is selected.

Power down state:
Following a period of activity, power down state may be reentered by writing a power down instruction.
Control Registers remain in their current state and can be changed either by MICROWIRE control interface or GCI control channel depending on mode selected.
In addition to the power down instruction, detection of loss MCLK (no transition detected) automatically enters the device in "reset" power down state with D_X output in the high impedance state and L0 in high impedance state.

Transmit section:
Transmit analog interface is designed in two stages to enable gains up to 35 dB to be realized. Stage 1 is a low noise differential amplifier providing 20 dB gain. A microphone may be capacitevely connected to MIC1+, MIC1- inputs, while the MIC2+ MIC2– inputs may be used to capacitively connect a second microphone (for digital handsfree operation) or an auxiliary audio circuit such as TEA 7540 Hands-free circuit. MIC1 or MIC2 source is selected with bit 7 of register CR4.
Following the first stage is a programmable gain amplifier which provides from 0 to 15 dB of additional gain in 1 dB step. The total transmit gain should be adjusted so that, at reference point A, see Block Diagram description, the internal 0 dBmO voltage is 0.739 V (overload level is 1.06 Vrms). Second stage amplifier can be programmed with bits 4 to 7 of CR5. To temporarily mute the transmit input, bit TE (6 of CR4) may be set low. In this case, the analog transmit signal is grounded and the sidetone path is also disabled.
An active RC prefilter then precedes the 8th order band pass switched capacitor filter. A/D converter has a compressing characteristic according to CCITT A or mu255 coding laws, which must be selected by setting bits MA, IA in register CR0. A precision on chip voltage reference ensures accurate and highly stable transmission levels.
Any offset voltage arising in the gain-set amplifier, the filters or the comparator is cancelled by an internal autozero circuit.
Each encode cycle begins immediatly at the beginning of the selected Transmit time slot. The total signal delay referenced to the start of the time slot is approximatively 195 µs (due to the transmit filter) plus 123 µs (due to encoding delay), which totals 320 µs. Voice data is shifted out on D_X during the selected time slot on the transmit rising adges of MCLK.

Receive section:
Voice Data is shifted into the decoder's Receive voice data Register via the D_R pin during the selected time slot on the 8 receive edges of MCLK.
The decoder consists of an expanding DAC with either A or MU255 law decoding characteristic which is selected by the same control instruction used to select the Encode law during intitialization. Following the Decoder is a 3400 Hz 6th order low pass switched capacitor filter with integral Sin X/X correction for the 8 kHz sample and hold.
0 dBmO voltage at this (B) reference point (see Block Diagram description) is 0.49 Vrms. A transcient suppressing circuitry ensure interference noise suppression at power up.
The analog speech signal output can be routed either to earpiece (V_{FR+}, V_{FR-} outputs) or to loudspeaker (LS+, LS- outputs) by setting bits SL and SE (1 and 0 of CR4).
Total signal delay is approximatively 190 µs (filter plus decoding delay) plus 62.5 µs (1/2 frame) which gives approximatively 252 µs.
Differential outputs V_{FR+},V_{FR-} are intended to di-

rectly drive an earpiece. Preceding the outputs is a programmable attenuation amplifier, which must be set by writing to bits 4 to 7 in register CR6. Attenuations in the range 0 to -15 dB relative to the maximum level in 1 dB step can be programmed. The input of this programmable amplifier is the summ of several signals which can be selected by writing to register CR4.:

- Receive speech signal which has been decoded and filtered,
- Internally generated tone signal, (Tone amplitude is programmed with bits 4 to 7 of register CR7),
- Sidetone signal, the amplitude of which is programmed with bits 0 to 3 of register CR5

V_{FR+} and V_{FR-} outputsare capable of driving output power level up to 14mW into differentially connected load impedance between 100 and 400 Ω.

Differential outputs LS+,LS- are intended to directly drive a Loudspeaker. Preceding the outputs is a programmable attenuation amplifier, which must be set by writing to bits 0 to 3 in register CR6. Attenuations in the range 0 to -30 dB relative to the maximum level in 2.0 dB step can be programmed. The input of this programmable amplifier can be the summ of signals which can be selected by writing to register CR4:

- Receive speech signal which has been decoded and filtered,
- Internally generated tone signal, (Tone amplitude is programmed with bits 4 to 7 of register CR7),
- EAIN input which may be an alternate Ring signal or any voice frequency band limited signal. (An external decoupling capacitor of about 0.1µF is necessary).

Receive voice signal may be directed to output HFO by means of bit HFE in Register CR4. After processing, signal must be re-entered through input HFI to Loudspeaker amplifier input. (An external decoupling capacitor of about 0.1µF is necessary).
LS+ and LS- outputs are capable of driving output power level up to 80 mW into 50 Ω differentially connected load impedance at low distortion meeting PCM channel specifications. When the signal source is a Ring squarewave signal, power levels up to approximatively 200 mW can be delivered.

Anti-acoustic feed-back for loudspeaker to handset microphone loop with squelch effect: on chip switchable anti-larsen for loudspeaker to handset microphone feedback is implemented. A 12dB depth gain control on both transmit and receive path is provided to keep constant the loop gain. On the transmit path the 12dB gain control is provided starting from the CR5 transmit gain definition; at the same time, on the receive path the 12dB gain control is provided starting from CR6 receive gain definition.

Digital and Control Interface:
PIAFE provides a choice of either of two types of Digital Interface for both control data and PCM.
For compatibility with systems which use time slot oriented PCM busses with a separate Control Interface, as used on COMBO I/II families of devices, PIAFE functions are described in next section.
Alternatively, for systems in which PCM and control data are multiplexed together using GCI interface scheme, PIAFE functions are described in the section following the next one.
PIAFE will automatically switch to one of these two types of interface by sensing the MS pin.
Due to Line Transceiver clock recovery circuitry, a low jitter may be provided on F_S and MCLK clocks. F_S and MCLK must be always in phase. For ST5421S Transceiver, as an example, maximun value of jitter amplitude is a step of 65 ns at each GCI frame (125µs). So, the maximum jitter amplitude is 130 ns pk-pk.

COMBO I/II mode.
Digital Interface (Fig. 1)
F_S Frame Sync input determines the beginning of frame. It may have any duration from a single cycle of MCLK to a squarewave. Two different relationships may be established between the Frame Sync input and the first time slot of frame by setting bit 3 in register CR0. Non delayed data mode is similar to long frame timing on ETC5057/ TS5070 series of devices (COMBO I and COMBO II respectively): first time slot begins nominally coincident with the rising edge of F_S. Alternative is to use delayed data mode, which is similar to short frame sync timing on COMBO I or COMBO II, in which F_S input must be high at least a half cycle of MCLK earlier the frame beginning. A time slot assignment circuit on chip may be used with both timing modes, allowing connection to one of the two B1 and B2 voice data channels.
Two data formats are available: in Format 1, time slot B1 corresponds to the 8 MCLK cycles following immediately the rising edge of FS, while time slot B2 corresponds to the 8 MCLK cycles following immediately time slot B1.
In Format 2, time slot B1 is identical to Format 1. Time slot B2 appears two bit slots after time slot B1. This two bits space is left available for insertion of the D channel data.
Data format is selected by bit FF (2) in register CR0. Time slot B1 or B2 is selected by bit T0 (0) in Control Register CR1.
Bit EN (2) in control register CR1 enables or disables the voice data transfer on D_X and D_R as appropriate. During the assigned time slot, D_X

Figure 1: Digital Interface Format

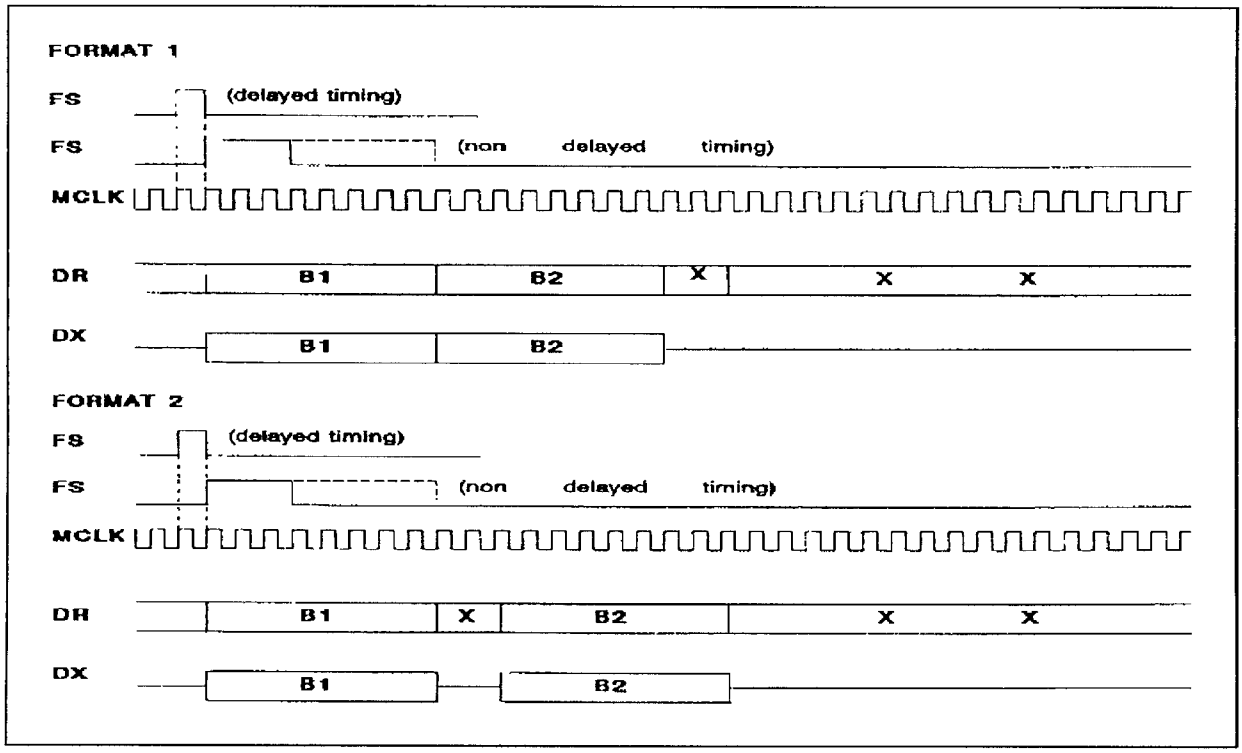
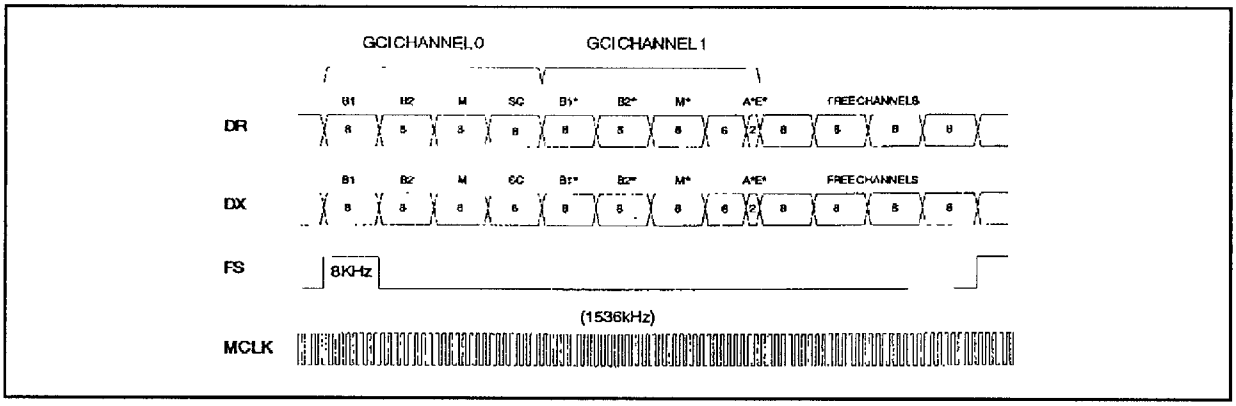


Figure 2: GCI Interface Frame Structure



output shifts data out from the voice data register on the rising edges of MCLK. Serial voice data is shifted into D_R input during the same time slot on the falling edges of MCLK.
D_X is in the high impedance Tristate condition when in the non selected time slots.

Control Interface:
Control information or data is written into or read-back from PIAFE via the serial control port consisting of control clock CCLK, serial data input CI and output CO, and Chip Select input, CS-. All control instructions require 2 bytes as listed in Table 1, with the exception of a single byte power-up/down command.
To shift control data into ST5080A, CCLK must be pulsed high 8 times while CS- is low. Data on CI input is shifted into the serial input register on the rising edge of each CCLK pulse. After all data is shifted in, the content of the input shift register is decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide CS- pulse or may follow the first contiguously, i.e. it is not mandatory for CS- to return high in between the first and second control bytes. At the end of

the 2nd control byte, data is loaded into the appropriate programmable register. CS- must return high at the end of the 2nd byte.
To read-back status information from PIAFE, the first byte of the appropriate instruction is strobed in during the first CS- pulse, as defined in Table 1. CS- must be set low for a further 8 CCLK cycles, during which data is shifted out of the CO pin on the falling edges of CCLK.
When CS- is high, CO pin is in the high impedance Tri-state, enabling CO pins of several devices to be multiplexed together.
Thus, to summarise, 2 byte READ and WRITE instructions may use either two 8-bit wide CS- pulses or a single 16 bit wide CS- pulse.

Control channel access to PCM interface:
It is possible to access the B channel previously selected in Register CR1.
A byte written into Control Register CR3 will be automatically transmitted from D_X output in the following frame in place of the transmit PCM data.
A byte written into Control Register CR2 will be automatically sent through the receive path to the Receive amplifiers.
In order to implement a continuous data flow from the Control MICROWIRE interface to a B channel, it is necessary to send the control byte on each PCM frame.
A current byte received on D_R input can be read in the register CR2. In order to implement a continuous data flow from a B channel to MICROWIRE interface, it is necessary to read register CR2 at each PCM frame.

GCI COMPATIBLE MODE
GCI interface is an European standardized interface to connect ISDN dedicated components in the different configurations of equipment as Terminals, Network Terminations, PBX, etc...
In a Terminal equipment, this interface called SCIT for Special Circuit Interface for Terminals allows for example connection between:
- ST5421 (SID-GCI) and ST5451 (HDLC/GCI controller) used for 16 kbit/s D channel packet frames processing and SID control,
- Peripheral devices connected to a 64 kbit/s B channel and ST5451 used for GCI peripheral control.

ST5080A may be assigned to one of the B channels present on the GCI interface and is monitored via a control channel which is multiplexed with the 64 kbit/s Voice Data channels.

Figure 2 shows the frame structure at the GCI interface. Two 256 kbit/s channel are supported.
a)GCI channel 0: It is structured in four subchannels:
- B1 channel 8 bits per frame
- B2 channel 8 bits per frame
- M channel 8 bits per frame ignored by PIAFE
- SC channel 8 bits per frame ignored by PIAFE

Only B1 or B2 channel can be selected in PIAFE for PCM data transfer.

b)GCI channel 1: It is structured also in four subchannels:
- B1* channel 8 bits per frame
- B2* channel 8 bits per frame
- M* channel 8 bits per frame
- SC* which is structured as follows:

6 bits ignored by PIAFE
A* bit associated with M* channel
E* bit associated with M* channel.
B1* or B2* channel can be selected in PIAFE for PCM data transfer.
M* channel and two associated bits E* and A* are used for PIAFE control.

Thus, to summarize, B1, B2, B1* or B2* channel can be selected to transmit PCM data and M* channel is used to read/write status/command peripheral device registers. Protocol for byte exchange on the M* channel uses E* and A* bits.

Physical Interface
The interface is physically constitued with 4 wires:

Input Data wire:	D_R
Output Data wire:	D_X
Bit Clock:	MCLK
Frame Synchronization:	F_S

Data is synchronized by MCLK and F_S clock inputs.
F_S insures reinitialization of time slot counter at each frame beginning. The rising edge or FS is the reference time for the first GCI channel bit.
Data is transmitted in both directions at half the MCLK input frequency. Data is transmitted on the the rising edge of MCLK and is sampled one period after the transmit rising edge, also on a rising edge.
Note: Transmit data may be sampled by far-end device ie SID ST5421 on the falling edge 1.5 period after the transmit rising edge.
Unused channel are high impedance. Data outputs are OPEN-DRAIN and need an external pull up resistor.

COMBO activation/deactivation
ST5080A is automatically set in power down mode when GCI clocks are idle. GCI section is reactivated when GCI clocks are detected. PIAFE is completly reactivated after receiving of a power up command.

Exchange protocol on M* channel

Protocol allows a bidirectional transfer of bytes between ST5080A and GCI controller with acknowledgment at each received byte. For PIAFE, standard protocol is simplified to provide read or write register cycles almost identical to MICROWIRE serial interface.

Write cycle
Control Unit sends through the GCI controller following bytes:

- First byte is the chip select byte. The first four bits indicate the device address: (A3,A2,A1,A0). The four last bits are ignored. ST5080A compare the validated byte received internally with the address defined by pins A3, A2, A1, A0. If comparison is true, byte is acknowledged, if not, ST5080A does not acknowledge the byte.

NOTE: An internal "message in progress" flag remains active till the end of the complete message transmission to avoid irrelevant acknowledgement of any further byte.

- Second byte is structured as defined in Table 1.
- Third byte is the Data byte to write into the Register as indicated in Table 1.

It is possible but optional to write to several different registers in a single message. In this case the Chip Select byte is sent only once at the beginning of the message, the device automatically toggles between address byte and data byte.

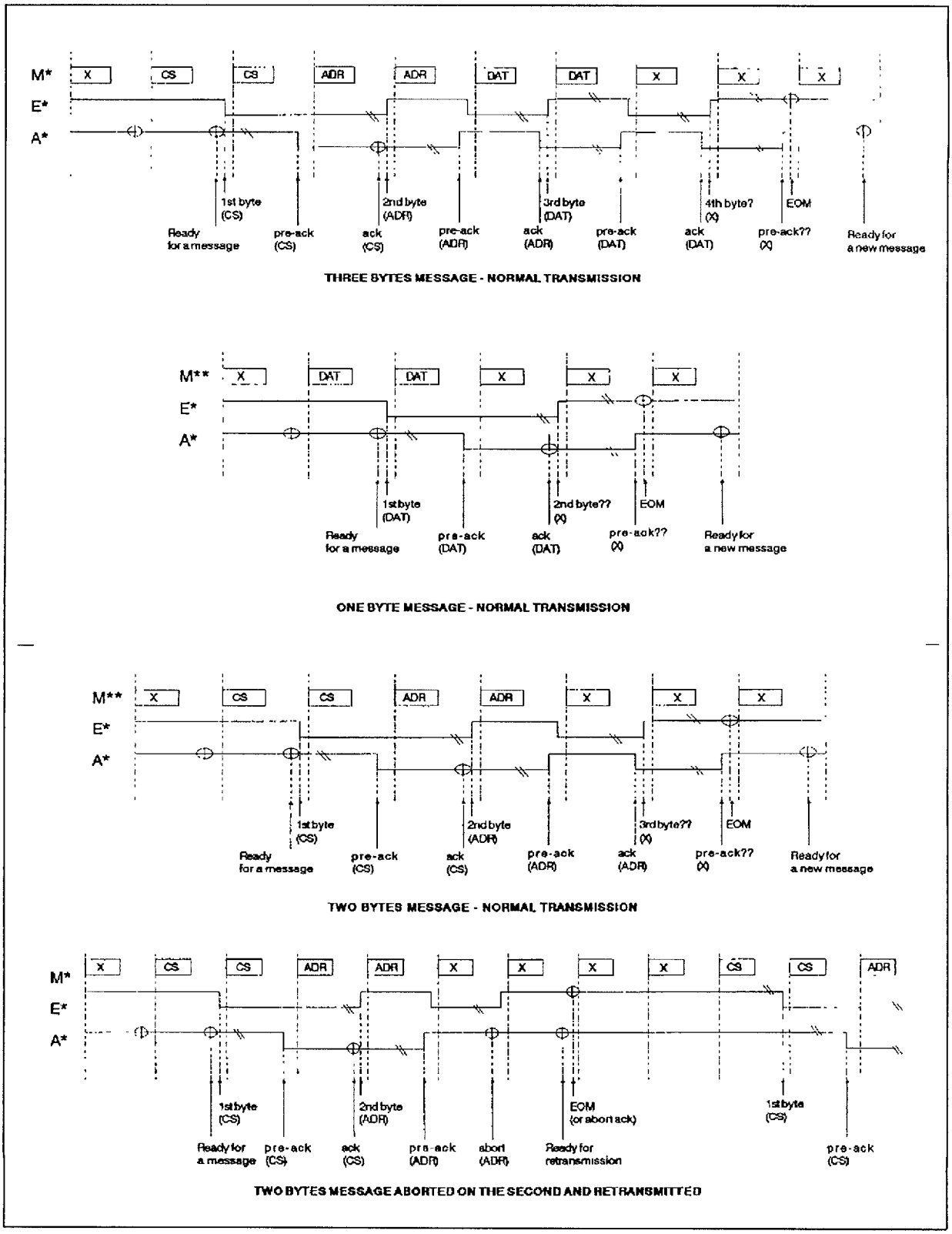
Read cycle
Control Unit sends two bytes. First byte is the chip select byte as defined above. Second byte is structured as defined in Table 1.
If PIAFE identifies a read-back cycle, bit 2 of byte 1 in Table 1 equal 1, it has to respond to the Control Unit by sending a single byte message which is the content of the addressed register.
It is possible but optional to request several different read-back register cycles in a single message but it is recommended to wait the answer before requesting a new read back to avoid loss of data. ST5080A responds by sending a single data byte message at each request.

Received byte validation:
A received byte is validated if it is detected two consecutive times identical.

Exchange Protocol:
Exchange protocol is identical for both directions.
Sender uses E* bit to indicate that it is sending a M* byte while receiver uses A* bit to acknowledge received byte.
When no message is transferred, E* bit and A* bit are forced to inactive state.
A transmission is initialized by sender putting E* bit from inactive state to active state and by sending first byte on M* channel in the same frame.
Transmission of a message is allowed only if A* bit from the receiver has been set inactive for at least two frames.
When receiver is ready, it validates the received byte internally when received in two consecutive frames identical. Then the receiver sets first A* bit from inactive to active state (pre-acknowlegement), and maintains A* bit active at least in the following frame (acknowledgement). If validation is not possible, (two last bytes received are not identical), receiver aborts the message setting A* bit active for only a single frame.
For the first byte received, Abort sequence is not allowed. PIAFE does not respond either if two last bytes are not identical or if the byte received does not meet the Chip Select byte defined by A0-A3 pins bias.
A second byte may be transmitted by the sender putting E* bit from active to inactive state and sending the second byte on the M* channel in the same frame. E* bit is set inactive for only one frame. If it remains inactive more than one frame, it is an end of message (i.e. not second byte available).
The second byte may be transmitted only after receiving the pre-acknowledgment of the previous byte transmitted (see Fig. 3). The same protocol is used if a third byte is transmitted. Each byte has to be transmitted at least in two consecutive frames.
The receiver validates current received byte as done on first byte and then set A* bit in the next two frames first from active to inactive state (pre-acknowledgement), and after from inactive to active state (acknowledgement). If the receiver cannot validate the received current byte (two bytes received are not identical), it pre-acknowledges normally, but let A* bit in the inactive state in the next frame which indicates an abort request.
If a message sent by ST5080A is aborted, it will stop the message and wait for a new read cycle instruction from the controller.
A message received by ST5080A is acknowledged or aborted without flow Control.
Figures 3 gives timing of a write cycle. Most significant bit (MSB) of a Monitor byte is sent first on M* channel.
E* and A* bits are active low and inactive state on DOUT is high impedance.

PROGRAMMABLE FUNCTIONS

Figure 3: E and A bits Timing



For both formats of Digital Interface, programmable functions are configured by writing to a number of registers using a 2-byte write cycle (not including chip select byte in GCI).
Most of these registers can also be read-back for verification. Byte one is always register address, while byte two is Data.
Table 1 lists the register set and their respective adresses.

Table 1: Programmable Register Intructions

Function	Address byte								Data byte
	7	6	5	4	3	2	1	0	
Single byte Power up/down	P	X	X	X	X	X	0	X	none
Write CR0	P	0	0	0	0	0	1	X	see CR0 TABLE 2
Read-back CR0	P	0	0	0	0	1	1	X	see CR0
Write CR1	P	0	0	0	1	0	1	X	see CR1 TABLE 3
Read-back CR1	P	0	0	0	1	1	1	X	see CR1
Write Data to receive path	P	0	0	1	0	0	1	X	see CR2 TABLE 4
Read data from D_R	P	0	0	1	0	1	1	X	see CR2
Write Data to D_X	P	0	0	1	1	0	1	X	see CR3 TABLE 5
Write CR4	P	0	1	0	0	0	1	X	see CR4 TABLE 6
Read-back CR4	P	0	1	0	0	1	1	X	see CR4
Write CR5	P	0	1	0	1	0	1	X	see CR5 TABLE 7
Read-back CR5	P	0	1	0	1	1	1	X	see CR5
Write CR6	P	0	1	1	0	0	1	X	see CR6 TABLE 8
Read-back CR6	P	0	1	1	0	1	1	X	see CR6
Write CR7	P	0	1	1	1	0	1	X	see CR7 TABLE 9
Read-back CR7	P	0	1	1	1	1	1	X	see CR7
Write CR8	P	1	0	0	0	0	1	X	see CR8 TABLE 10
Read-back CR8	P	1	0	0	0	1	1	X	see CR8
Write CR9	P	1	0	0	1	0	1	X	see CR9 TABLE 11
Read-back CR9	P	1	0	0	1	1	1	X	see CR9
Write Test Register CR10	P	1	0	1	0	0	1	X	reserved

NOTE 1: bit 7 of the address byte and data byte is always the first bit clocked into or out from: CI and CO pins when MICROWIRE serial port is enabled, or into and out from D_R and D_X pins when GCI mode selected.
X = reserved: write 0

NOTE 2: "P" bit is Power up/down Control bit. P = 1 Means Power Down.
Bit 1 indicates, if set, the presence of a second byte.

NOTE 3: Bit 2 is write/read select bit.

Table 2: Control Register CR0 Functions

7	6	5	4	3	2	1	0	Function		
F1	F0	MA	IA	DN	FF	B7	DL			
0	0							MCLK = 512 kHz		(1)
0	1							MCLK = 1.536 MHz	*	
1	0							MCLK = 2.048 MHz		
1	1							MCLK = 2.560 MHz		(1)
		0	X					Select MU-255 law	*	
		1	0					A-law including even bit inversion		
		1	1					A-law; No bit inversion		
				0				Delayed data timing	*	(1)
				1				Non delayed data timing		(1)
					0			B1 and B2 consecutive	*	(1)
					1			B1 and B2 separated		(1)
						0		8 bits time-slot	*	
						1		7 bits time-slot		
							0	Normal operation	*	
							1	Digital Loop-back		

*: state at power on initialization

(1): significant in COMBO I/II mode only

Table 3: Control Register CR1 Functions

7	6	5	4	3	2	1	0	Function		
HFE	ALE	DO	MR	MX	EN	T1	T0			
0								HFO / HFI pins disabled	*	
1								HFO / HFi pins enabled		
	0							Anti-larsen disabled	*	
	1							Anti-larsen enabled		
		0						L0 latch is put in high impedance	*	
		1						L0 latch set to 0		
			0					D_R connected to rec. path	*	(1)
			1					CR2 connected to rec. path		(1)
				0				Trans path connected to D_X	*	(1)
				1				CR3 connected to D_X		(1)
					0			voice data transfer disable	*	
					1			voice data transfer enable		
						0	0	B1 channel selected	*	
						0	1	B2 channel selected		
						1	0	B1* channel selected		(2)
						1	1	B2* channel selected		(2)

*: state at power on initialization

(1): significant in COMBO I / II mode only

(2): significant in GCI mode only.

Table 4: Control Register CR2 Functions

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb							lsb	Data sent to Receive path or Data received from D_R input

Table 5: Control Registers CR3 Functions

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb							lsb	D_X data transmitted

Table 6: Control Register CR4 Functions

7	6	5	4	3	2	1	0	Function	
VS	TE	SI	EE	RTL	RTE	SL	SE		
0 1								MIC1 selected MIC2 selected	*
	0 1							Transmit input muted Transmit input enabled	*
		0 1						Internal sidetone disabled Internal sidetone enabled	*
			0 1					EAIN disconnected EAIN selected to Loudspeaker	*
				0 0 1 1	0 1 0 1			Ring / Tone muted Ring / Tone to Earpiece Ring / Tone to Loudspeaker Ring / Tone to Earpiece and Loudspeaker	*
						0 0 1 1	0 1 0 1	Receive signal muted Receive signal connected to earpiece amplifer Receive signal connected to loudspeaker amplifier Receive signal connected to loudspeaker and earpiece amplifier	*

*: state at power on initialization

Table 7: Control Register CR5 Functions

7	6	5	4	3	2	1	0	Function
Transmit amplifier				Sidetone amplifier				
0	0	0	0					0 dB gain *
0	0	0	1					1 dB gain
-	-	-	-					in 1 dB step
1	1	1	1					15 dB gain
				0	0	0	0	-12.5 dB gain *
				0	0	0	1	-13.5 dB gain
				-	-	-	-	in 1 dB step
				1	1	1	1	-27.5 dB gain

*: state at power on initialization

Table 8: Control Register CR6 Functions

7	6	5	4	3	2	1	0	Function
Earpiece amplfier				Loudspeaker				
0	0	0	0					0 dB gain *
0	0	0	1					-1 dB gain
-	-	-	-					in 1 dB step
1	1	1	1					-15 dB gain
				0	0	0	0	0 dB gain *
				0	0	0	1	-2 dB gain
				-	-	-	-	in 2 dB step
				1	1	1	1	-30 dB gain

*: state at power on initialization

Table 9: Control Register CR7 Functions

7	6	5	4	3	2	1	0	Function		
Tone gain				F1	F2	SN	DE	Attenuation	f1 V_{pp}	f2 V_{pp}
0	0	0	0					0 dB *	2.4 (1)	1.9 (1)
0	0	0	1					-3 dB	1.70	1.34
0	0	1	0					-6 dB	1.20	0.95
0	0	1	1					- 9 dB	0.85	0.67
0	1	0	0					-12 dB	0.60	0.47
0	1	0	1					-15 dB	0.43	0.34
0	1	1	0					-18 dB	0.30	0.24
0	1	1	1					-21 dB	0.21	0.17
1	X	X	0					-24 dB	0.15	0.12
1	X	X	1					-27 dB	0.10	0.08
				0	0			f1 and f2 muted		*
				0	1			f2 selected		
				1	0			f1 selected		
				1	1			f1 and f2 in summed mode		
						0		Squarewave signal selected		*
						1		Sinewave signal selected		
							0	Normal operation		*
							1	Tone / Ring Generator connected to Transmit path		

*: state at power on initialization

(1): value provided if f1 or f2 is selected alone.
If f1 and f2 are selected in the summed mode, f1=1.34 V_{pp} while f2=1.06 V_{pp}.
Output generator is 2.4 V_{pp}

X reserved: write 0

Table 10: Control Register CR8 Functions

7	6	5	4	3	2	1	0	Function
f17	f16	f15	f14	f13	f12	f11	f10	
msb							lsb	Binary equivalent of the decimal number used to calculate f1

Table 11: Control Register CR9 Functions

7	6	5	4	3	2	1	0	Function
f27	f26	f25	f24	f23	f22	f21	f20	
msb							lsb	Binary equivalent of the decimal number used to calculate f2

CONTROL REGISTER CR0

First byte of a READ or a WRITE instruction to Control Register CR0 is as shown in TABLE 1. Second byte is as shown in TABLE 2.

Master Clock Frequency Selection

A master clock must be provided to PIAFE for operation of filter and coding/decoding functions.
In COMBO I/II mode, MCLK frequency can be either 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz.
Bit F1 (7) and F0 (6) must be set during initialization to select the correct internal divider.
In GCI mode, MCLK must be either 1.536MHz or 2.048MHz.
512KHz and 2.56MHz are not allowed.
Default value is 1.536 MHz for both modes.
Any clock different from the default one must be selected prior a Power-Up instruction for both modes.

Coding Law Selection

Bits MA (5) and IA (4) permit selection of Mu-255 law or A law coding with or without even bit inversion.
After power on initialization, the Mu-255 law is selected.

	Mu 255 law								True A law even bit inversion								A law without even bit inversion							
	msb							lsb	msb							lsb	msb							lsb
Vin = + full scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1
Vin = 0 V	1 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 0	1 1	0 0	1 1	0 0	1 1	0 0	1 1	1 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
Vin = - full scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	1	1	1	1	1

MSB is always the first PCM bit shifted in or out of PIAFE.

Digital Interface timing

Bit DN=0 (3) selects digital interface in delayed timing mode while DN=1 selects non delayed data timing.
In GCI mode, bit DN is not significant.
After reset and if COMBO I/II mode is selected, delayed data timing is selected.

Digital Interface format

Bit FF=0 (2) selects digital interface in Format 1 where B1 and B2 channel are consecutive. FF=1 selects Format 2 where B1 and B2 channel are separated by two bits. (see digital interface format section).
In GCI mode, bit FF is not significant.

56+8 selection

Bit 'B7' (1) selects capability for PIAFE to take into account only the seven most significant bits of the PCM data byte selected.
When 'B7' is set, the LSB bit on D_R is ignored and LSB bit on D_X is high impedance. This function allows connection of an external "in band" data generator directly connected on the Digital Interface.

Digital loopback

Digital loopback mode is entered by setting DL bit(0) equal 1.
In Digital Loopback mode, data written into Receive PCM Data Register from the selected received time-slot is read-back from that Register in the selected transmit time-slot on D_X. Time slot is selected with Register CR1.
No PCM decoding or encoding takes place in this mode. Transmit and Receive amplifier stages are muted.

CONTROL REGISTER CR1

First byte of a READ or a WRITE instruction to Control Register CR1 is as shown in TABLE 1. Second byte is as shown in TABLE 3.

Hands-free I/Os selection

Bit HFE set to one enables HFI, HFO pins for connection of an external handfree circuit such as TEA 7540. HFO is an analog output that provides the receive voice signal. 0 dBMO level on that output is 0.491 Vrms ($1.4V_{pp}$). HFI is an analog high impedance input (10 KΩ typ.) intended to send back the processed receive signal to the Loudspeaker. 0 dBMO level on that input is 0.491Vrms.

Anti-larsen selection

Bit ALE set to one enables on-chip antilarsen and squelch effect system.

Latch output control

Bit DO controls directly logical status of latch output LO: ie, a "ZERO" written in bit DO puts output LO in high impedance, a "ONE" written in bit DO sets output LO to zero.

Microwire access to B channel on receive path
Bit MR (4) selects access from MICROWIRE Register CR2 to Receive path. When bit MR is set high, data written to register CR2 is decoded each frame, sent to the receive path and data input at D_R is ignored.
In the other direction, current PCM data input received at D_R can be read from register CR2 each frame.

Microwire access to B channel on transmit path
Bit MX (3) selects access from MICROWIRE write only Register CR3 to D_X output. When bit MX is set high, data written to CR3 is output at D_X every frame and the output of PCM encoder is ignored.

B channel selection
Bit 'EN' (2) enables or disables voice data transfer on D_X and D_R pins. When disabled, PCM data from DR is not decoded and PCM time-slots are high impedance on D_X.
In GCI mode, bits 'T1' (1) and 'T0' (0) select one of the four channels of the GCI interface.
In COMBO I/II mode, only B1 or B2 channel can be selected according to the interface format selected. Bit 'T1' is ignored.

CONTROL REGISTER CR2
Data sent to receive path or data received from D_R input. Refer to bit MR(4) in "Control Register CR1" paragraph.

CONTROL REGISTER CR3
D_X data transmitted. Refer to bit MX(3) in "Control Rgister CR1" paragraph.

CONTROL REGISTER CR4
First byte of a READ or a WRITE instruction to Control Register CR4 is as shown in TABLE 1. Second byte is as shown in TABLE 6.

Transmit Input Selection
MIC1 or MIC2 source is selected with bit VS (7).
Transmit input selected can be enabled or muted with bit TE (6).
Transmit gain can be adjusted within a 15 dB range in 1 dB step with Register CR5.

Sidetone select
Bit "SI" (5) enables or disables Sidetone circuitry. When enabled, sidetone gain can be adjusted with Register (CR5). When Transmit path is disabled, bit TE set low, sidetone circuit is also disabled.

External Auxiliary signal select
Bit "EE" (4) set to one connects EAIN input to the loudspeaker amplifier input.

Ring/Tone signal routing
Bits "RTL" (3) and RTE (2) provide select capability to connect on-chip Ring/Tone generator either to loudspeaker amplifier input or to earpiece amplifier input or both.

PCM receive data routing
Bits "SL" (1) and "SE" (0) provide select capability to connect received speech signal either to Loudspeaker amplifier input or to earpiece amplifier input or both.

CONTROL REGISTER CR5
First byte of a READ or a WRITE instuction to Control Register CR5 is as shown in TABLE 1. Second byte is as shown in TABLE 7.

Transmit gain selection
Transmit amplifier can be programmed for a gain from 0dB to 15dB in 1dB step with bits 4 to 7.
0 dBmO level at the output of the transmit amplifier (A reference point) is 0.739 Vrms (overload voltage is 1.06 Vrms).

Sidetone attenuation selection
Transmit signal picked up after the switched capacitor low pass filter may be fed back into the Receive Earpiece amplifier.
Attenuation of the signal at the output of the sidetone attenuator can be programmed from –12.5dB to -27.5dB relative to reference point A in 1 dB step with bits 0 to 3.

CONTROL REGISTER CR6
First byte of a READ or a WRITE instruction to Control Register CR6 is as shown in TABLE 1. Second byte is as shown in TABLE 8.

Earpiece amplifier gain selection:
Earpiece Receive gain can be programmed in 1 dB step from 0 dB to -15 dB relative to the maximum with bits 4 to 7.
0 dBmO voltage at the output of the amplifier on pins V_{Fr+} and V_{Fr-} is then 824.5 mVrms when 0dB gain is selected down to 146.6 mVrms when –15 dB gain is selected.

Loudspeaker amplifier gain selection:
Loudspeaker Receive amplifier gain can be programmed in 2 dB step from 0 dB to -30 dB relative to the maximum with bits 0 to 3.
0 dBmO voltage on the output of the amplifier on pins LS+ and LS- on 50 Ω is then 1.384 Vrms ($3.91V_{pp}$) when 0 dB gain is selected down to 43.7 mVrms ($123.6mV_{pp}$) when -30 dB gain is selected.

Current limitation is approximatively 150 mApk.

CONTROL REGISTER CR7:
First byte of a READ or a WRITE instruction to Control Register CR7 is as shown in TABLE 1. Second byte is as shown in TABLE 9.

Tone/Ring amplifier gain selection
Output level of Ring/Tone generator, before attenuation by programmable attenuator is 2.4 Vpk-pk when f1 generator is selected alone or summed with the f2 generator and 1.9 Vpk-pk when f2 generator is selected alone.
Selected output level can be attenuated down to -27 dB by programmable attenutator by setting bits 4 to 7.

Frequency mode selection
Bits 'F1' (3) and 'F2' (2) permit selection of f1 and/or f2 frequency generator according to TABLE 9.
When f1 (or f2) is selected, output of the Ring/Tone is a squarewave (or a sinewave) signal at the frequency selected in the CR8 (or CR9) Register.
When f1 and f2 are selected in summed mode, output of the Ring/Tone generator is a signal where f1 and f2 frequency are summed.
In order to meet DTMF specifications, f2 output level is attenuated by 2dB relative to the f1 output level.
Frequency temporization must be controlled by the microcontroller.

Waveform selection
Bit 'SN' (1) selects waveform of the output of the Ring/Tone generator. Sinewave or squarewave signal can be selected.

DTMF selection
Bit DE (0) permits connection of Ring/Tone/DTMF generator on the Transmit Data path instead of the Transmit Amplifier output. Earpiece feed-back may be provided by sidetone circuitry by setting bit SI or directly by setting bit RTE in Register CR4. Loudspeaker feed-back may be provided directly by setting bit RTL in Register CR4.

CONTROL REGISTERS CR8 AND CR9
First byte of a READ or a WRITE instruction to Control Register CR8 or CR9 is as shown in TABLE 1. Second byte is respectively as shown in TABLE 10 and 11.
Tone or Ring signal frequency value is defined by the formula:

$f1 = CR8 / 0.128\ Hz$

and

$f2 = CR9 / 0.128\ Hz$

where CR8 and CR9 are decimal equivalents of the binary values of the CR8 and CR9 registers respectively. Thus, any frequency between 7.8 Hz and 1992 Hz may be selected in 7.8 Hz step.
TABLE 12 gives examples for the main frequencies usual for Tone or Ring generation.

Table 12: Examples of Usual Frequency Selection

Description	f1 value (decimal)	Theoric value (Hz)	Typical value (Hz)	Error %
Tone 250 Hz	32	250	250	.00
Tone 330 Hz	42	330	328.2	−.56
Tone 425 Hz	54	425	421.9	−.73
Tone 440 Hz	56	440	437.5	−.56
Tone 800 Hz	102	800	796.9	−.39
Tone 1330 Hz	170	1330	1328.1	−.14
DTMF 697 Hz	89	697	695.3	−.24
DTMF 770 Hz	99	770	773.4	+.44
DTMF 852 Hz	109	852	851.6	−.05
DTMF 941 Hz	120	941	937.5	−.37
DTMF 1209 Hz	155	1209	1210.9	+.16
DTMF 1336 Hz	171	1336	1335.9	−.01
DTMF 1477 Hz	189	1477	1476.6	.00
DTMF 1633 Hz	209	1633	1632.8	.00
SOL	50	392	390.6	−.30
LA	56	440	437.5	−.56
SI	63	494	492.2	−.34
DO	67	523.25	523.5	+.04
RE	75	587.33	586.0	−.23
MI flat	80	622.25	625.0	+.45
MI	84	659.25	656.3	−.45
FA	89	698.5	695.3	−.45
FA sharp	95	740	742.2	+.30
SOL	100	784	781.3	−.34
SOL sharp	106	830.6	828.2	−.29
LA	113	880	882.9	+.33
SI	126	987.8	984.4	−.34
DO	134	1046.5	1046.9	+.04
RE	150	1174.66	1171.9	−.23
MI	169	1318.5	1320.4	+.14

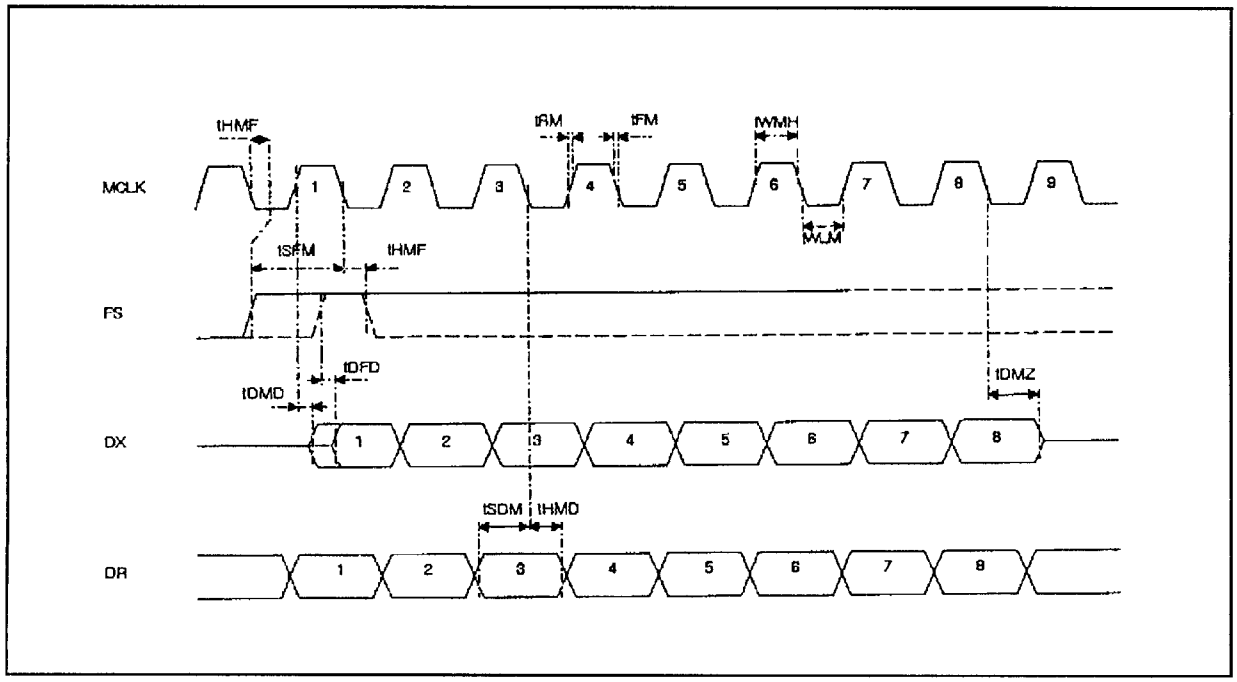
POWER SUPPLIES

While pins of PIAFE device are well protected against electrical misuse, it is recommended that the standard CMOS practise of applying GND before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

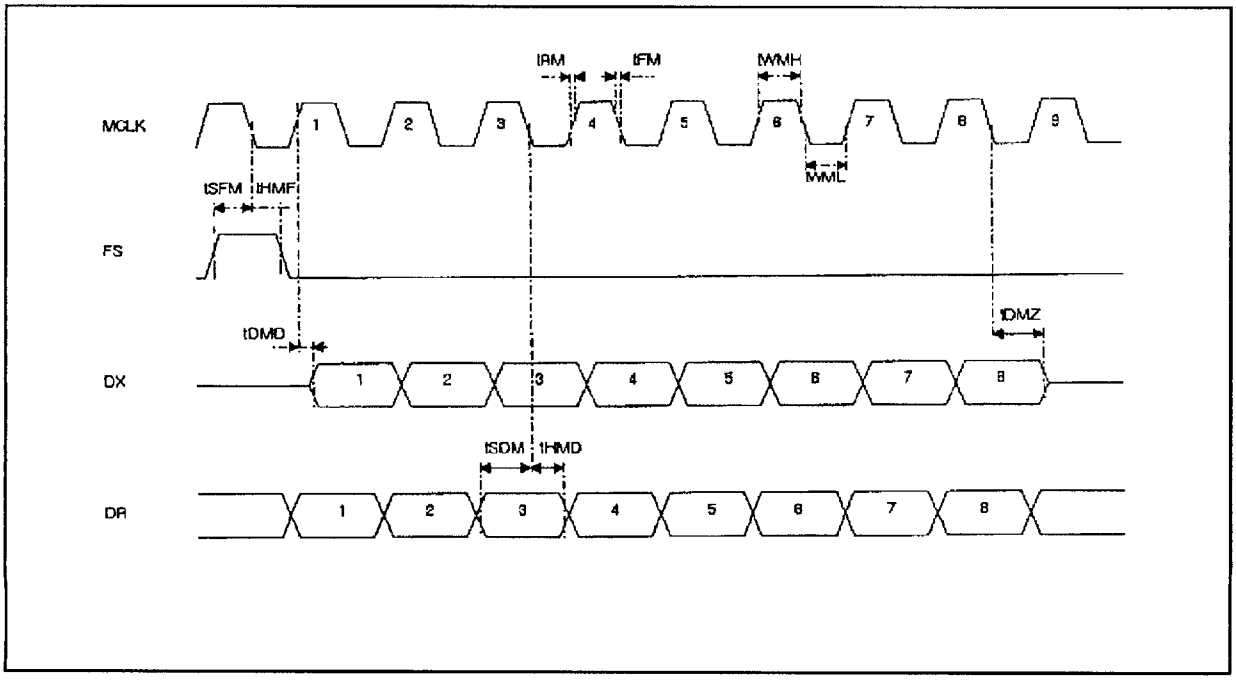
To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A power supply decoupling capacitor of 0.1 µF should be connected from this common point to V_{CC} as close as possible to the device pins.

TIMING DIAGRAM

Non Delayed Data Timing Mode

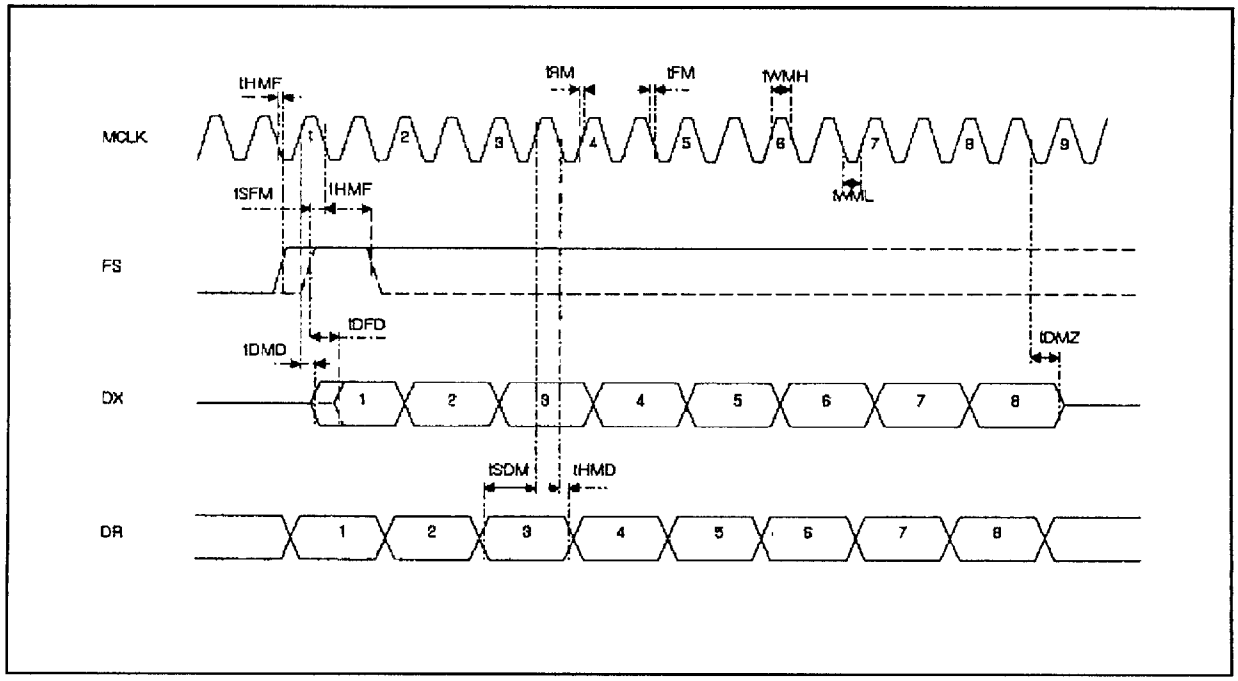


Delayed Data Timing Mode

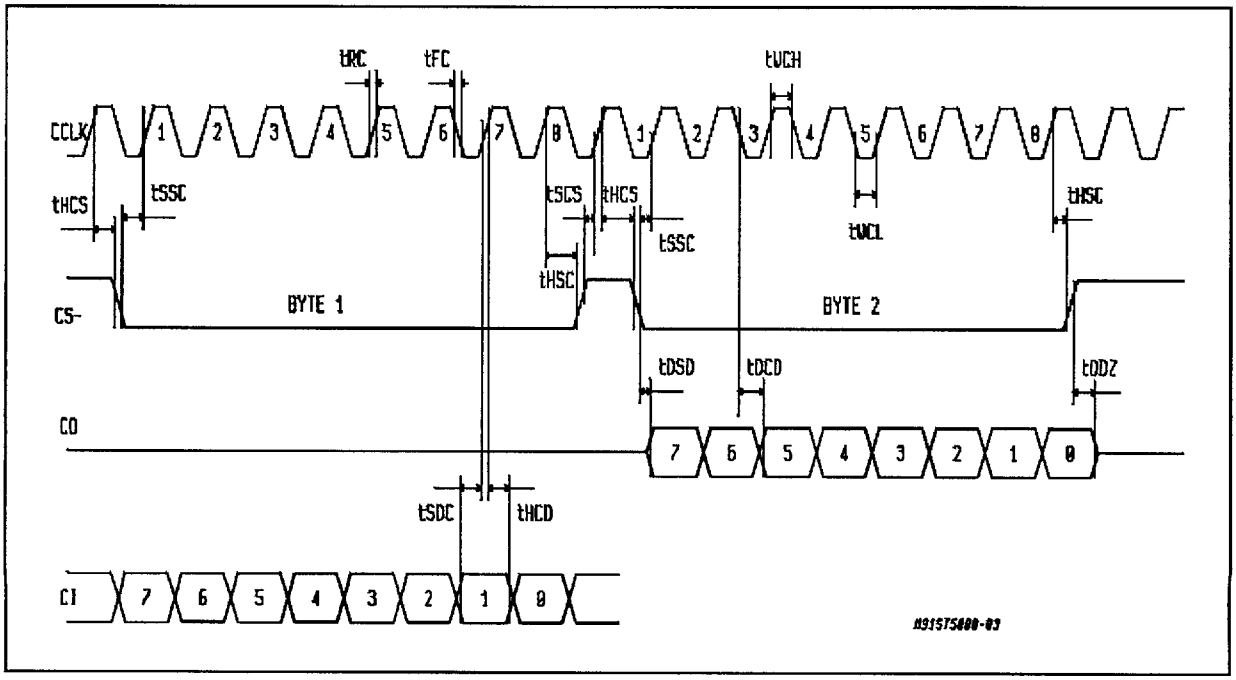


TIMING DIAGRAM (continued)

GCI Timing Mode



Serial Control Timing (MICROWIRE MODE)



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
V_{CC} to GND	7	V
Current at V_{MIC} ($V_{CC} \leq 5.5V$)	±50	mA
Current at V_{RxO} and LS	± 100	mA
Current at any digital output	± 50	mA
Voltage at any digital input ($V_{CC} \leq 5.5V$); limited at ± 50mA	V_{CC} + 1 to GND - 1	V
Storage temperature range	- 65 to + 150	°C
Lead Temperature (wave soldering, 10s)	+ 260	°C

TIMING SPECIFICATIONS (unless otherwise specified, $V_{CC} = 5V \pm 10\%$, $T_A = -25°C$ to $85°C$; typical characteristics are specified $V_{CC} = 5V$, $T_A = 25°C$; all signals are referenced to GND, see Note 5 for timing definitions)

MASTER CLOCK TIMING

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{MCLK}	Frequency of MCLK	Selection of frequency is programmable (see table 2)		512 1.536 2.048 2.560		kHz MHz MHz MHz
t_{WMH}	Period of MCLK high	Measured from V_{IH} to V_{IH}	80			ns
t_{WML}	Period of MCLK low	Measured from V_{IL} to V_{IL}	80			ns
t_{RM}	Rise Time of MCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK	Measured from V_{IH} to V_{IL}			30	ns

PCM INTERFACE TIMING (COMBO I / II and GCI modes)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{HMF}	Hold Time MCLK low to FS low		10			ns
t_{SFM}	Setup Time, FS high to MCLK low		30			ns
t_{DMD}	Delay Time, MCLK high to data valid	Load = 100 pf			100	ns
t_{DMZ}	Delay Time, MCLK low to DX disabled		15		100	ns
t_{DFD}	Delay Time, FS high to data valid	Load = 100 pf; Applies only if FS rises later than MCLK rising edge in Non Delayed Mode only			100	ns
t_{SDM}	Setup Time, D_R valid to MCLK receive edge		20			ns
t_{HMD}	Hold Time, MCLK low to D_R invalid		20			ns

SERIAL CONTROL PORT TIMING (Usual COMBO I / II mode only)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{CCLK}	Frequency of CCLK				2.048	MHz
t_{WCH}	Period of CCLK high	Measured from V_{IH} to V_{IH}	160			ns
t_{WCL}	Period of CCLK low	Measured from V_{IL} to V_{IL}	160			ns
t_{RC}	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			50	ns
t_{HCS}	Hold Time, CCLK high to CS– low		10			ns
t_{SSC}	Setup Time, CS– low to CCLK high		50			ns
t_{SDC}	Setup Time, CI valid to CCLK high		50			ns
t_{HCD}	Hold Time, CCLK high to CI invalid		50			ns
t_{DCD}	Delay Time, CCLK low to CO data valid	Load = 100 pF , plus 1 LSTTL load			80	ns
t_{DSD}	Delay Time, CS–low to CO data valid				50	ns
t_{DDZ}	Delay Time CS–high or 8th CCLK low to CO high impedance whichever comes first		15		80	ns
t_{HSC}	Hold Time, 8th CCLK high to CS– high		100			ns
t_{SCS}	Set up Time, CS– high to CCLK high		100			ns

Note 5: A signal is valid if it is above V_{IH} or below V_{IL} and invalid if it is between V_{IL} and V_{IH}.
For the purpoes of this specification the following conditions apply:
a) All input signal are defined as: V_{IL} = 0.4V, V_{IH} = 2.7V, t_R < 10ns, t_F < 10ns.
b) Delay times are measured from the inputs signal valid to the output signal valid.
c) Setup times are measured from the data input valid to the clock input invalid.
d) Hold times are measured from the clock signal valid to the data input invalid.

ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{CC} = 5V ± 10%, T_A = –25°C to 85°C ; typical characteristic are specified at V_{CC} = 5V, T_A = 25°C ; all signals are referenced to GND)

DIGITAL INTERFACES

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All digital inputs	DC			0.7	V
			AC			0.4	V
V_{IH}	Input High Voltage	All digital inputs	DC	2.0			V
			AC	2.7			V
V_{OL}	Output Low Voltage	D_X,I_L = -2.0mA; all other digital outputs, I_L = –1mA	DC			0.4	V
			AC			0.7	V
V_{OH}	Output High Voltage	D_X,I_L = 2.0mA; all other digital outputs, I_L = 1mA	DC	2.4			V
			AC	2.0			V
I_{IL}	Input Low Current	Any digital input, GND < V_{IN} < V_{IL}		-10		10	µA
I_{IH}	Input High Current	Any digital input, V_{IH} < V_{IN} < V_{CC}		-10		10	µA
I_{OZ}	Output Current in High impedance (Tri-state)	D_X and CO		-10		10	µA

ANALOG INTERFACES

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{MIC}	Input Leakage	GND < V_{MIC} < V_{CC}	-100		+100	µA
R_{MIC}	Input Resistance	GND < V_{MIC} < V_{CC}	50			kΩ
R_{LVFr}	Load Resistance	V_{Fr+} to V_{Fr-}	100			Ω
C_{LVFr}	Load Capacitance	V_{Fr+} to V_{Fr-}			150	nF
R_{OVFr0}	Output Resistance	Steady zero PCM code applied to DR; I = ± 1mA		1.0		Ω
V_{OSVFr0}	Differential offset: Voltage at V_{Fr+}, V_{Fr-}	Alternating ± zero PCM code applied to DR maximum receive gain; R_L = 100Ω	-100		+100	mV
R_{LLS}	Load Resistance	L_{S+} to L_{S-}		50		Ω
C_{LLS}	Load Capacitance	L_{S+} to L_{S-}			600	nF
R_{OLS}	Output Resistance	Steady zero PCM code applied to DR; I ± 1mA		1		Ω
V_{OSLS}	Differential offset Voltage at L_{S+}, L_{S-}	Alternating ± zero PCM code applied to DR maximum receive gain; R_L = 50Ω	–100		+100	mV

POWER DISSIPATION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CC0}	Power down Current	CCLK,CI = 0.4V; CS = 2.4V (µwire only) All other inputs active GCI mode only:		0.2 0.2	0.5 0.5	mA mA
I_{CC1}	Power Up Current	L_{S+}, L_{S-} and V_{Fr+}, V_{Fr-} not loaded		12.0	17.0	mA

TRANSMISSION CHARACTERISTICS (unless otherwise specified, V_{CC} = 5V ± 10%, T_A = –25°C to 85°C; typical characteristics are specified at V_{CC} = 5V, T_A = 25°C, MIC1/2 = 0dB_{m0}, D_R = 0dB_{m0} PCM code, f = 1015.625 Hz; all signal are referenced to GND)

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Transmit path - Absolute levels at MIC1 / MIC2

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Transmit Amps connected for 0dB gain		73.9		mV_{RMS}
Overload level	A law selected		106.08		mV_{RMS}
Overload level	mu law selected		106.47		mV_{RMS}
0 dBM0 level	Transmit Amps connected for 15dB gain		13.14		mV_{RMS}
Overload level	A law selected		18.86		mV_{RMS}
Overload level	mu law selected		18.93		mV_{RMS}

TRANSMISSION CHARACTERISTICS (continued)

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Receive path - Absolute levels at V_{FR} (Differentially measured)

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Receive Amp programmed for 0dB gain		824.5		mV_{RMS}
0 dBM0 level	Receive Amp programmed for - 15dB attenuation		146.6		mV_{RMS}

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Receive path - Absolute levels at L_S (Differentially measured)

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Receive Amp programmed for 0dB gain		1.384		V_{RMS}
0 dBM0 level	Receive Amp programmed for - 30dB gain		43.7		mV_{RMS}

AMPLITUDE RESPONSE
Transmit path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for maximum. Measure deviation of Digital PCM Code from ideal $0dB_{m0}$ PCM code at D_X	-0.30		0.30	dB
G_{XAG}	Transmit Gain Variation with programmed gain	Measure Transmit Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GXA, i.e. $G_{AXG} = G_{actual} - G_{prog.} - G_{XA}$	-0.5		0.5	dB
G_{XAT}	Transmit Gain Variation with temperature	Measured relative to G_{XA}. min. gain < G_X < Max. gain	-0.1		0.1	dB
G_{XAV}	Transmit Gain Variation with supply	Measured relative to G_{XA} G_X = Maximum gain	-0.1		0.1	dB
G_{XAF}	Transmit Gain Variation with frequency	Relative to 1015,625 Hz, multitone test technique used. min. gain < G_X < Max. gain				
		f = 60 Hz			-26	dB
		f = 200 Hz	-1.5		-0.1	dB
		f = 300 Hz to 3000 Hz	-0.3		0.3	dB
		f = 3400 Hz	-0.8		0.0	dB
		f = 4000 Hz			-14	dB
		f = 4600 Hz (*)			-35	dB
		f = 5000 Hz to 6000 Hz			-40	dB
		f = 8000 Hz (*)			-47	dB
		f > 8000 Hz			-40	dB
G_{XAL}	Transmit Gain Variation with signal level	Sinusoidal Test method. Reference Level = $-10\ dB_{m0}$				
		$V_{MIC} = -40\ dB_{m0}$ to $+3\ dB_{m0}$	-0.25		0.25	dB
		$V_{MIC} = -50\ dB_{m0}$ to $-40\ dB_{m0}$	-0.5		0.5	dB
		$V_{MIC} = -55\ dB_{m0}$ to $-50\ dB_{m0}$	-1.2		1.2	dB

(*) The limit at frequencies between 4600Hz and 8000Hz lies on a stright line connecting the two frequencies on a linear (dB) scale versus log (Hz) scale.

AMPLITUDE RESPONSE
Receive path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{RAE}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply 0 dB_{m0} PCM code to D_R Measure $V_{Fr\pm}$	-0.3		0.3	dB
G_{RAL}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply 0 dB_{m0} PCM code to D_R Measure $L_{S\pm}$	-0.6		0.6	dB
G_{RAGE}	Receive Gain Variation with programmed gain	Measure Earpiece Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GRAE, i.e. $G_{RAGE} = G_{actual} - G_{prog.} - G_{RAE}$	-0.5		0.5	dB
G_{RAGL}	Receive Gain Variation with programmed gain	Measure Loudspeaker Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GRAL, i.e. $G_{RAGL} = G_{actual} - G_{prog.} - G_{RAL}$	-1.0		1.0	dB
G_{RAT}	Receive Gain Variation with temperature	Measured relative to GRA. (LS and V_{Fr}) G_R = Maximum Gain	-0.1		0.1	dB
G_{RAV}	Receive Gain Variation with Supply	Measured relative to GRA. (LS and V_{Fr}) G_R = Maximum Gain	-0.1		0.1	dB
G_{RAF}	Receive Gain Variation with frequency (Earpiece or Loudspeaker)	Relative to 1015,625 Hz, multitone test technique used. min. gain < G_R < Max. gain f = 200 Hz f = 300 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz	 -0.3 -0.3 -0.8		 0.3 0.3 0.0 -14	 dB dB dB dB
$G_{RAL\ E}$	Receive Gain Variation with signal level (Earpiece)	Sinusoidal Test Method Reference Level = –10 dBm0 D_R = 0 dBm0 to +3 dBm0 D_R = -40 dBm0 to 0 dBm0 D_R = -50 dBm0 to -40 dBm0 D_R = -55 dBm0 to -50 dBm0	 -0.25 -0.25 -0.5 -1.2		 0.25 0.25 0.5 1.2	 dB dB dB dB
$G_{RAL\ L}$	Receive Gain Variation with signal level (Loudspeaker)	Sinusoidal Test Method Reference Level = –10 dBm0 D_R = 0 dBm0 to +3 dBm0 D_R = -40 dBm0 to 0 dBm0 D_R = -50 dBm0 to -40 dBm0 D_R = -55 dBm0 to -50 dBm0	 -0.25 -0.25 -0,5 -1.2		 0.25 0.25 0.5 1.2	 dB dB dB dB

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DXA	Tx Delay, Absolute	f = 1600 Hz		320		µs
DXR	Tx Delay, Relative	f = 500 - 600 Hz f = 600 - 800 Hz f = 800 - 1000 Hz f = 1000 - 1600 Hz f = 1600 - 2600 Hz f = 2600 - 2800 Hz f = 2800 - 3000 Hz		225 125 50 20 55 80 130		µs µs µs µs µs µs µs
DRA	Rx Delay, Absolute	f = 1600 Hz		252		µs
DRR	Rx Delay, Relative	f = 500 - 1000 Hz f = 1000 - 1600 Hz f = 1600 - 2600 Hz f = 2600 - 2800 Hz f = 2800 - 3000 Hz		10 30 105 135 185		µs µs µs µs µs

NOISE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
NXC	Tx Noise, C weighted	V_{MIC} = 0V Max. Gain			16	dBrnC0
NXP	Tx Noise, P weighted	V_{MIC} = 0V Max. Gain			-70	dBm0p
NREC	Rx Noise, C weighted (Earpiece)	Receive PCM code = Alternating Positive and Negative Code Max. Gain			18	dBrnC0
NREP	Rx Noise, P weighted (Earpiece)	Receive PCM code = Positive Zero Max. Gain			-70	dBm0p
NRLC	Rx Noise, C weighted (Loudspeaker)	Receive PCM code = Alternating Positive and Negative code Max. Gain			21	dBrnC0
NRLP	Rx Noise, P weighted (Loudspeaker)	Receive PCM code = Positive Zero Max. Gain			-67	dBm0p
NRS	Noise, Single Frequency	V_{MIC} = 0V, Loop-around measurament from f = 0 Hz to 100 kHz			-50	dBm0
PPSRx	Positive PSRR, Tx	V_{MIC} = 0V, V_{CC} = 5.0 V_{DC} + 100 mV_{rms}; f = 0Hz to 50KHz	30			dB
PPSRp	Positive PSRR, Rx	PCM Code equals Positive Zero, V_{CC} = 5.0 VDC + 100 mVrms, measure $V_{Fr\pm}$ f = 0 Hz - 4 kHz f = 4 kHz - 50 kHz	30 30 30			dB dB dB
SOS	Spurious Out-Band signal at the output	DR input set to 0 dBm0 PCM code 300 - 3400 Hz Input PCM Code applied at DR 4600 Hz - 5600 Hz 5600 Hz - 7600 Hz 7600 Hz - 8400 Hz 8400 Hz - 100 kHz			 -40 -50 -50 -50	 dB dB dB dB

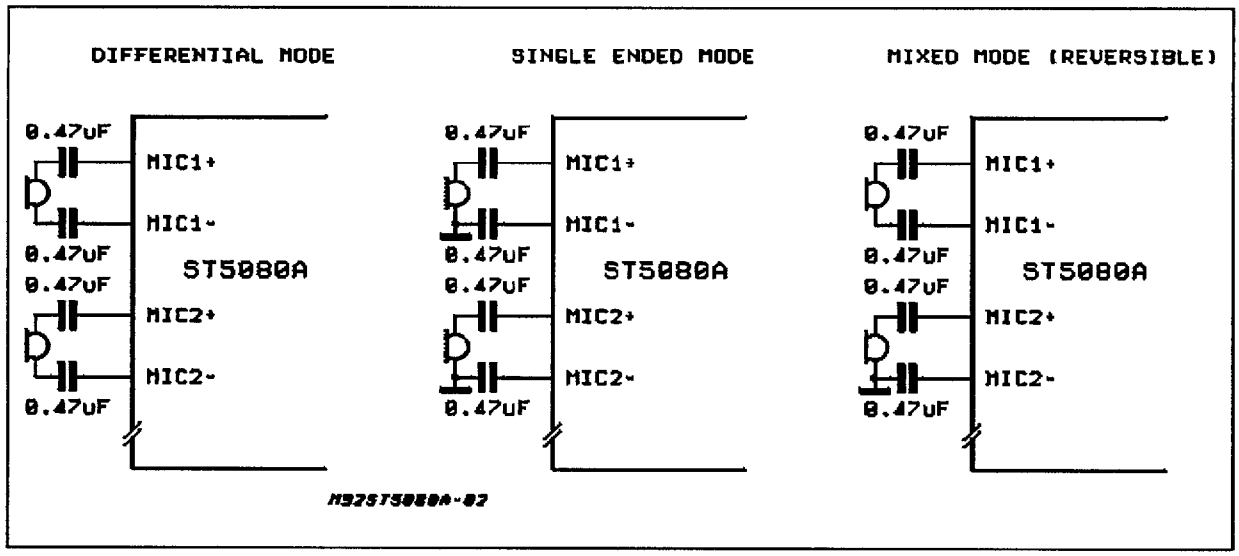
DISTORTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
S_{TDx} S_{TDr}	Signal to Total Distortion	Sinusoidal Test Methode (measured using C message weighting Filter) Level = 0 dBm0 to - 20 dBm0 Level = - 20 to -30 dBm0 Level = - 40 dBm0 Level = - 45 dBm0	 37 36 29 24			 dBC dBC dBC dBC
S_{DFx}	Single Frequency Distortion transmit	0 dBm0 input signal			-46	dB
S_{DFr}	Single Frequency Distortion receive	0 dBm0 input signal			-46	dB
IMD	Intermodulation	Loop-around measurament Voltage at V_{MIC} = -4 dBm0 to -21 dBm0, 2 Frequencies in the range 300 - 3400 Hz			-41	dB

CROSSTALK

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
C_{Tx-r}	Transmit to Receive	Transmit Level = 0 dBm0, f = 300 - 3400 Hz DR = QuietPCM Code			-65	dB
C_{Tr-x}	Receive to Transmit	Receive Level = 0 dBm0, f = 300 - 3400 Hz V_{MIC} = 0V			-65	dB

APPLICATION NOTE FOR MICROPHONE CONNECTIONS



The 4 connection modes (since the MIXED MODE is symmetrical with respect to MIC1 and MIC2) allow one microphone at a time to be selected via the V_S bit (bit 7 of Control Register CR4).

SO28 PACKAGE MECHANICAL DATA

DIM.	mm			Inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)