



## 3.2Gbps Compact SFP VCSEL Driver

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V<sub>CC</sub>) .....-0.5V to +5.0V  
 Voltage at TX\_DISABLE, IN+, IN-, MODSET,  
 PEAKSET, BIASSET, BIAS, BIASMON .....-0.5V to (V<sub>CC</sub> + 0.5V)  
 Voltage at OUT+, OUT- .....(V<sub>CC</sub> - 2V) to (V<sub>CC</sub> + 2V)  
 Current into OUT+, OUT- .....60mA

Continuous Power Dissipation (T<sub>A</sub> = +85°C)  
 16-Lead Thin QFN (derate 25mW/°C above +85°C) .....2W  
 Operating Temperature Range ..... -40°C to +85°C  
 Storage Temperature Range .....-55°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +2.97V to +3.63V, T<sub>A</sub> = -40°C to +85°C. Typical values are at V<sub>CC</sub> = +3.3V, T<sub>A</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I <sub>CC</sub>	TX_DISABLE set low, peaking is not used (Note 1)	I <sub>MOD</sub> = 2mA <sub>P-P</sub>	41		mA
			I <sub>MOD</sub> = 15mA <sub>P-P</sub>	51	65	
		Additional current when peaking is used (Note 2)			14	
	I <sub>CC-SHDW</sub>	Total current when TX_DISABLE is high		0.15	1	
<b>TX_DISABLE INPUT</b>						
Input Impedance			80	105		kΩ
Input High Voltage	V <sub>IH</sub>		2			V
Input Low Voltage	V <sub>IL</sub>				0.8	V
TX_DISABLE Time	t <sub>off</sub>	Time from rising edge of TX_DISABLE to I <sub>BIAS</sub> = I <sub>BIAS_OFF</sub> and I <sub>MOD</sub> = I <sub>MOD_OFF</sub> (Note 3)		0.2	3	μs
	t <sub>on</sub>	Time from falling edge of TX_DISABLE to I <sub>BIAS</sub> = 15mA and I <sub>MOD</sub> = 15mA <sub>P-P</sub>		111		
Input Leakage		V <sub>CC</sub> = 0V and V <sub>TX_DISABLE</sub> = 3.3V		25	40	μA
<b>BIAS GENERATOR (Note 4)</b>						
Bias Current	I <sub>BIAS</sub>	Min			1	mA
		Max	15			
Accuracy of Programmed Bias Current	ΔI <sub>BIAS</sub>		-8		+8	%
Bias Current During Disable	I <sub>BIAS_OFF</sub>	TX_DISABLE high			10	μA
BIASMON Gain			0.095	0.115	0.135	mA/mA
<b>LASER MODULATOR (Note 5)</b>						
Data Input Voltage Swing	V <sub>ID</sub>	Total differential signal	250		2200	mV <sub>P-P</sub>
Output Resistance	R <sub>OUT</sub>	Single-ended resistance at OUT+, OUT-		63	80	Ω
Modulation Current	I <sub>MOD</sub>	Min			2	mA <sub>P-P</sub>
		Max	15			

# 3.2Gbps Compact SFP VCSEL Driver

MAX3741

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +2.97V$  to  $+3.63V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ . Typical values are at  $V_{CC} = +3.3V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Programmable Peaking Current	$I_{PEAK}$	Min		0.2		mA
		Max		2		
Peaking Current Duration				80		ps
Tolerance of Programmed Modulation Current			-10		+10	%
Modulation Transition Time	$t_R, t_F$	$5mAP-P \leq I_{MOD} \leq 15mAP-P$ (Note 3)		65	95	ps
Deterministic Jitter	DJ	$5mAP-P \leq I_{MOD} \leq 15mAP-P$ (Notes 3, 6)		13	25	psp-P
Random Jitter	RJ	(Note 3)		1	4	psRMS
Laser Modulation During Disable	$I_{MOD\_OFF}$	Differential input voltage at 2200mVp-p		15	50	$\mu AP-P$
Differential Input Resistance			85	100	115	$\Omega$
Input Bias Voltage	$V_{IN}$			$V_{CC} - 0.3$		V

**Note 1:** Measured with  $R_{BIASSET} = 1.87k\Omega$  ( $I_{BIAS} \approx 15mA$ ). Supply current excludes  $I_{BIAS}$ .

**Note 2:** Tested with  $R_{PEAK} = 1.18k\Omega$ .

**Note 3:** Guaranteed by design and characterization.

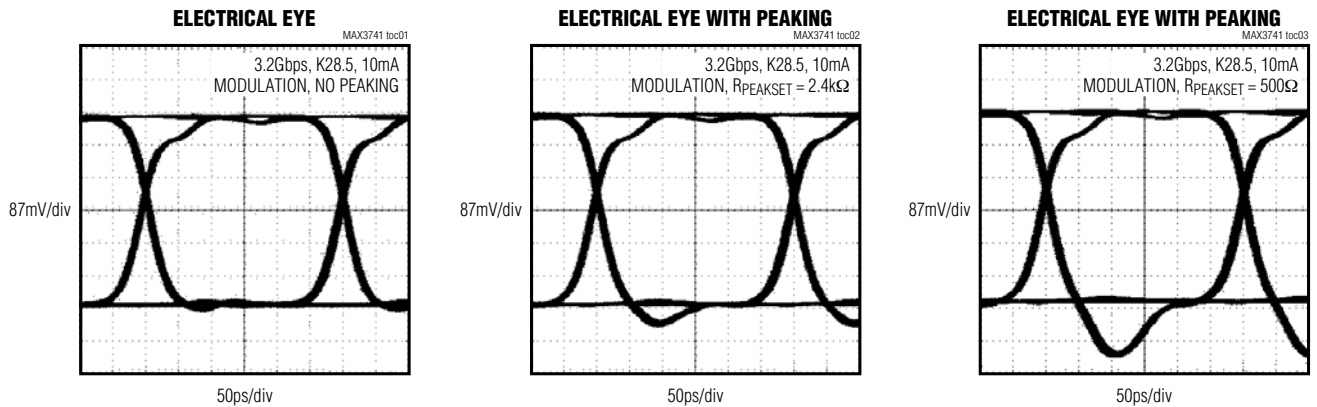
**Note 4:**  $V_{BIAS}$  is less than  $V_{CC} - 0.7V$ .

**Note 5:** Measured electrically with a  $50\Omega$  load AC-coupled to  $OUT+$ .

**Note 6:** Deterministic jitter is the peak-to-peak deviation from the ideal time crossings measured with a K28.5 bit pattern at 3.2Gbps (00111110101100000101).

## Typical Operating Characteristics

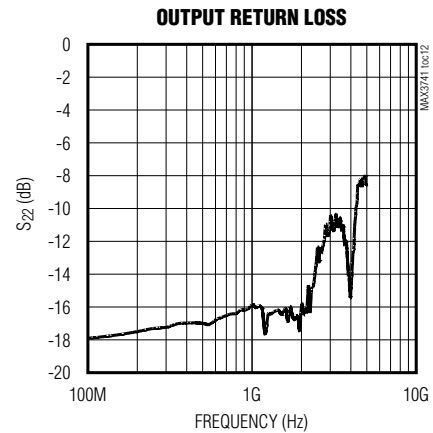
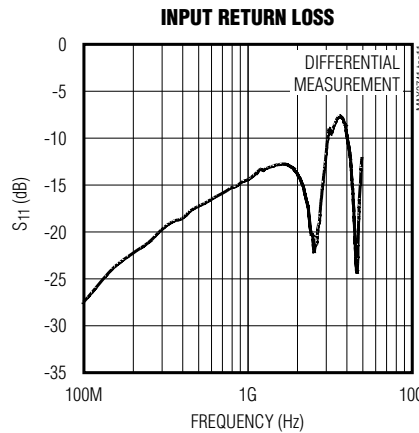
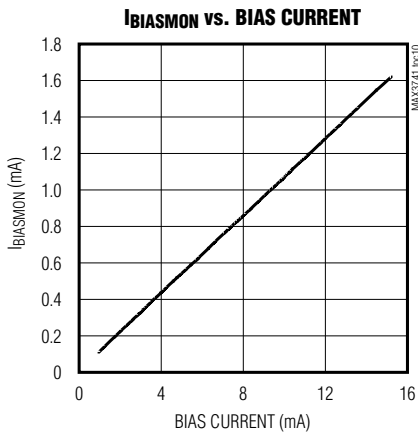
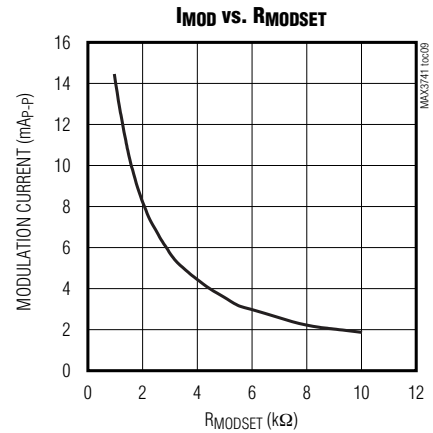
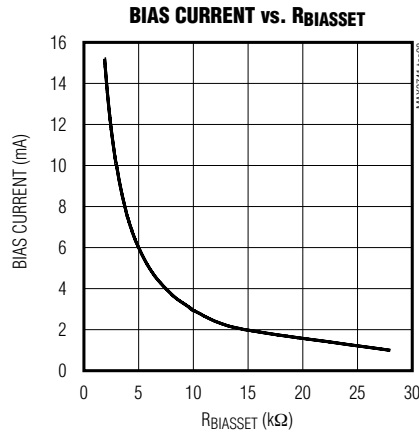
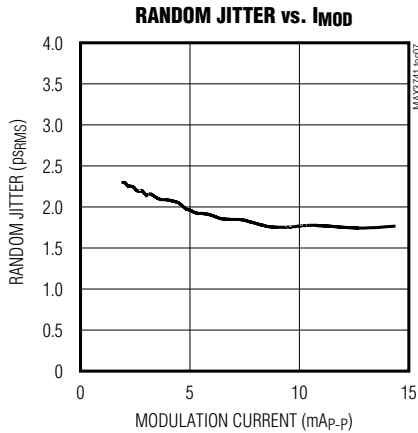
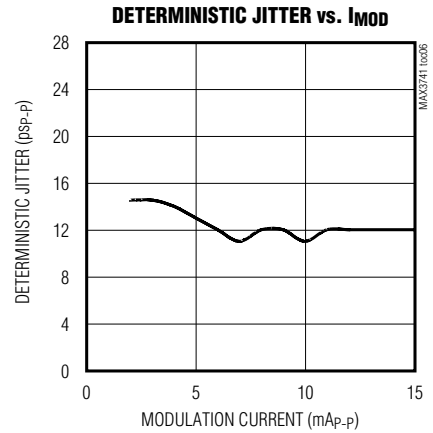
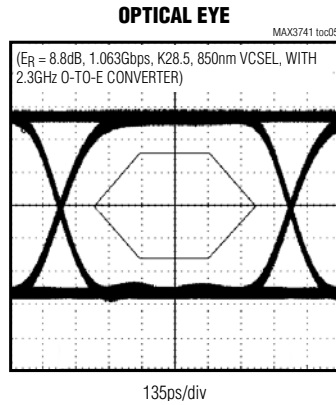
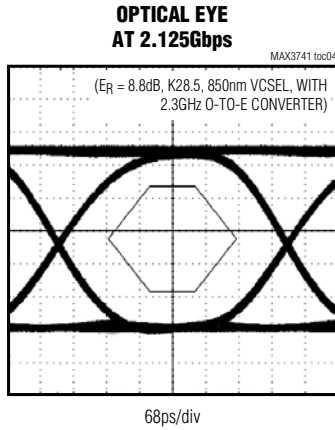
( $V_{CC} = +3.3V$ ,  $T_A = 25^{\circ}C$ , measured electrically with a  $50\Omega$  load AC-coupled to  $OUT+$ , unless otherwise noted.)



# 3.2Gbps Compact SFP VCSEL Driver

## Typical Operating Characteristics (continued)

( $V_{CC} = +3.3V$ ,  $T_A = 25^\circ C$ , measured electrically with a  $50\Omega$  load AC-coupled to OUT+, unless otherwise noted.)

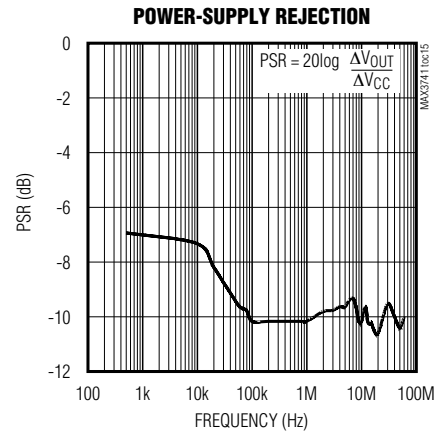
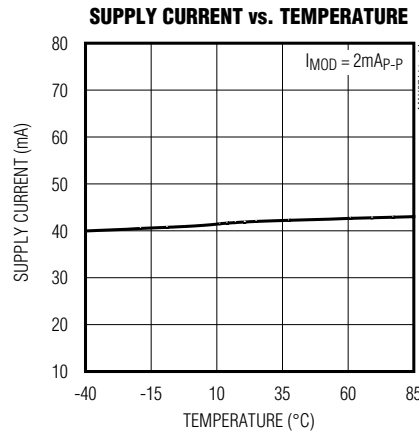
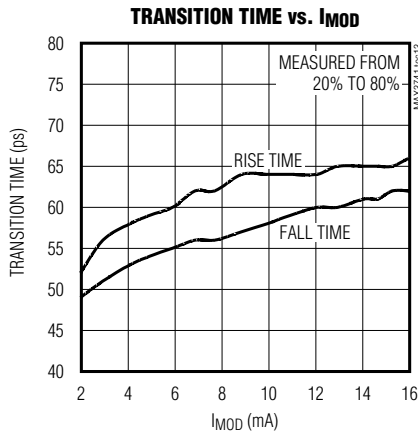


# 3.2Gbps Compact SFP VCSEL Driver

MAX3741

## Typical Operating Characteristics (continued)

( $V_{CC} = +3.3V$ ,  $T_A = 25^\circ C$ , measured electrically with a  $50\Omega$  load AC-coupled to OUT+, unless otherwise noted.)

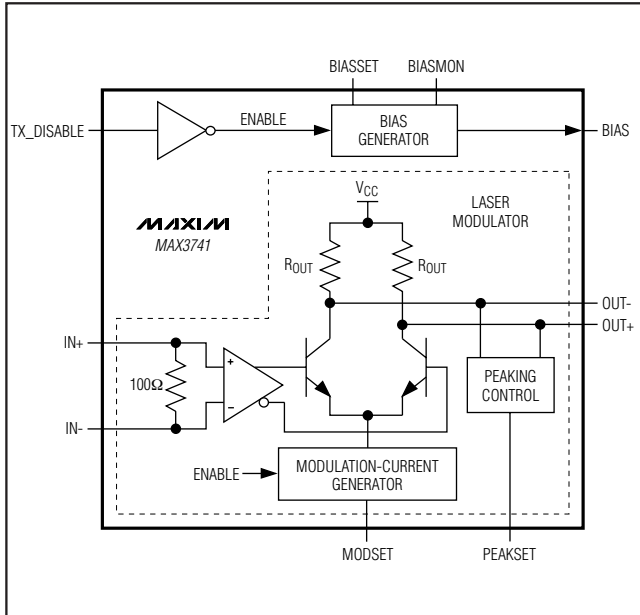


## Pin Description

PIN	NAME	FUNCTION
1	TX_DISABLE	Transmit Disable. Driver output is disabled when TX_DISABLE is high or left unconnected. The driver output is enabled when the pin is asserted low.
2	IN+	Noninverted Data Input
3	IN-	Inverted Data Input
4	N.C.	No Connection
5, 9, 15	V <sub>CC</sub>	+3.3V Supply Voltage
6	MODSET	Modulation Set. A resistor connected from MODSET to ground (R <sub>MODSET</sub> ) programs the desired modulation current amplitude.
7	PEAKSET	Peaking Current Set. A resistor connected between PEAKSET and ground (R <sub>PEAKSET</sub> ) programs the peaking current amplitude. To disable peaking, leave PEAKSET open.
8, 16	GND	Ground
10	OUT-	Inverted Modulation-Current Output
11	OUT+	Noninverted Modulation-Current Output
12	BIASMON	Bias Current Monitor. The output of BIASMON is a sourced current proportional to the bias current. A resistor connected between BIASMON and ground (R <sub>BIASMON</sub> ) can be used to form a ground referenced bias monitor.
13	BIAS	Bias Current Output
14	BIASSET	Bias Current Set. A resistor connected between BIASSET and ground (R <sub>BIASSET</sub> ) programs the VCSEL bias current.
EP	Exposed Pad	Ground. This must be soldered to the circuit board ground for proper thermal and electrical performance. See the <i>Layout Considerations</i> section.

# 3.2Gbps Compact SFP VCSEL Driver

## Functional Diagram



## Detailed Description

The MAX3741 contains a bias generator and a laser modulator with optional peaking compensation.

### Bias Generator

Figure 1 shows the bias generator circuitry that contains a bandgap voltage reference, current mirror, and bias monitor. The bias current output to the laser is controlled with the  $R_{BIASSET}$  resistor. For appropriate  $R_{BIASSET}$  values, see the Bias Current vs.  $R_{BIASSET}$  graph in the *Typical Operating Characteristics*.

The  $BIASMON$  output provides a current proportional to the laser bias current given by:

$$I_{BIASMON} = I_{BIAS} / 9$$

### Modulation Circuit

The modulation circuitry consists of an input buffer, a current mirror, and a high-speed current switch (Figure 2). The modulators drive up to 15mA of modulation into a 50Ω VCSEL load.

The amplitude of the modulation current is set with resistor at  $MODSET$  ( $R_{MODSET}$ ). For appropriate  $R_{MODSET}$  values, see the  $I_{MOD}$  vs.  $R_{MODSET}$  graph in the *Typical Operating Characteristics*. Figure 3 shows a simplified diagram of the MAX3741 output stage.

## Input Termination

The MAX3741 data inputs are SFP MSA compatible. On-chip 100Ω differential input impedance is provided for optimal termination (Figure 4). The MAX3741 inputs self-bias to the proper operating point to accommodate AC-coupling.

## Applications Information

### VCSEL Selection

Select a communications-grade VCSEL with a rise time of 260ps or better for 1.25Gbps or 130ps or better for 2.5Gbps applications.

Use a high-efficiency VCSEL that requires low modulation current and generates a low voltage swing. Trim the leads to reduce VCSEL package inductance. The typical package leads have inductance of 25nH per inch (1nH/mm). This inductance causes a large voltage swing across the VCSEL. A compensation filter network can be used to reduce ringing, edge speed, and voltage swing. See the *Designing the Laser-Compensation Filter Network* section for more information.

### Layout Considerations

To minimize inductance, keep the connections between the MAX3741 output pins and VCSEL as close as possible. Use good high-frequency layout techniques and multiple-layer boards with uninterrupted ground planes to minimize EMI and crosstalk.

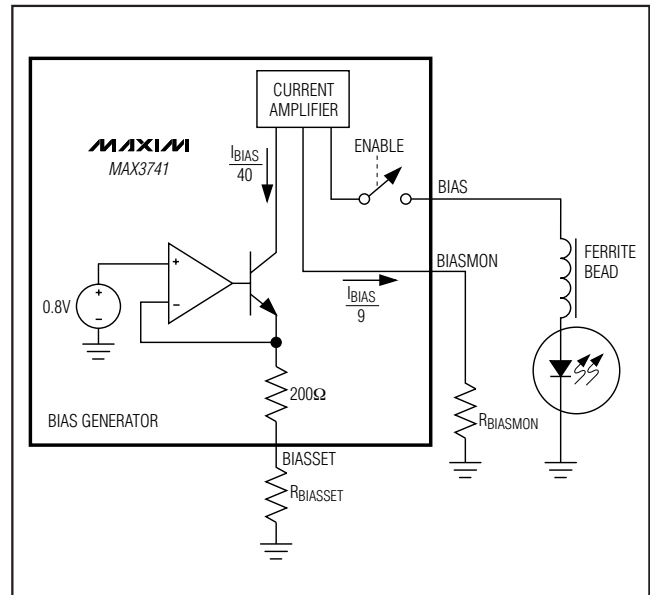


Figure 1. Bias Generator

# 3.2Gbps Compact SFP VCSEL Driver

MAX3741

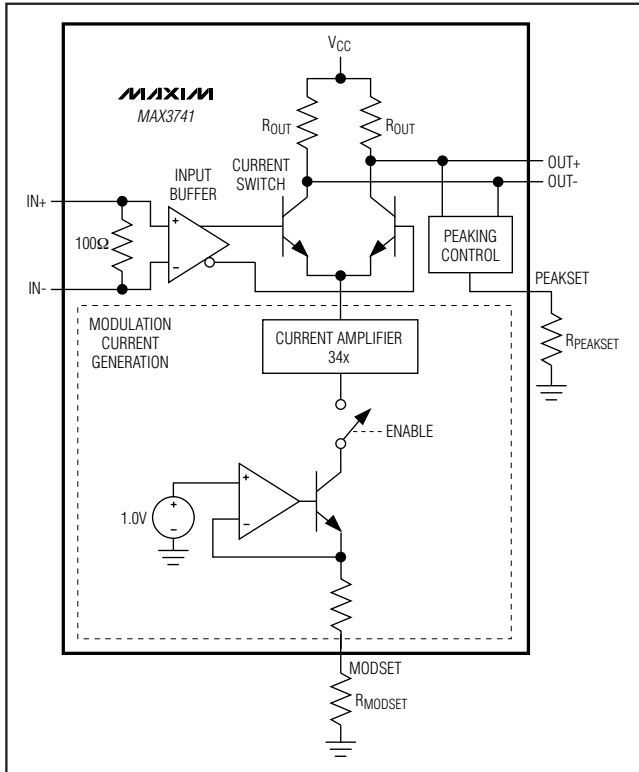


Figure 2. Modulation Circuit

## Designing the Compensation Filter Network

VCSEL package inductance causes the VCSEL impedance to increase at high frequencies, leading to ringing, overshoot, and degradation of the VCSEL output. A VCSEL compensation filter network can be used to reduce the VCSEL impedance at high frequencies, thereby reducing output ringing and overshoot.

The compensation components ( $R_F$  and  $C_F$ ) are most easily determined by experimentation. Begin with  $R_F = 50\Omega$  and  $C_F = 1\text{pF}$ . Increase  $C_F$  until the desired transmitter response is obtained (Figure 5). Refer to Application Note HFAN-2.0: *Interfacing Maxim Laser Drivers with Laser Diodes* for more information.

## Exposed-Pad (EP) Package

The exposed pad on the 16-pin thin QFN provides a very low thermal resistance path for heat removal from the IC. The pad is electrical ground on the MAX3741 and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Maxim Application Note HFAN-08.1: *Thermal Considerations for QFN and Other Exposed Pad Packages*, for additional information.

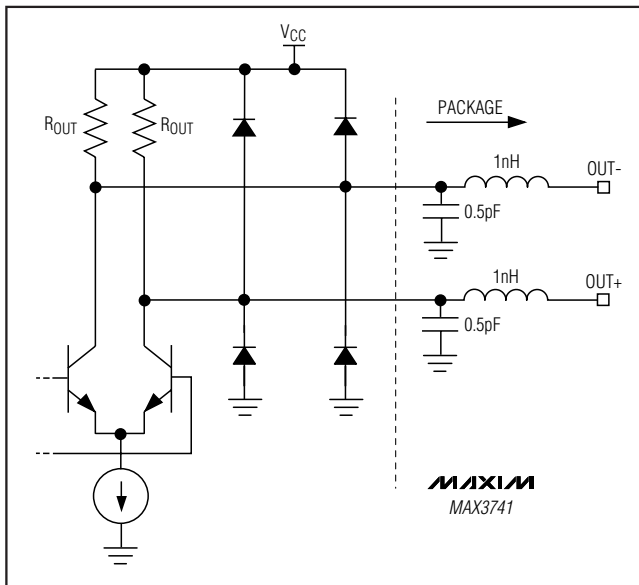


Figure 3. Simplified Output Structure

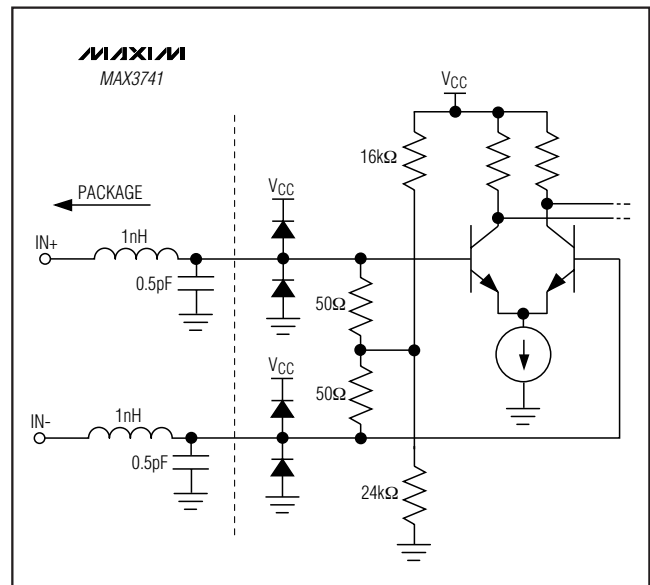


Figure 4. Simplified Input Structure

## 3.2Gbps Compact SFP VCSEL Driver

### Laser Safety and IEC 825

The International Electrotechnical Commission (IEC) determines standards for hazardous light emissions from fiber-optic transmitters. IEC 825 defines the maximum light output for various hazard levels. Using this laser driver alone does not ensure that a transmitter design is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Customers must determine the level of fault tolerance required by their applications, recognizing that Maxim products are not designed or authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application where the failure of a Maxim product could create a situation where personal injury or death may occur.

### Hybrid Lead-Free Package

The MAX3741HETE is a MAX3741 in a hybrid lead-free package. It is a hybrid part that contains high-lead bumps inside a lead-free thin QFN package. The part is not 100% lead free; however, the high-lead solder in the internal portion of the part does meet the RoHS exemption for high-lead solders. For more information, visit [www.maxim-ic.com/emmi](http://www.maxim-ic.com/emmi).

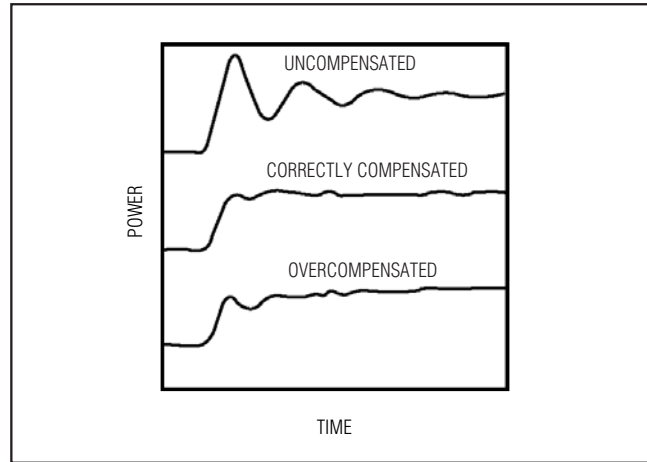


Figure 5. Laser Compensation

### Chip Information

TRANSISTOR COUNT: 1597

PROCESS: SiGe bipolar

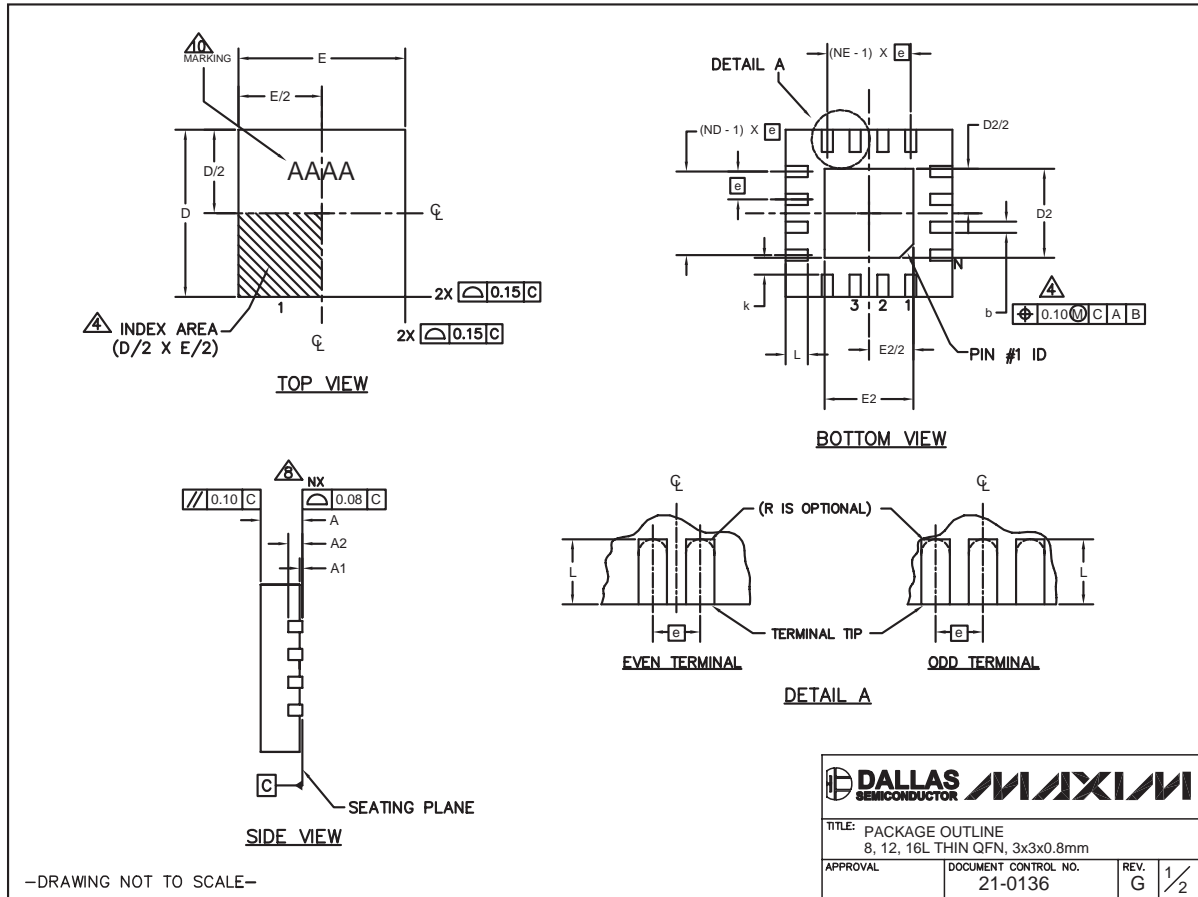


# 3.2Gbps Compact SFP VCSEL Driver

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

**MAX3741**



-DRAWING NOT TO SCALE-

<b>DALLAS SEMICONDUCTOR</b>		<b>MAXIM</b>	
TITLE: PACKAGE OUTLINE 8, 12, 16L THIN QFN, 3x3x0.8mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0136	REV. G	1/2

# 3.2Gbps Compact SFP VCSEL Driver

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

PKG. CODES	D2			E2			PIN ID	JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC	NO
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	NO
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	YES
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2	N/A
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2	N/A
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220 REVISION C.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

<b>DALLAS SEMICONDUCTOR</b>			
<b>MAXIM</b>			
TITLE: PACKAGE OUTLINE			
8, 12, 16L THIN QFN, 3x3x0.8mm			
APPROVAL	DOCUMENT CONTROL NO.	REV.	2/2
	21-0136	G	

## Revision History

- Rev 0; 10/02: Initial data sheet release.
- Rev 1; 5/04: Added package code (page 1); added package drawing (page 9).
- Rev 2; 8/06: Added hybrid package ordering information (pages 1 and 8).

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

10 \_\_\_\_\_ **Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600**



SITE  
SEARCH
PART NO.  
SEARCH

WHAT'S NEW

PRODUCTS

SOLUTIONS

DESIGN

APPNOTES

SUPPORT

BUY

COMPANY

MEMBERS

## MAX3741

### Part Number Table

#### Notes:

1. See the [MAX3741 QuickView Data Sheet](#) for further information on this product family or download the [MAX3741 full data sheet](#) (PDF, 292KB).
2. Other options and links for purchasing parts are listed at: <http://www.maxim-ic.com/sales>.
3. [Didn't Find What You Need?](#) Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
4. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: See [full data sheet](#) or [Part Naming Conventions](#).
5. \* Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses.

Part Number	Free Sample	Buy Direct	Package: TYPE PINS SIZE DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
MAX3741HETE#TG16	<input type="checkbox"/>	<input type="checkbox"/>	THIN QFN;16 pin;3X3X0.8mm Dwg: <a href="#">21-0136I</a> (PDF) Use pkgcode/variation: T1633FH-3*	-40C to +85C	RoHS/Lead-Free: <a href="#">Yes</a> <a href="#">Materials Analysis</a>
MAX3741ETE	<input type="checkbox"/>	<input type="checkbox"/>	Thin QFN;16 pin;3X3X0.8mm Dwg: <a href="#">21-0136I</a> (PDF) Use pkgcode/variation: T1633F-3*	-40C to +85C	RoHS/Lead-Free: <a href="#">No</a> <a href="#">Materials Analysis</a>
MAX3741ETE-T	<input type="checkbox"/>	<input type="checkbox"/>	Thin QFN;16 pin;3X3X0.8mm Dwg: <a href="#">21-0136I</a> (PDF) Use pkgcode/variation: T1633F-3*	-40C to +85C	RoHS/Lead-Free: <a href="#">No</a> <a href="#">Materials Analysis</a>
MAX3741HETE#G16	<input type="checkbox"/>	<input type="checkbox"/>	THIN QFN;16 pin;3X3X0.8mm Dwg: <a href="#">21-0136I</a> (PDF) Use pkgcode/variation: T1633FH-3*	-40C to +85C	RoHS/Lead-Free: <a href="#">Yes</a> <a href="#">Materials Analysis</a>

[Didn't Find What You Need?](#)

[CONTACT US: SEND US AN EMAIL](#)