

DR-135 / DR-235 / DR-435

Service Manual

CONTENTS

SPECIFICATIONS

GENERAL	2
TRANSMITTER	2
RECEIVER	2

CIRCUIT DESCRIPTION DR-135

1) Receiver System (DR-135)	3, 4
2) Transmitter System (DR-135)	4, 5
3) PLL Synthesizer Circuit (DR-135)	5, 6
4) Receiver System (DR-235)	6, 7
5) Transmitter System (DR-235)	7, 8
6) PLL Synthesizer Circuit (DR-235)	8, 9
7) Receiver System (DR-435)	9, 10
8) Transmitter System (DR-435)	10
9) PLL Synthesizer Circuit (DR-435)	11
10) CPU and Peripheral Circuits(DR-135 DR-235 DR-435)	11, 12
11) Power Supply Circuit	13
12) M3826M8269GP (XA0818)	14~16

SEMICONDUCTOR DATA

1) M5218FP (XA0068)	17
2) NJM7808FA (XA0102)	17
3) TC4S66F (XA0115)	17
4) TK10930VTL (XA0223)	18
5) BU4052BF (XA0236)	19
6) TC4W53FU (XA0348)	19
7) M64076GP (XA0352)	20
8) LA4425A (XA0410)	21
9) M67746 (XA0412)	21
10) M68729 (XA0591)	22
11) M57788 (XA0077A)	23
12) mPC2710T (XA0449)	24
13) NJM2902 (XA0596)	24
14) 24LC32A (XA0604)	25
15) S-80845ALMP-EA9-T2 (XA0620)	25
16) L88MS05TLL (XA0675)	25
17) AN8010M (XA0119)	26
18) TK10489M (XA0314)	26
19) Transistor, Diode, and LED Outline Drawings	27
20) LCD Connection (TTR3626UPFDHN)	28

EXPLODED VIEW

1) Top and Front View	29
2) Bottom View	30
3) LCD Assembly	31

PARTS LIST

CPU	32, 33
Main Unit(DR-135)	33~36
Main Unit(DR-235)	36~39
VCO Unit(DR-235)	39
Main Unit(DR-435)	42
VCO Unit(DR-435)	42

Mechanical Parts	43
Packing Parts	43
ACCESSORIES	43
ACCESSORIES(SCREW SET)	43
TNC(EJ41U)	44
TNC (EJ41U) Packing Parts	45

DR-135 ADJUSTMENT

1) Adjustment Spot	46
2) VCO and RX Adjustment Specification	47
3) Tx Adjustment Specification	47
4) Rx Test Specification	48
5) Tx Test Specification	49

DR-235 ADJUSTMENT

1) Adjustment Spot	50
2) VCO and RX Adjustment Specification	51
3) Tx Adjustment Specification	51
4) Rx Test Specification	52
5) Tx Test Specification	53

DR-435 ADJUSTMENT

1) Adjustment Spot	54
2) VCO and RX Adjustment Specification	55
3) Tx Adjustment Specification	55
4) Rx Test Specification	56
5) Tx Test Specification	57

PC BOARD VIEW

1) CPU Unit Side A	58
2) CPU Unit Side B	58
3) Main Unit Side A DR-135 (UP 0400B)	59
4) Main Unit Side B DR-135 (UP 0400B)	59
5) Main Unit Side A DR-235 (UP 0414)	60
6) Main Unit Side B DR-235 (UP 0414)	60
7) Main Unit Side A DR-435 (UP 0415)	61
8) Main Unit Side B DR-435 (UP 0415)	61
9) Tnc Unit Side A (UP 0402) (DR-135TP only)	62
10) Tnc Unit Side B (UP 0402) (DR-135TP only)	62

SCHEMATIC DIAGRAM

1) CPU Unit DR-135 / DR-235 / DR-435	63
2) Main Unit DR-135	64
3) Main Unit DR-235	65
4) Main Unit DR-435	66
5) TNC Unit (DR-135TP only)	67

BLOCK DIAGRAM

1) DR-135	68
2) DR-235	69
3) DR-435	70

ALINCO, INC.

SPECIFICATIONS

■ General

Frequency coverage	DR-135	DR-235	DR-435
T,TG (U.S amateur)	118.000 ~ 135.995MHz (AM RX) 136.000 ~ 173.995MHz (RX) 144.000 ~ 147.995MHz (TX)	216.000 ~ 279.995MHz (RX) 222.000 ~ 224.995MHz (TX)	350.000 ~ 511.995MHz (RX) 430.000 ~ 449.995MHz (TX)
E,EG (European amateur)	144.000 ~ 145.995MHz (RX.TX)		430.000 ~ 439.995MHz (RX.TX)
TA,TAG (Commercial)	118.000 ~ 135.995MHz (AM RX) 136.000 ~ 173.995MHz (RX.TX)		

Operating mode	FM 16K0F3E (Wide mode) 8K50F3E (Narrow mode)		
Frequency resolution	5,8.33,10,12.5,15,20,25,30,50 KHz		
Number of memory channels	100		
Antenna impedance	50Ω unbalanced		
Power requirement	13.8V DC ±15% (11.7 to 15.8V)		
Ground method	Negative ground		
Current drain Receive	0.6A(Max.)	0.4A(Squelched)	
Transmit	11.0A max.	8.0A max.	10.0A max.
Operating temperature	-10°C to 60°C		
Frequency stability	±5ppm		
Dimensions	142(w)×40(h)×174(d) mm (142×40×188mm for projection included)		
Weight	Approx. 1.0kg		

■ Transmitter

Output power	High:50W (144-148MHz)	High:25W	High:35W
	More than 33W (136-174MHz)		
	Mid:10W	Mid:10W	Mid:10W
	Low:Approx.5W	Low:Approx.5W	Low:Approx.5W
Modulation system	Variable reactance frequency modulation		
Maximum frequency deviation	±5kHz (Wide mode) ±2.5kHz (Narrow mode)		
Spurious emission	-60dB		
Adjacent channel power	-60dB		
Noise and hum ratio	-40dB (Wide mode) -34dB (Narrow mode)		
Microphone impedance	2kΩ		

■ Receiver

Sensitivity	-16dBu for 12dB SINAD					
Receiver circuitry	Double conversion superheterodyne					
Intermediate frequency	1st 21.7MHz	2nd 450kHz	1st 30.85MHz	2nd 455kHz	1st 30.85MHz	2nd 455kHz
Squelch sensitivity	-18dBu					
Adjacent channel selectivity	-65dB(Wide mode) -55dB(Narrow mode)					
Intermodulation rejection ratio	60dB					
Spurious and image rejection ratio	70dB					
Audio output power	2.0W (8Ω,10%THD)					

! Note: All specifications are subject to change without notice or obligation.

CIRCUIT DESCRIPTION DR-135/DR-235/DR-435

1) Receiver System (DR-135)

The receiver system is a double superheterodyne system with a 21.7 MHz first IF and a 450 kHz second IF.

1. Front End

The received signal at any frequency in the 136.000MHz to 173.995MHz range is passed through the low-pass filter (L116, L115, L114, L113, C204, C203, C202, C216 and C215) and tuning circuit (L105, L104 and D105, D104), and amplified by the RF amplifier (Q107). The signal from Q107 is then passed through the tuning circuit (L103, L102, and varicaps D103 and D102) and converted into 21.7 MHz by the mixer (Q106). The tuning circuit, which consists of L105, L104, varicaps D105 and D104, L103, L102, varicaps D103 and D102, is controlled by the tracking voltage from the VCO. The local signal from the VCO is passed through the buffer (IC112), and supplied to the source of the mixer (Q106). The radio uses the lower side of the superheterodyne system.

2. IF Circuit

The mixer mixes the received signal with the local signal to obtain the sum of and difference between them. The crystal filter (XF102, XF101) selects 21.7 MHz frequency from the results and eliminates the signals of the unwanted frequencies. The first IF amplifier (Q105) then amplifies the signal of the selected frequency.

3. Demodulator Circuit

After the signal is amplified by the first IF amplifier (Q105), it is input to pin 24 of the demodulator IC (IC108). The second local signal of 21.25 MHz (shared with PLL IC reference oscillation), which is oscillated by the internal oscillation circuit in IC116 and crystal (X103), is input through pin 1 of IC108. Then, these two signals are mixed by the internal mixer in IC108 and the result is converted into the second IF signal with a frequency of 450 kHz. The second IF signal is output from pin 3 of IC108 to the ceramic filter (FL101 or FL102), where the unwanted frequency band of that signal is eliminated, and the resulting signal is sent back to the IC108 through pins 5.

The second IF signal input via pin 5 is demodulated by the internal limiter amplifier and quadrature detection circuit in IC108, and output as an audio signal through pin 12.

4. Audio Circuit

The audio signal from pin 12 of IC108 is amplified by the audio amplifier (IC104:A), and switched by the signal switch IC (IC111) and then input to the de-emphasis circuit.

and is compensated to the audio frequency characteristics in the de-emphasis circuit (R203, R207, R213, R209, C191, C218, C217) and amplified by the AF amplifier (IC104:D). The signal is then input to volume (VR1). The adjusted signal is sent to the audio power amplifier (IC117) through pin 1 to drive the speaker.

5. Squelch Circuit

The detected output which is outputted from the pin 12 of IC108 is inputted to pin 19 of IC108 after it was been amplified by IC104:A and it is outputted from pin 20 after the noise component was been eliminated from the composed band pass filter in the built in amplifier of the IC, then the signal is rectified by D106 to convert into DC component. The adjusted voltage level at VR101 is delivered to the comparator of the CPU.

The voltage is led to pin 2 of CPU and compared with the setting voltage. The squelch will open if the input voltage is lower than the setting voltage.

During open squelch, pin 30 (SQC) of the CPU becomes "L" level, AF control signal is being controlled and sounds is outputted from the speaker.)

6. AIR Band Reception(T only)

When the frequency is within 118~135.995MHz, Q110 automatically turns ON, pin 14 of IC108 becomes "L" level and the condition becomes in AM detection mode.

The receiver signal passed through the duplexer is let to the antenna switch (D107,D101). After passing through the band-pass filter, the signal is amplified by RF amplifier Q112. Secondly the signal is mixed with the signal from the first local oscillator in the first-mixer Q106,then converted into the first IF. Its unwanted signal is let to IC106, pin24. Then converted into the second IF. and is demodulated by AM decoder of IC106, and is output from pin13 as the AF signal.

7. WIDE/NARROW switching circuit

The 2nd IF 450 kHz signal which passes through filter FL101 (wide) and FL102 (narrow) during narrow, changes its width using the width control switching IC103 and IC102.

2) Transmitter System (DR-135)

1. Modulator Circuit

The audio signal is converted to an electrical signal by the microphone, and input it to the microphone amplifier (Q6). Amplified signal which passes through mic-mute control IC109 is adjusted to an appropriate mic-volume by means of mic-gain adjust VR106.

IC114:A and B consists of two operational amplifiers; one amplifier (pins 1, 2, and 3) is composed of pre-emphasis and IDC circuits and the other (pins 5, 6, and 7) is composed of a splatter filter. The maximum frequency deviation is obtained by VR107. and input to the signal switch (IC113) (9600 bps packet signal input switch) and input to the cathode of the varicap of the VCO, to change the electric capacity in the oscillation circuit. This produces the frequency modulation.

2. Power Amplifier Circuit

The transmitted signal is oscillated by the VCO, amplified by the drive amplifier (IC112) and younger amplifier (Q115), and input to the final power module (IC110). The signal is then amplified by the final power module (IC110) and led to the antenna switch (D110) and low-pass filter (L113, L114, L115, L116, C215, C216, C202, C203 and C204), where unwanted high harmonic waves are reduced as needed, and the resulting signal is supplied to the antenna.

3. APC Circuit

Part of the transmission power from the low-pass filter is detected by D111 and D112, converted to DC. The detection voltage is passed through the APC circuit (Q118, Q117, Q116), then it controls the APC voltage supplied to the younger amplifier Q115 and the final power module IC110 to fix the transmission power.

3) PLL Synthesizer Circuit (DR-135)

1. PLL

The dividing ratio is obtained by sending data from the CPU (IC1) to pin 2 and sending clock pulses to pin 3 of the PLL IC (IC116). The oscillated signal from the VCO is amplified by the buffer (Q134 and Q135) and input to pin 15 of IC116. Each programmable divider in IC116 divides the frequency of the input signal by N according to the frequency data, to generate a comparison frequency of 5 or 6.25 kHz.

2. Reference Frequency Circuit

The reference frequency appropriate for the channel steps is obtained by dividing the 21.25 MHz reference oscillation (X103) by 4250 or 3400, according to the data from the CPU (IC1). When the resulting frequency is 5 kHz, channel steps of 5, 10, 15, 20, 25, 30, and 50 kHz are used. When it is 6.25 kHz, the 12.5 kHz channel step is used.

3. Phase Comparator Circuit

The PLL (IC116) uses the reference frequency, 5 or 6.25kHz. The phase comparator in the IC116 compares the phase of the frequency from the VCO with that of the comparison frequency, 5 or 6.25kHz, which is obtained by the internal divider in IC116.

4. PLL Loop Filter Circuit

If a phase difference is found in the phase comparison between the reference frequency and VCO output frequency, the charge pump output (pin 13) of IC116 generates a pulse signal, which is converted to DC voltage by the PLL loop filter and input to the varicap of the VCO unit for oscillation frequency control.

5. VCO Circuit

A Colpitts oscillation circuit driven by Q131 directly oscillates the desired frequency. The frequency control voltage determined in the CPU (IC1) and PLL circuit is input to the varicaps (D122 and D123). This changes the oscillation frequency, which is amplified by the VCO buffer (Q134) and output from the VCO area.

6. VCO Shift Circuit

During transmission or the AIR band Reception (118~136 MHz), the VCO shift circuit turns ON Q138, change control the capacitance of L123 and safely oscillates the VCO by means of H signal from pin 16 of IC116.)

4) Receiver System (DR-235)

The receiver system is a double superheterodyne system with a 30.85 MHz first IF and a 455 kHz second IF.

1. Front End

The received signal at any frequency in the 216.000MHz to 279.995MHz range is passed through the low-pass filter (L116, L115, L114, L113, C204, C203, C202, C216 and C215) and tuning circuit (L105, L104 and D105, D104), and amplified by the RF amplifier (Q107). The signal from Q107 is then passed through the tuning circuit (L103, L107, L102, and varicaps D103, D107 and D102) and converted into 30.85 MHz by the mixer (Q106). The tuning circuit, which consists of L105, L104, varicaps D105 and D104, L103, L107, L102, varicaps D103, D107 and D102, is controlled by the tracking voltage from the VCO. The local signal from the VCO is passed through the buffer (Q112), and supplied to the source of the mixer (Q106). The radio uses the lower side of the superheterodyne system.

2. IF Circuit

The mixer mixes the received signal with the local signal to obtain the sum of and difference between them. The crystal filter (XF102, XF101) selects 30.85 MHz frequency from the results and eliminates the signals of the unwanted frequencies. The first IF amplifier (Q105) then amplifies the signal of the selected frequency.

3. Demodulator Circuit

After the signal is amplified by the first IF amplifier (Q105), it is input to pin 24 of the demodulator IC (IC108). The second local signal of 30.395 MHz, which is oscillated by the internal oscillation circuit in IC108 and crystal (X104), is input through pin 1 of IC108. Then, these two signals are mixed by the internal mixer in IC108 and the result is converted into the second IF signal with a frequency of 455 kHz. The second IF signal is output from pin 3 of IC108 to the ceramic filter (FL101 or FL102), where the unwanted frequency band of that signal is eliminated, and the resulting signal is sent back to the IC108 through pins 5. The second IF signal input via pin 5 is demodulated by the internal limiter amplifier and quadrature detection circuit in IC108, and output as an audio signal through pin 12.

4. Audio Circuit

The audio signal from pin 12 of IC108 is amplified by the audio amplifier (IC104:A), and switched by the signal switch IC (IC111) and then input it to the de-emphasis circuit.

and is compensated to the audio frequency characteristics in the de-emphasis circuit (R203, R207, R213, R209, C191, C218, C217) and amplified by the AF amplifier (IC104:D). The signal is then input to volume (VR1) . The adjusted signal is sent to the audio power amplifier (IC117) through pin 1 to drive the speaker.

5. Squelch Circuit

The detected output which is outputted from the pin 12 of IC108 is inputted to pin 19 of IC108 after it was been amplified by IC104:A and it is outputted from pin 20 after the noise component was been eliminated from the composed band pass filter in the built in amplifier of the IC, then the signal is rectified by D106 to convert into DC component. The adjusted voltage level at VR101 is delivered to the comparator of the CPU.

The voltage is led to pin 2 of CPU and compared with the setting voltage. The squelch will open if the input voltage is lower than the setting voltage.

During open squelch, pin 30 (SQC) of the CPU becomes "L" level, AF control signal is being controlled and sounds is outputted from the speaker.)

6. AIR Band Reception(T only)

If it is made air band receiving mode, IF signal is demodulated by AM decoder of IC106, and is output from pin13 as the AF signal.

7. WIDE/NARROW switching circuit

The 2nd IF 455 kHz signal which passes through filter FL101 (wide) and FL102 (narrow) during narrow, changes its width using the width control switching IC103 and IC102.

5) Transmitter System (DR-235)

1. Modulator Circuit

The audio signal is converted to an electrical signal by the microphone, and input it to the microphone amplifier (Q6). Amplified signal which passes through mic-mute control IC109 is adjusted to an appropriate mic-volume by means of mic-gain adjust VR106.

IC114:A and B consists of two operational amplifiers; one amplifier (pins 1, 2, and 3) is composed of pre-emphasis and IDC circuits and the other (pins 5, 6, and 7) is composed of a splatter filter. The maximum frequency deviation is obtained by VR107. and input to the signal switch (IC113) (9600 bps packet signal input switch) and input to the cathode of the varicap of the VCO, to change the electric capacity in the oscillation circuit. This produces the frequency modulation.

2. Power Amplifier Circuit

The transmitted signal is oscillated by the VCO, amplified by the drive amplifier (IC112) and younger amplifier (Q115), and input to the final power module (IC110). The signal is then amplified by the final power module (IC110) and led to the antenna switch (D110) and low-pass filter (L113, L114, L115, L116, C215, C216, C202, C203 and C204), where unwanted high harmonic waves are reduced as needed, and the resulting signal is supplied to the antenna.

3. APC Circuit

Part of the transmission power from the low-pass filter is detected by D111 and D112, converted to DC. The detection voltage is passed through the APC circuit (Q118, Q117, Q116), then it controls the APC voltage supplied to the younger amplifier Q115 and the final power module IC110 to fix the transmission power.

6) PLL Synthesizer Circuit (DR-235)

1. PLL

The dividing ratio is obtained by sending data from the CPU (IC1) to pin 2 and sending clock pulses to pin 3 of the PLL IC (IC501). The oscillated signal from the VCO is amplified by the buffer (Q504 and Q501) and input to pin 15 of IC501. Each programmable divider in IC501 divides the frequency of the input signal by N according to the frequency data, to generate a comparison frequency of 5 or 6.25 kHz.

2. Reference Frequency Circuit

The reference frequency appropriate for the channel steps is obtained by dividing the 12.8 MHz reference oscillation (X103) by 2560 or 2048, according to the data from the CPU (IC1). When the resulting frequency is 5 kHz, channel steps of 5, 10, 15, 20, 25, 30, and 50 kHz are used. When it is 6.25 kHz, the 12.5 kHz channel step is used.

3. Phase Comparator Circuit

The PLL (IC501) uses the reference frequency, 5 or 6.25kHz. The phase comparator in the IC501 compares the phase of the frequency from the VCO with that of the comparison frequency, 5 or 6.25kHz, which is obtained by the internal divider in IC501.

4. PLL Loop Filter Circuit

If a phase difference is found in the phase comparison between the reference frequency and VCO output frequency, the charge pump output (pin 13) of IC501 generates a pulse signal, which is converted to DC voltage by the PLL loop filter and input to the varicap of the VCO unit for oscillation frequency control.

5. VCO Circuit

A Colpitts oscillation circuit driven by Q503 directly oscillates the desired frequency. The frequency control voltage determined in the CPU (IC1) and PLL circuit is input to the varicaps (D503 and D504). This changes the oscillation frequency, which is amplified by the VCO buffer (Q504) and output from the VCO area.

7) Receiver System (DR-435)

The receiver system is a double superheterodyne system with a 30.85 MHz first IF and a 455 kHz second IF.

1. Front End

The received signal at any frequency in the 430.00MHz to 439.995MHz range is passed through the low-pass filter (L115, L114, L116, C204, C203, C202, C216 and C215) and amplified by the RF amplifier (Q107). The signal from Q107 is then passed through the BPF circuit (L103, L102) and converted into 30.85 MHz by the mixer (Q106). The local signal from the VCO is passed through the buffer (Q503, Q504), and supplied to the source of the mixer (Q106). The radio uses the lower side of the superheterodyne system.

2. IF Circuit

The mixer mixes the received signal with the local signal to obtain the sum of and difference between them. The crystal filter (XF101) selects 30.85MHz frequency from the results and eliminates the signals of the unwanted frequencies. The first IF amplifier (Q105) then amplifies the signal of the selected frequency.

3. Demodulator Circuit

After the signal is amplified by the first IF amplifier (Q105), it is input to pin 20 of the demodulator IC (IC108). The second local signal of 30.85MHz (Crystal oscillator) is input pin 1 of IC108. Then, these two signals are mixed by the internal mixer in IC108 and the result is converted into the second IF signal with a frequency of 455 kHz. The second IF signal is output from pin 4 of IC108 to the ceramic filter (FL101 or FL102), where the unwanted frequency band of that signal is eliminated, and the resulting signal is sent back to the IC108 through pins 6.

The second IF signal input via pin 6 is demodulated by the internal limiter amplifier and quadrature detection circuit in IC108, and output as an audio signal through pin 11.

4. Audio Circuit

The audio signal from pin 11 of IC108 is amplified by the audio amplifier (IC104:A), and switched by the signal switch IC (IC111) and then input to the de-emphasis circuit.

and is compensated to the audio frequency characteristics in the de-emphasis circuit (R203, R207, R213, R209, C191, C218, C217) and amplified by the AF amplifier (IC104:D). The signal is then input to volume (VR1) . The adjusted signal is sent to the audio power amplifier (IC117) through pin 1 to drive the speaker.

5. Squelch Circuit

The detected output which is outputted from the pin 11 of IC108 is inputted to pin 13 of IC108 after it was been amplified by IC104:A and it is outputted from pin 14 after the noise component was been eliminated from the composed band pass filter in the built in amplifier of the IC, then the signal is rectified by D106 to convert into DC component. The adjusted voltage level at VR101 is delivered to the comparator of the CPU.

The voltage is led to pin 2 of CPU and compared with the setting voltage. The squelch will open if the input voltage is lower than the setting voltage.

During open squelch, pin 30 (SQC) of the CPU becomes "L" level, AF control signal is being controlled and sounds is outputted from the speaker.

6. WIDE/NARROW switching circuit

The 2nd IF 455 KHz signal which passes through filter FL101 (wide) and FL102 (narrow) during narrow, changes its width using the width control switching IC103 and IC102.

8) Transmitter System (DR-435)

1. Modulator Circuit

The audio signal is converted to an electrical signal by the microphone, and input it to the microphone amplifier (Q6). Amplified signal which passes through mic. mute control IC109 is adjusted to an appropriate mic. volume by means of mic. gain adjust VR106.

IC114:A and B consists of two operational amplifiers; one amplifier (pins 1, 2, and 3) is composed of pre-emphasis and IDC circuits and the other (pins 5, 6, and 7) is composed of a splatter filter. The maximum frequency deviation is obtained by VR107. and input to the signal switch (IC113) (9600 bps packet signal input switch) and input to the cathode of the varicap of the VCO, to change the electric capacity in the oscillation circuit. This produces the frequency modulation.

2. Power Amplifier Circuit

The transmitted signal is oscillated by the VCO, amplified by the drive amplifier (Q131, Q125) and younger amplifier (Q115), and input to the final power module (IC110). The signal is then amplified by the final power module (IC110) and led to the antenna switch (D110) and low-pass filter (L116, L114, L115, C215, C216, C202, C203 and C204), where unwanted high harmonic waves are reduced as needed, and the resulting signal is supplied to the antenna.

3. APC Circuit

Part of the transmission power from the low-pass filter is detected by D111 and D112, converted to DC. The detection voltage is passed through the APC circuit(Q118, Q117, Q116), then it controls the APC voltage supplied to the younger amplifier Q115 and the final power module IC110 to fix the transmission power.

9) PLL Synthesizer Circuit (DR-435)

1. PLL

The dividing ratio is obtained by sending data from the CPU (IC1) to pin 2 and sending clock pulses to pin 3 of the PLL IC (IC501). The oscillated signal from the VCO is amplified by the buffer (Q503 and Q501) and input to pin 15 of IC501. Each programmable divider in IC501 divides the frequency of the input signal by N according to the frequency data, to generate a comparison frequency of 5 or 6.25 kHz.

2. Reference Frequency Circuit

The reference frequency appropriate for the channel steps is obtained by dividing the 21.25 MHz reference oscillation (X103) by 4250 or 3400, according to the data from the CPU (IC1). When the resulting frequency is 5 kHz, channel steps of 5, 8.33, 10, 15, 20, 25, 30, and 50 kHz are used. When it is 6.25 kHz, the 12.5 kHz channel step is used.

3. Phase Comparator Circuit

The PLL (IC501) uses the reference frequency, 5 or 6.25kHz. The phase comparator in the IC501 compares the phase of the frequency from the VCO with that of the comparison frequency, 5 or 6.25kHz, which is obtained by the internal divider in IC501.

4. PLL Loop Filter Circuit

If a phase difference is found in the phase comparison between the reference frequency and VCO output frequency, the charge pump output (pin 13) of IC501 generates a pulse signal, which is converted to DC voltage by the PLL loop filter and input to the varicap of the VCO unit for oscillation frequency control.

5. VCO Circuit

A Colpitts oscillation circuit driven by Q502 directly oscillates the desired frequency. The frequency control voltage determined in the CPU (IC1) and PLL circuit is input to the varicaps (D502 and D503). This change the oscillation frequency, which is amplified by the VCO buffer (Q503,504) and output from the VCO unit.

10) CPU and Peripheral Circuits (DR-135 DR-235 DR-435)

1. LCD Display Circuit

The CPU turns ON the LCD via segment and common terminals with 1/4 the duty and 1/3 the bias, at the frame frequency is 64Hz.

2. Dimmer Circuit

The dimmer circuit makes the output of pin 13 of CPU (IC1) into "H" level at set mode, so that Q9 and Q3 will turn ON to make the lamp control resistor R84 short and make its illumination bright. But on the other hand, if the dimmer circuit makes pin 13 into "L" level, Q9 and Q3 will turn OFF, R84's illumination will become dimmer as its hang on voltage falls down in the working LED (D11, D2, D5, D3 and D6).

3. Reset and Backup

When the power form the DC cable increases from Circuits 0 V to 2.5 or more, "H" level reset signal is output form the reset IC (IC4) to pin 33 of the CPU (IC1), causing the CPU to reset. The reset signal, however, waits at 100, and does not enter the CPU until the CPU clock (X1) has stabilized.

4. S(Signal) Meter Circuit

The DC potential of pin 16 of IC106 is input to pin 1 of the CPU (IC1), converted from an analog to a digital signal, and displayed as the S-meter signal on the LCD.

5. DTMF Encoder

The CPU (IC1) is equipped with an internal DTMF encoder. The DTMF signal is output from pin 10, through R35, R34 and R261 (for level adjustment), and then through the microphone amplifier (IC114:A), and is sent to the varicap of the VCO for modulation. At the same time, the monitoring tone passes through the AF circuit and is output form the speaker.

6. Tone Encoder

The CPU (IC1) is equipped with an internal tone encoder. The tone signal (67.0 to 250.3 Hz) is output from pin 9 of the CPU to the varicap (D122 and D123) of the VCO for modulation.

7. DCS Encoder

The CPU (IC1) is equipped with an internal DCS code encoder. The code (023 to 754) is output from pin 9 of the CPU to the varicap (D124) of the PLL reference oscillator. When DCS is ON, DCS MUTE circuit (Q126-ON, Q133-ON, Q132-OFF) works. The modulation activates in X103 side only.

8. CTCSS, DCS Decoder

The voice band of the AF output signal from pin 1 of IC104:A is cut by sharp active filter IC104:B and C (VCVS) and amplified, then led to pin 4 of CPU. The input signal is compared with the programmed tone frequency code in the CPU. The squelch will open when they match. During DCS, Q108 is ON, C156 is working and cut off frequency is lowered.

11) Power Supply Circuit

When power supply is ON, there is a "L" signal being inputted to pin 39 (PSW) of CPU which enables the CPU to work.

Then, "H" signal is outputted from the pin 41 (C5C) of CPU and drives ON the power supply switch control Q8 and Q7 which turns the 5VS ON.

5VS turns ON the PLL IC116, main power supply switch Q127 and Q122, AF POWER IC117 and the 8 V of AVR (IC115).

During reception, pin 29 (R5) of CPU outputs "H" level, Q124 is ON, and the reception circuits supplied by 8 V.

While during transmission, pin 28 (T5) of CPU outputs "L" level which is reverse by Q11 so that the output in Q128 will be "H" level, Q123 is ON, and the transmission circuit is supplied by 8 V.

Or, in the case when the condition of PLL is UNLOCK, "H" level is outputted from pin 14 of IC106, UNLOCK switch Q129 is ON, transmission switch Q128 is OFF which makes the transmission to stop.

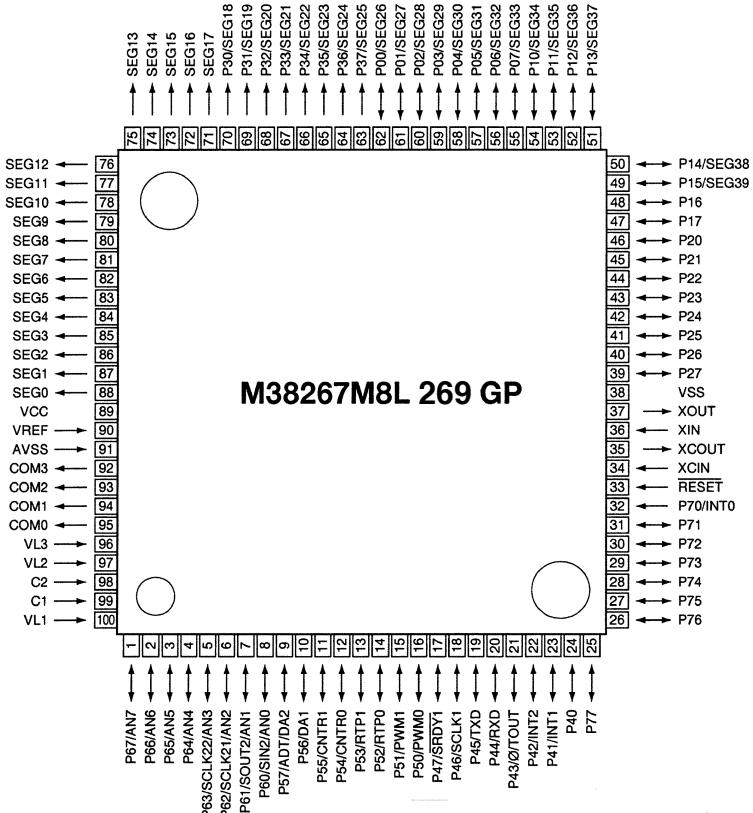
1. ACC External Power Supply Terminal

When optional power supply cord DEC-37 etc. is connected to the external power supply terminal JK101, with ACC power supply ON, switch Q101 will turn ON, 5 V of AVR IC101 pin 2 (STB) becomes "L" which makes C5V to turn ON. With this, it can turn the power supply of the radio ON.

12) M3826M8L269GP (XA0818)

CPU

Terminal Connection
(TOP VIEW)



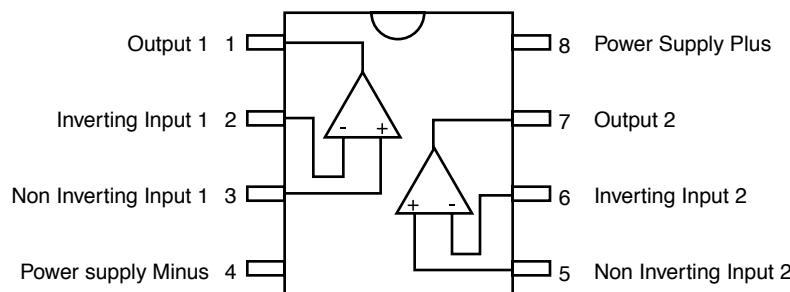
No.	Pin Name	Function	I/O	PU	Logic	Description
1	P67/AN7	SMT	I	-	A/D	S-meter input
2	P66/AN6	SQL	I	-	A/D	Noise level input for squelch
3	P65/AN5	BAT	I	-	A/D	Battery voltage input
4	P64/AN4	TIN	I	-	A/D	CTCSS tone input/DSC code input
5	P63/SCLK22/AN3	BP1	I	-	A/D	Band plan 1
6	P62/SCLK21/AN2	BP2	I	-	A/D	Band plan 2
7	P61/SOUT2/AN1	DCSW	O	-	Activ high	DCS signal mute
8	P60/SIN2/AN0	RE2	I	-	Activ low	Rotary encoder input
9	P57/ADT/DA2	TOUT	O	-	D/A	CTCSS tone output/DCS tone output
10	P56/DA1	DOUT	O	-	D/A	DTMF output
11	P55/CNTR1	SCL	O	-	Pulse	Serial clock for EEPROM
12	P54/CNTR0	TBST	O	-	Pulse	Tone burst output
13	P53/RTP1	BP4	I	-	-	Band plan 4
14	P52/RTP0	MUTE	I/O	-	Activ low	Microphone mute/Security alarm SW
15	P51/PWM3	CLK	O	-	Pulse	Serial clock output for PLL,scramble
16	P50/PWM	DATA	I/O	-	Pulse	Serial data output for PLL scramble/PLL unlock signal input
17	P47/SROY1	TSTB	I/O	-	Activ low/Pulse	Trunking board detection / Strobe signal to trunking board
18	P46/SCLK1	STB	O	-	Pulse	Strobe for PLL IC
19	P45/TXD	UTX	O	-	Pulse	UART data transmission output
20	P44/RXD	RTX	I	-	Pulse	UART data reception output
21	P43/Φ/TOUT	BEEP	I/O	-	Pulse/Activ low	Beep tone/Band plan 3
22	P42I/INT2	SEC	I	-	Activ high	Security voltage input
23	P41/INT1	RE1	I	-	Activ low	Rotary encoder input
24	P40	DSQ	I	-	Activ high	Digital squelch input
25	P77	PTT	I	-	Activ low	PTT input
26	P7	SSTB	O	-	Pulse/Activ low	Strobe signal to scramble IC/Security mode
27	P75	W/N	O	-	Activ low	Wide Narrow SW
28	P74	T5	O	-	Activ low	TX power ON/OFF output
29	P73	R5	O	-	Activ high	RX power ON/OFF output
30	P72	SQC	O	-	Activ low	SQL ON/OFF
31	P71	C/S	O	-	Activ low	Digital scramble ON/OFF
32	P70/INTO	BU	I	-	Activ low	Backup signal detection input
33	RESET	RESET	I	-	Activ low	Reset input
34	Xcin	Xcin	-	-	-	-
35	Xcout	Xcout	-	-	-	-
36	Xin	Xin	-	-	-	Main clock input
37	Xout	Xout	-	-	-	Main clock output
38	Vss	GND	-	-	-	CPU GND
39	P27	PSW	I	-	Activ low	Power switch input
40	P26	SDA	O	-	Pulse	Serial data for EEPROM
41	P25	C5C	O	-	Activ high	C5V power ON/OFF output
42	P24	AIR	O	-	Activ high	Air band SW / Tx middle power
43	P23	LOW	O	-	Activ high	Tx low power
44	P22	EXP	O	-	Activ high	Trunking data SW
45	P21	SW6	I	*	Activ low	Key sw6 (SQL)
46	P20	SW5	I	*	Activ low	Key sw5 (CALL)
47	P17	SW4	I	*	Activ low	Key sw4 (TSQ)
48	P16	SW3	I	*	Activ low	Key sw3 (MHz)
49	P15/SEG39	SW2	I	*	Activ low	Key sw2 (V/M)
50	P14/SEG38	SW1	I	*	Activ low	Key sw1 (FUNC)
51	P13/SEG37	DOWN	I	*	Activ low	Mic down input
52	P12/SEG36	DUD	I	-	-	Digital unit detect
53	P11/SEG35	SCR	I	*	Active low	Scramble IC ready signal/Packet PTT
54	P10/SEG34	UP	I	*	Active low	Mic down input
55	P07/SEG33	S33	O	-	-	LCD segment signal

No.	Pin Name	Function	I/O	PU	Logic	Description
56	P06/SEG32	S32	O	-	-	
57	P05/SEG31	S31	O	-	-	
58	P04/SEG30	S30	O	-	-	
59	P03/SEG29	S29	O	-	-	
60	P02/SEG28	S28	O	-	-	
61	P01/SEG27	S27	O	-	-	
62	P00/SEG26	S26	O	-	-	
63	P37/SEG25	S25	O	-	-	
64	P36/SEG24	S24	O	-	-	
65	P35/SEG23	S23	O	-	-	
66	P34/SEG22	S22	O	-	-	
67	P33/SEG21	S21	O	-	-	
68	P32/SEG20	S20	O	-	-	
69	P31/SEG19	S19	O	-	-	
70	P30/SEG18	S18	O	-	-	
71	SEG17	S17	O	-	-	
72	SEG16	S16	O	-	-	LCD segment signal
73	SEG15	S15	O	-	-	
74	SEG14	S14	O	-	-	
75	SEG13	S13	O	-	-	
76	SEG12	S12	O	-	-	
77	SEG11	S11	O	-	-	
78	SEG10	S10	O	-	-	
79	SEG9	S9	O	-	-	
80	SEG8	S8	O	-	-	
81	SEG7	S7	O	-	-	
82	SEG6	S6	O	-	-	
83	SEG5	S5	O	-	-	
84	SEG4	S4	O	-	-	
85	SEG3	S3	O	-	-	
86	SEG2	S2	O	-	-	
87	SEG1	S1	O	-	-	
88	SEG0	S0	O	-	-	
89	Vcc	VDD	-	-	-	CPU power terminal
90	Vref	Vref	-	-	-	AD converter power supply
91	Avss	Avss	-	-	-	AD converter GND
92	COM3	COM3	O	-	-	LCD COM3 output
93	COM2	COM2	O	-	-	LCD COM2 output
94	COM1	COM1	O	-	-	LCD COM1 output
95	COM0	COM0	O	-	-	LCD COM0 output
96	VL3	VL3	-	-	-	
97	VL2	VL2	-	-	-	LCD power supply
98	C2	I	-	-	-	-
99	C1	C1	-	-	-	-
100	VL1	VL1	I	-	A/D	LCD power supply

SEMICONDUCTOR DATA

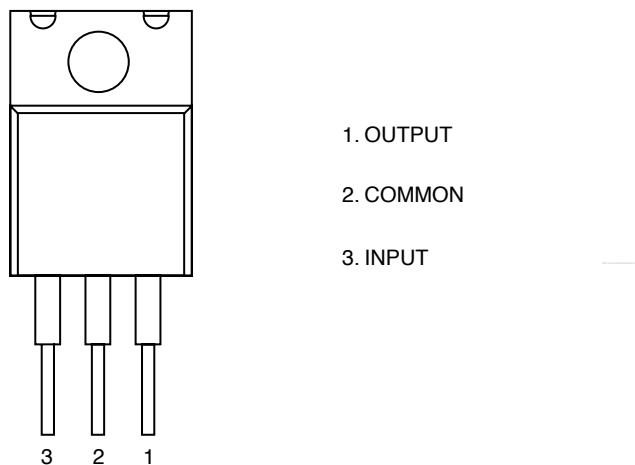
1) M5218FP (XA0068)

Dual Low Noise
Operational Amplifiers



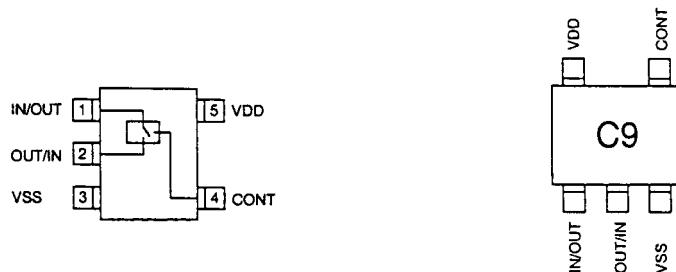
2) NJM7808FA (XA0102)

Pin Assignment



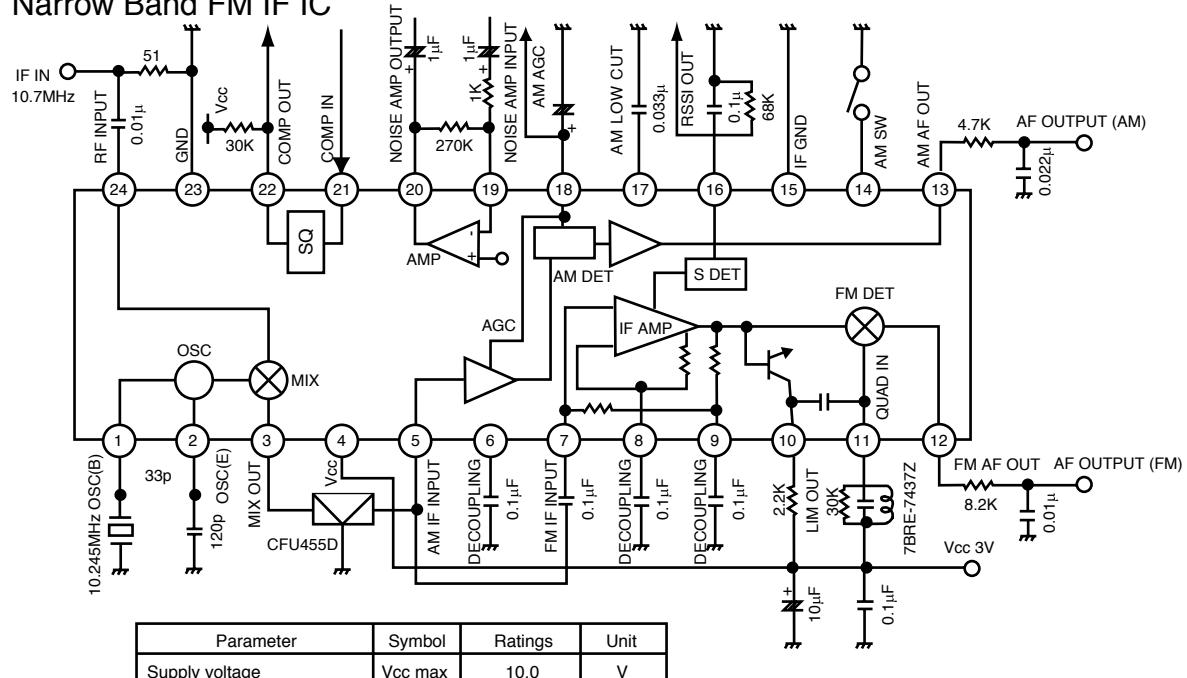
3) TC4S66F (XA0115)

Bilateral Switch



4) TK10930VTL (XA0223)

Narrow Band FM IF IC



Parameter	Symbol	Ratings	Unit
Supply voltage	Vcc max	10.0	V
Power dissipation	Pd	400	mV
Storage temperature	Tstg	-55~+150	°C
Operating temperature	Top	-30~+75	°C
Operating voltage	Vop	2.5~8.5	V
Operating frequency	fop	~60	MHz

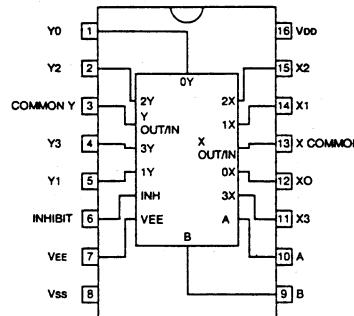
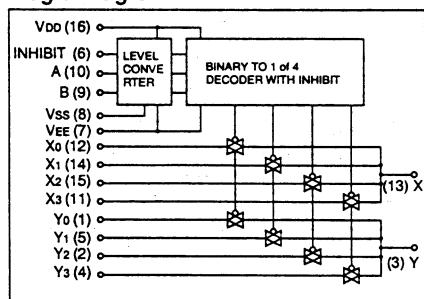
Ta=25°C Vcc=3V

Parameter	Symbol	Ratings			Unit	Condition
		Min	Typical	Max		
Supply Current 1	Icc1		6.8	8.9	mA	No signal, AM ON
Supply Current 2	Icc2		3.9	5.3	mA	No signal, AM OFF
Mixer Coversion Gain	Mg		20		dB	
Mixer Input Impedance	Mz		3.6		KΩ	DC Test
FM						
Limiting Sensitivity	Limit		2.0	8.0	µV	-3.0dB
Output Voltage	Vo1	85	150	230	mVRms	10mVin +/-3kHz DEV
Distortion	THD1		1.0	2.0	%	10mVin +/-3kHz DEV
Output Impedance	Zo		800		Ω	10mVin
Filter Gain	Gf	30	38		dB	Fin=30kHz, Vo=100mV
Scan Control Hi Voltage	SH	2.3			V	Squelch input=2.5V
Scan Control Low Voltage	SL		0.3		V	Squelch input=0V
Squelch Hysteresis	Hys		30		mV	
S meter Output Voltage	S0		0.05	0.5	V	Vin=0mV, RS=68kΩ
S meter Output Voltage	S1	0.05	0.5	0.9	V	Vin=0.01mV, RS=68kΩ
S meter Output Voltage	S2	0.7	1.2	1.7	V	Vin=0.1mV, RS=68kΩ
S meter Output Voltage	S3	1.2	1.8	2.5	V	Vin=1mV, RS=68kΩ
S meter Output Voltage	S4	1.6	2.3	2.9	V	Vin=10mV, RS=68kΩ
S meter Output Voltage	S5	1.8	2.4	2.9	V	Vin=100mV, RS=68kΩ
AM						
Sensitivity	US	20	15		µV	required input level to get 20mV rms output
Output Voltage	Vo2	60	120	160	mVRms	1kHz, 30%, Vin=1mV
Distortion-1	THD2		1.0	2.0	%	1kHz, 30%, Vin=1mV
Distortion-2	THD3		2.0	4.0	%	1kHz, 30%, Vin=1mV
S/N	S/N	40	48		dB	1kHz, 30%, Vin=1mV
AM OFF	Vo	-0.3		0.3	%	

5) BU4052BF (XA0236)

Analog Multiplexer/Demultiplexer

Logic Diagram



Truth Table

INHIBIT	A	B	ON SWITCH
L	L	L	X0 Y0
L	H	L	X1 Y1
L	L	H	X2 Y2
L	H	H	X3 Y3
H	X	X	NONE

X: Don't Care

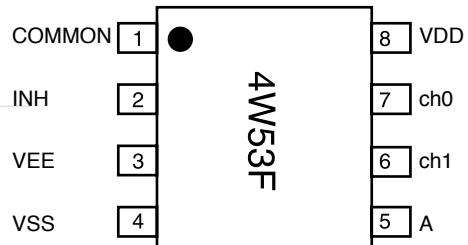
6) TC4W53FU (XA0348)

Multiplexer/Demultiplexer

Function Table

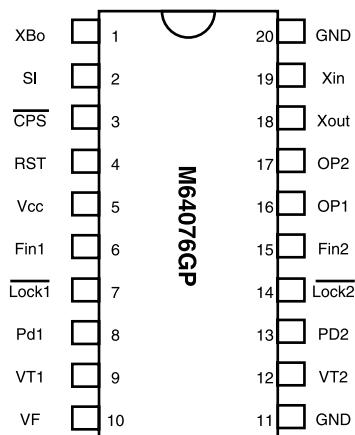
Control input		ON channel
INH	A	
L	L	ch0
L	H	ch1
H	*	NONE

* Don't Care



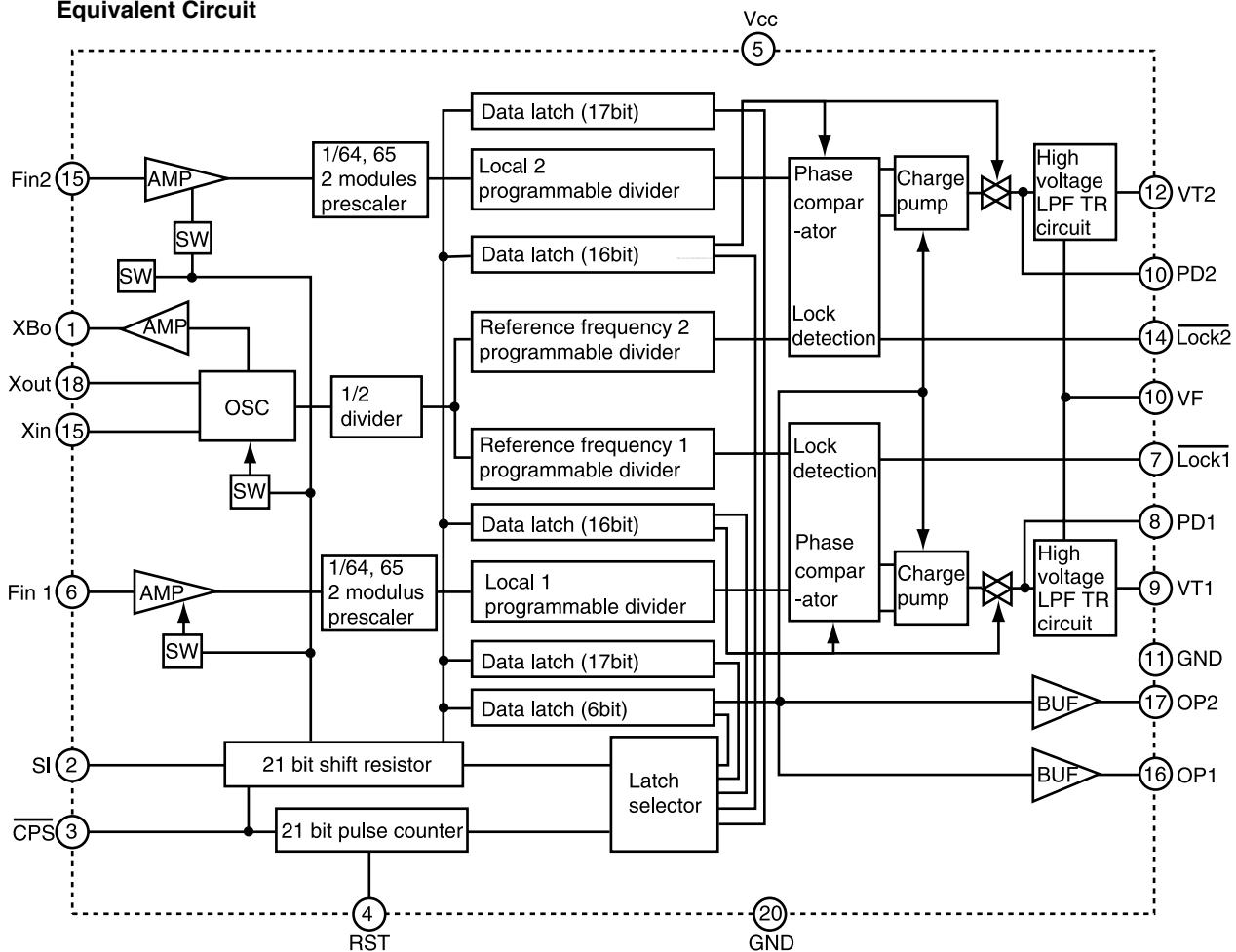
7) M64076GP (XA0352)

Dual PLL Synthesizer



Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	Fin=80~520MHz Vin=-10dBm	2.7	-	5.5	V
LPF supply voltage	VF		-	9	12	V
Local oscillator input level	Vin	Fin=80~520MHz	-20	-	-4	dBm
Local oscillator input frequency	Fin	Vin=-20~-4dBm Vcc=2.7~5.5V	80	-	520	MHz
Xin input level	Vxin	Vcc=2.7~5.5V Fxin=10~25MHz Sine wave	0.4	-	1.4	Vp-p
Xin input frequency	Fxin	Vcc=2.7~5.5V Vxin=0.4~1.4Vp-p	10	-	25	MHz

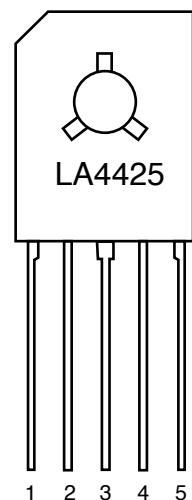
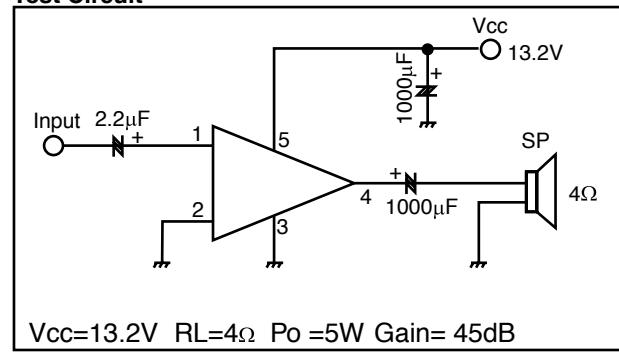
Equivalent Circuit



8) LA4425A (XA0410)

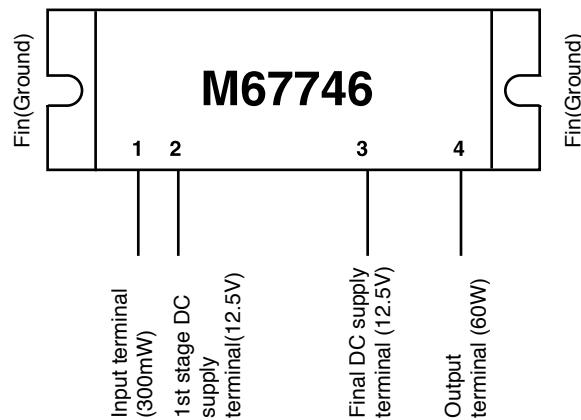
5W Audio Power Amplifiers

Test Circuit



9) M67746 (XA0412)

144 ~ 148MHz 60W
RF Power Module



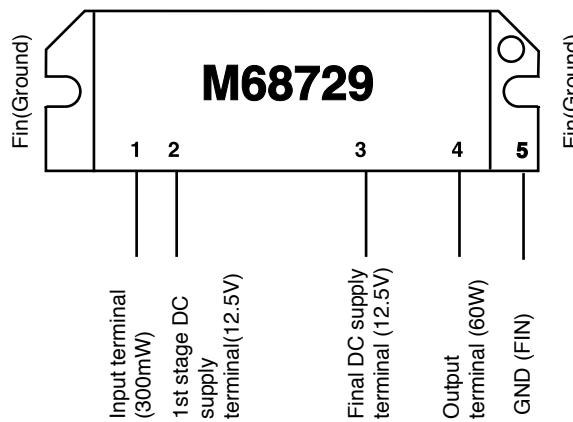
Rating	Symbol	Ratings	Unit
Supply voltage	Vcc	17	V
Total current	Icc	20	A
Input power	Pin(max)	600	mW
Output Power	Po(max)	70	W
Operation case temperature	Tc(op)	-30 to + 110	°C
Strage temperature	Tstg	-40 to + 110	°C

Zg=Zl=50Ω

10) M68729 (XA0591)

220 ~ 246MHz 30W
RF Power Module

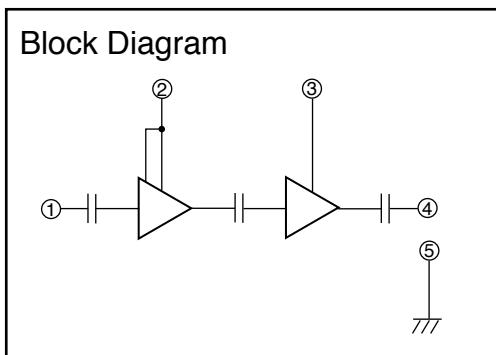
ABSOLUTE MAXIMUM RATING($T_C = 25^\circ\text{C}$)



Rating	Symbol	Ratings	Unit
Supply voltage	Vcc	17	V
Total current	Icc	10	A
Input power	Pin(max)	600	mW
Output Power	Po(max)	40	W
Operation case temperature	Tc(op)	-30 to + 110	°C
Strage temperature	Tstg	-40 to + 110	°C

$Z_g = Z_L = 50\Omega$

ELECTRICAL CHARACTERISTICS

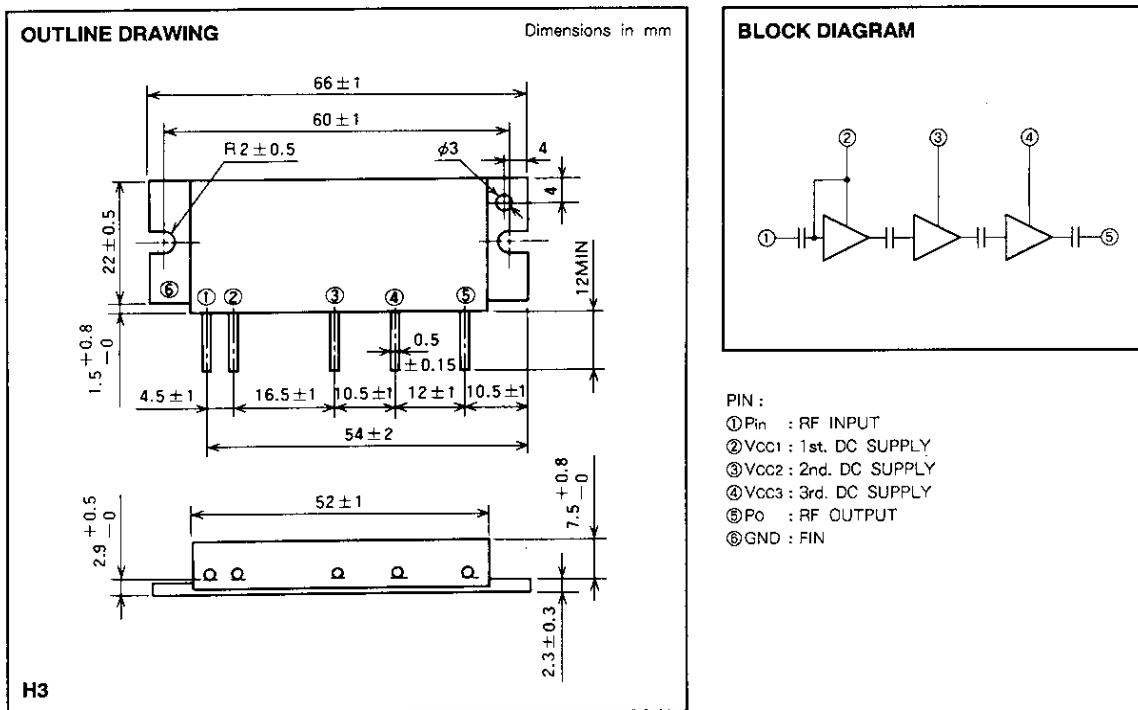


PIN :

- ① Pin : RF INPUT
- ② Vcc1 : 1st. DC SUPPLY
- ③ Vcc2 : 2nd. DC SUPPLY
- ④ PO : RF OUTPUT
- ⑤ GND : FIN

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range	$V_{CC1,2} = 12.5V$ $Pin = 300mV$ $Z_G = Z_L = 50\Omega$	220	246	MHz
Po	Output power		30		W
η_T	Total efficiency		40		%
2fo	2nd. harmonic			-30	dBc
3fo	3rd. harmonic			-30	dBc
pin	Input VSWR			3	-
-	Load VSWR tolerance	$V_{CC1,2} = 15.2V$ $Po = 30W(Pin = Controlled)$ $Load VSWR = 20:1$ (All phase), $Z_G = 50\Omega$	No degradation or destroy		-

11) M57788M (XA0077)



ABSOLUTE MAXIMUM RATINGS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc1			16	V
Vcc2,3	Supply voltage		17	V
Icc	Total current		12	A
Pin(max)	Input power	$Z_G = Z_L = 50 \Omega$	0.5	W
Po(max)	Output power	$Z_G = Z_L = 50 \Omega$	50	W
Tc(OP)	Operation case temperature		-30~110	°C
Tstg	Storage temperature		-40~110	°C

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

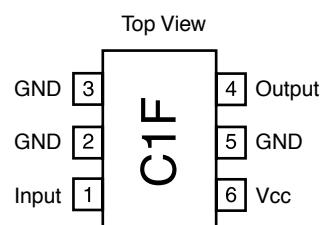
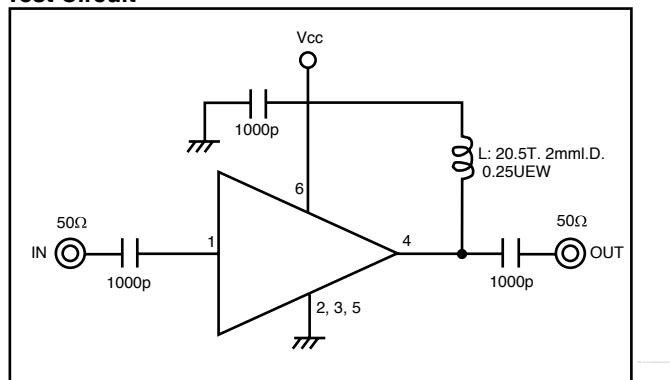
Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range		430	450	MHz
Po	Output power		40		W
η_T	Total efficiency	$V_{cc} = 12.5V$	40		%
2fo	2nd. harmonic	$Z_G = Z_L = 50 \Omega$		-30	dB
ρ_{in}	Input VSWR			2.8	-
-	Load VSWR tolerance	$V_{cc} = 15.2V$, $P_o = 40W$ (P_{in} : controlled) Load VSWR=8.8:1(All phase), 2sec. $Z_G = 50 \Omega$	No degradation		-

12) μPC2710T (XA0449)

RF Amplifier

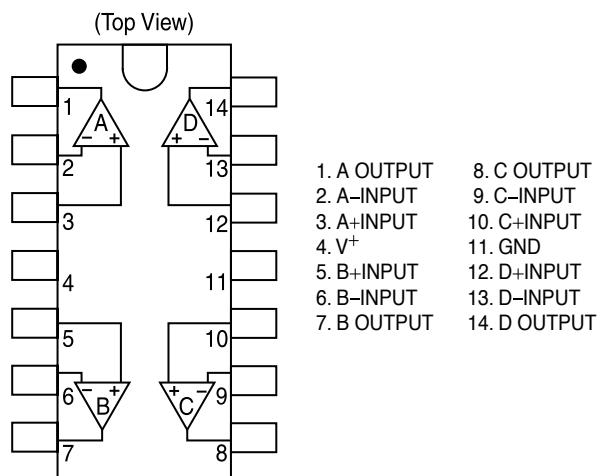
Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	Vcc		5.0	V
Circuit current	Icc	Vcc=5V, no signal	22	mA
Power gain	GP	Vcc=5V, f=500MHz	33	dB
Saturated output power	Po(sat)	Vcc=5V, f=500MHz, Pin=-8dBm	+13.5	dBm
Noise figure	NF	Vcc=5V, f=500MHz	3.5	dB
Upper frequency (-3dB)	fu	Vcc=5V, Reference freq. =100MHz	1000	MHz
Isolation	ISL	Vcc=5V, f=500MHz	39	dB
Input return loss	RL in	Vcc=5V, f=500MHz	6	dB
Output return loss	RL out	Vcc=5V, f=500MHz	12	dB
Gain flatness	Gp	Vcc=5V, f=0.1~0.6GHz	0.8	dB

Test Circuit



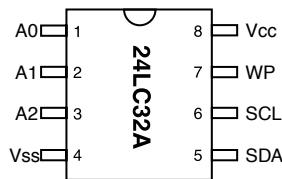
13) NJM2902 (XA0596)

Pin Assignment



14) 24LC32A (XA0604)

PDIP

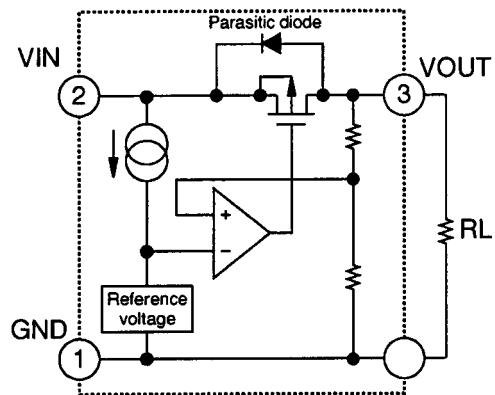
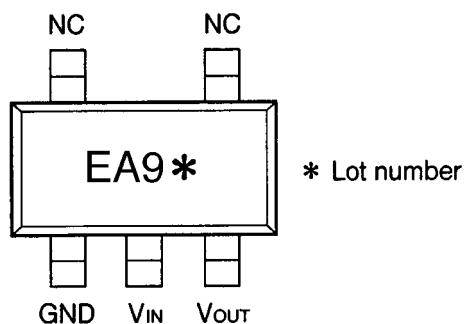


Name	Function
A0..A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+2.5V~6.0V Power Supply

15) S-80845ALMP-EA9-T2 (XA0620)

Vin=18V

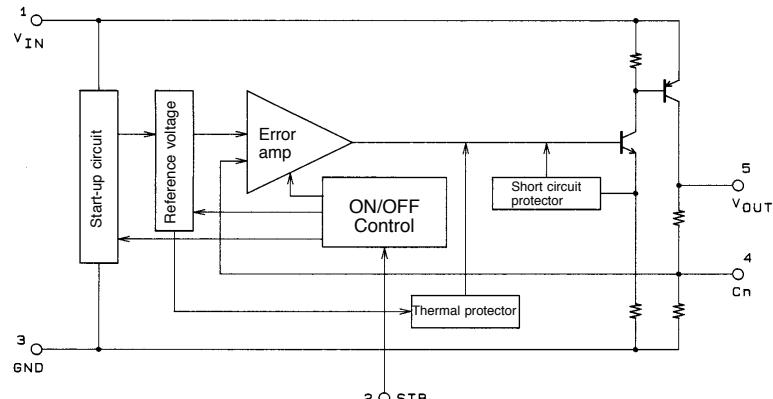
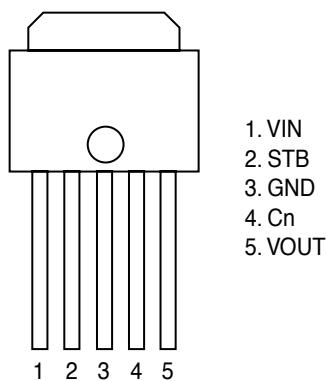
Iout=100mA



16) L88MS05TLL (XA0675)

5V Voltage Regulator With On/Off Function

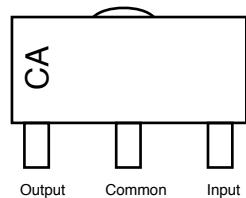
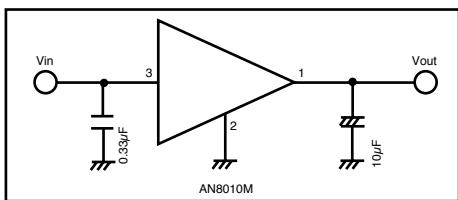
Pin Assignment



17) AN8010M (XA0119)

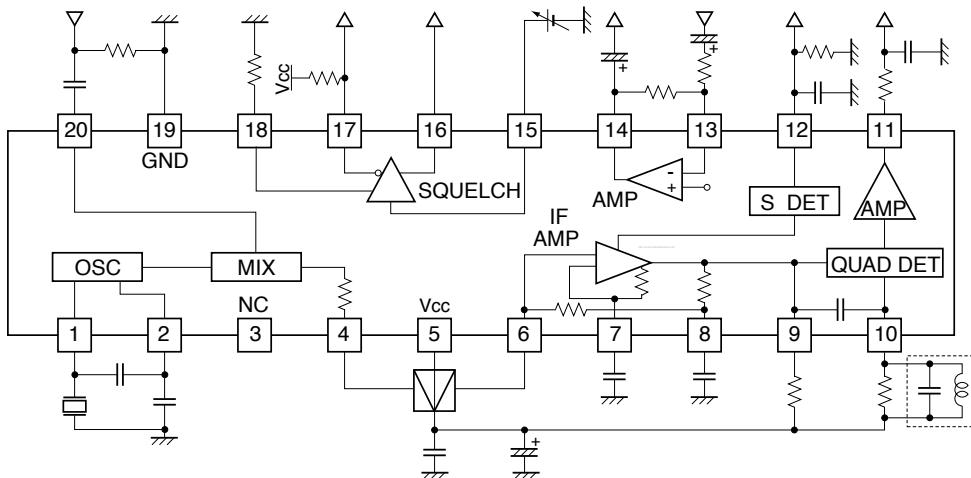
Voltage Regulator

Test Circuit



AN8010M

18) TK10489M (XA0314)



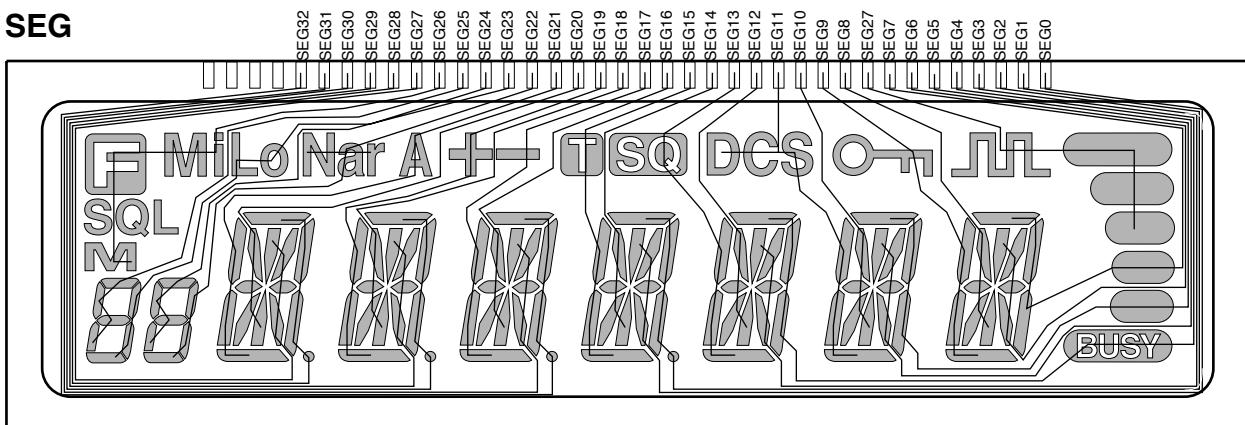
19) Transistor, Diode, and LED Outline Drawings

Top View

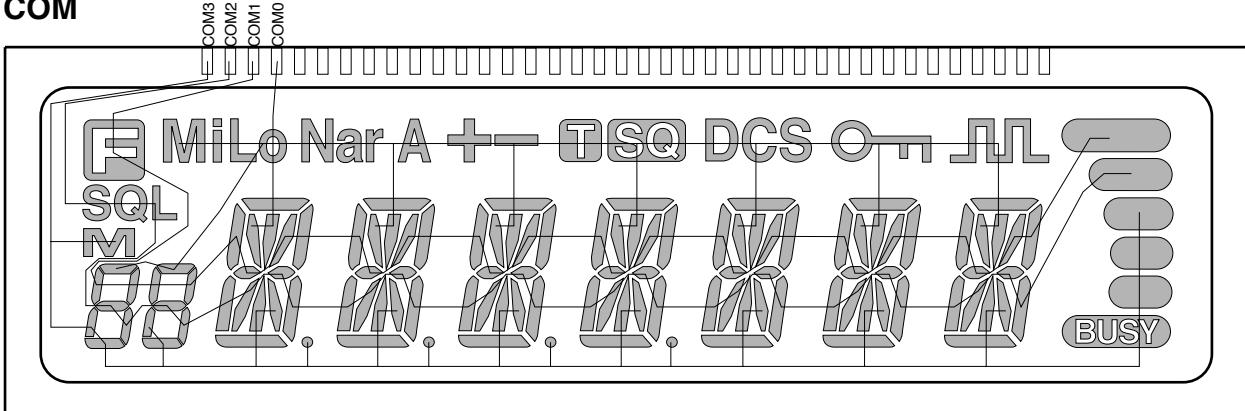
RLS-73 XD0363	1SS355 XD0254	1SS356 XD0272	1SV214 XD0131	1SV237 XD0141	1SV262 XD0300	1SV268 XD0301
DA204U XD0130	DAN235U XD0246	DSA3A1 XD0131	MA304 XD0299	MA729 XD0300	MA8100 XD0297	MA742 XD0250
MI407 XD0013	2SK508 XE0010	2SK880GR XE0021	3SK131V12 XE0028	2SA1036K XT0110	2SA1576 XT0094	2SA1736 XT0099
2SB1132 XT0061	2SB1292F XT0112	2SC2954 XT0084	2SC3356 XT0030	2SC3357 XT0048	2SC4081 XT0095	2SC4099 XT0096
2SC4215 XT0124	2SC4226 XT0141	2SC4245 XT0125	3SK184S XE0013	DTA114YU XU0112	DTC114EU XU0131	DTC144EUA XU0148
DTC144YU XU0029	FA1111C XL0069	FA1111C XL0077	UDZ5.1B XD0165	UMC3TR XU0047	UMC5N XU0152	U1BC44 XD0135
XP1215 XU0178						

20) LCD Connection (TTR3626UPFDHN)

SEG

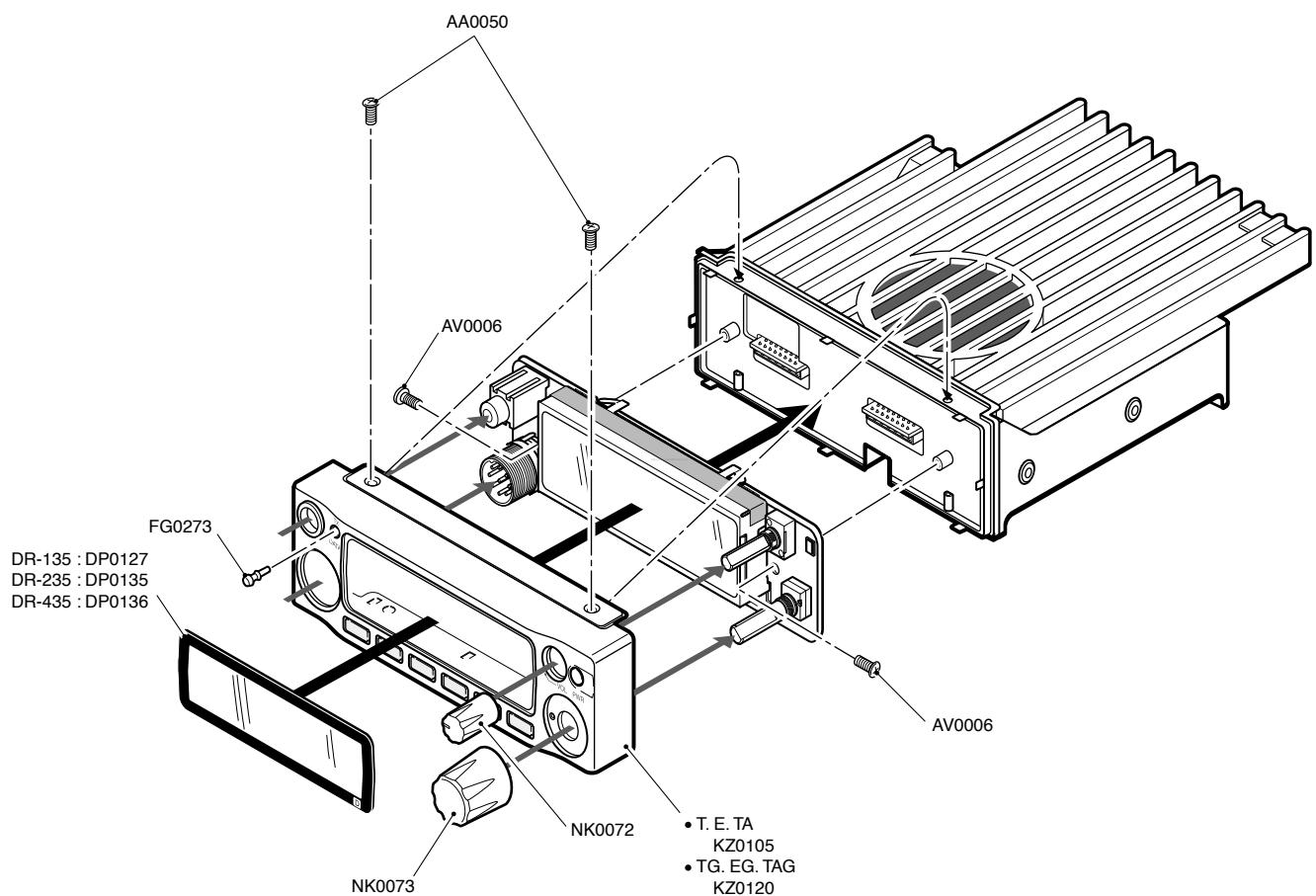


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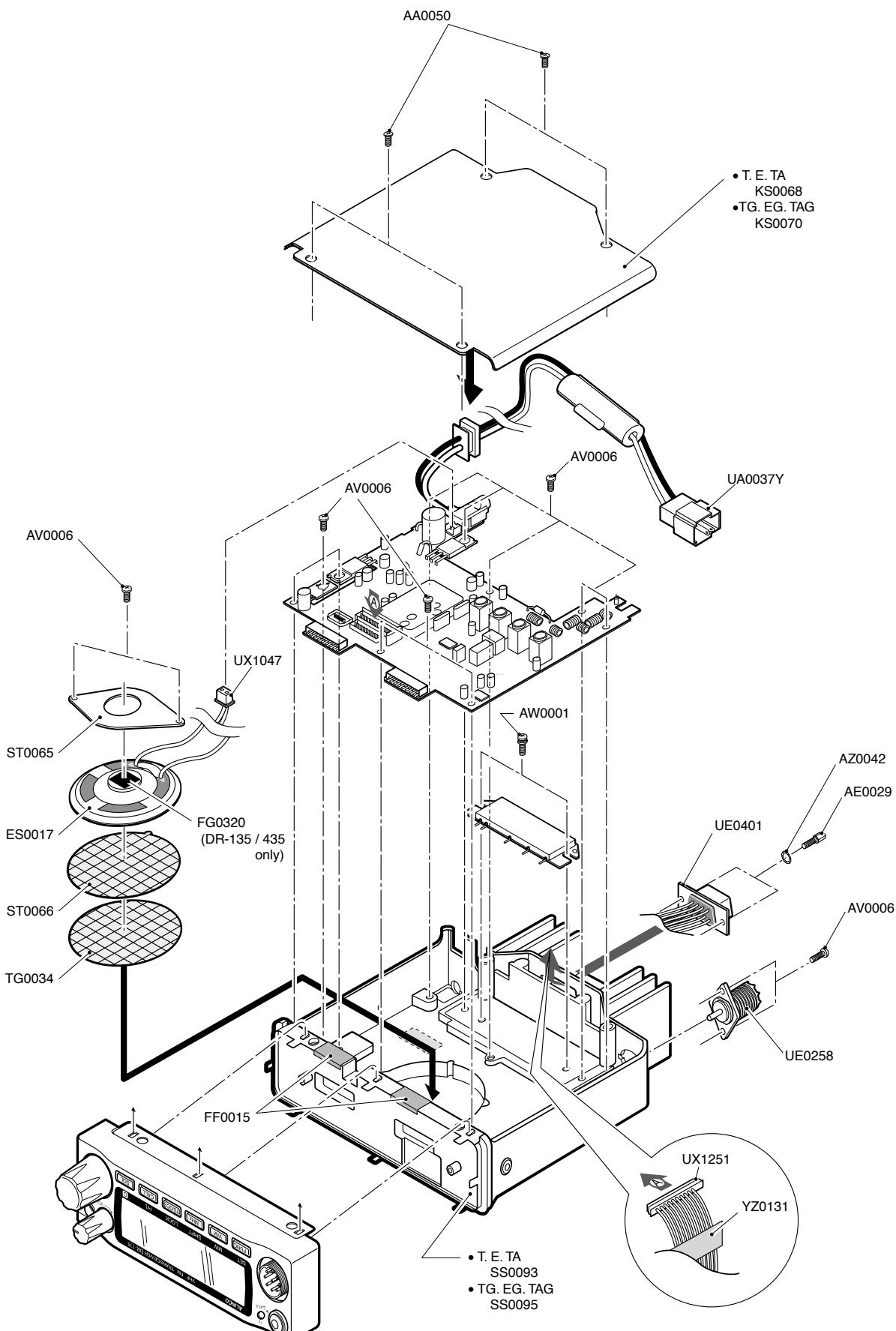


EXPLODED VIEW

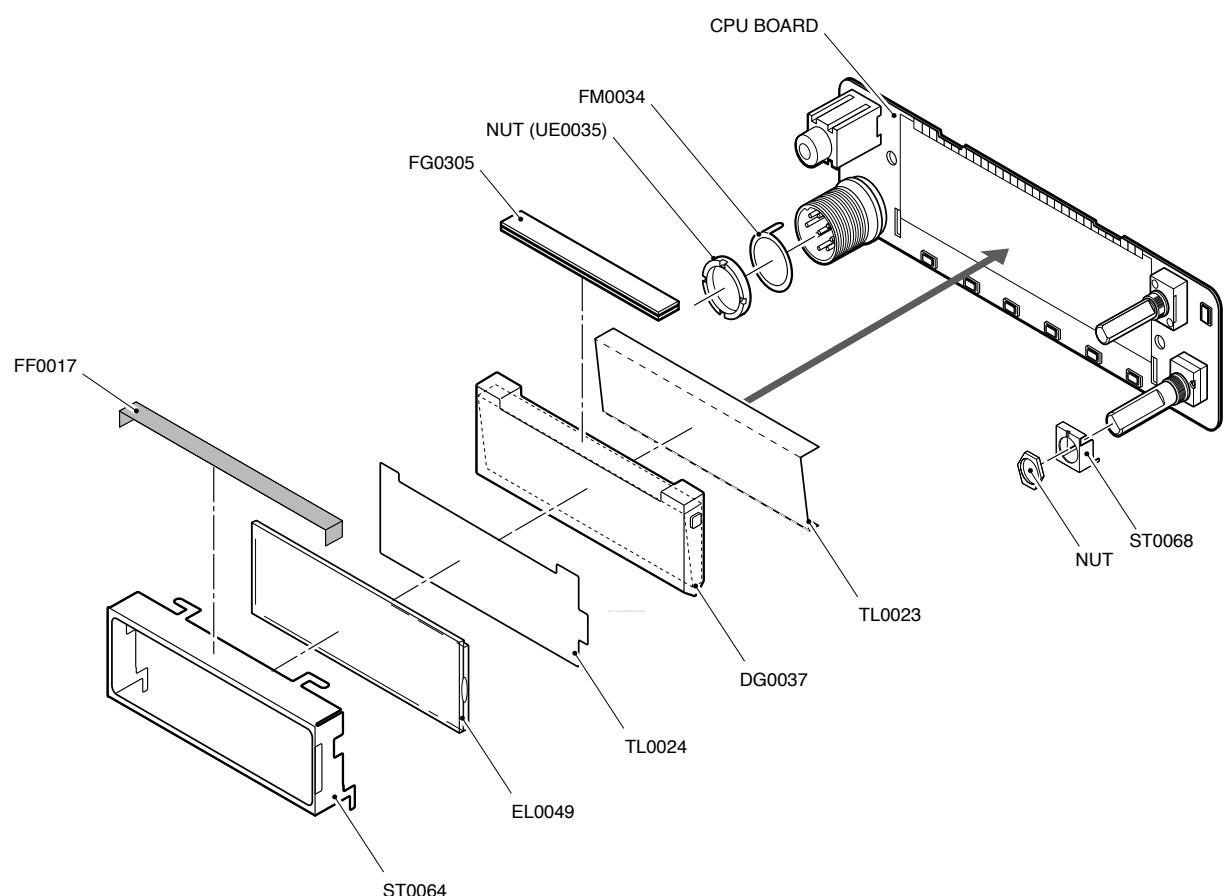
1) Top and Front View



2) Bottom View



3) LCD Assembly



Ref. No.	Parts No.	Description	Parts Name	Qty			Ver
				DR-135	DR-235	DR-435	
SW1	UU0015Z	Switch	EVQPPXA25	1	1	1	
SW2	UU0015Z	Switch	EVQPPXA25	1	1	1	
SW3	UU0015Z	Switch	EVQPPXA25	1	1	1	
SW4	UU0015Z	Switch	EVQPPXA25	1	1	1	
SW5	UU0015Z	Switch	EVQPPXA25	1	1	1	
SW6	UU0015Z	Switch	EVQPPXA25	1	1	1	
SW7	UU0015Z	Switch	EVQPPXA25	1	1	1	
VR1	RV0035	Variable	EUVF2JFK4B14	1	1	1	
W1	UX1270	Wire	WIRE DR235 W1	1	1	1	
X1	XQ0131	Xtal	CSA310/3.6864MHz	1	1	1	
TL0024			DIFFUSION SHEET 135	1	1	1	
YZ0042			CEMENT G17 / 1G	1	1	1	
ST0068			DIAL FITTING	1	1	1	
FG0305			LCD RUB.CONNECT. 135	1	1	1	
TL0023			REFLECTION DR135	1	1	1	
DG0037			LCD LIGHT DR135	1	1	1	
FM0034			MIC GND PLATE	1	1	1	
FP0034			MIC SPACER DR110	1	1	1	
ST0064			LCD HOLDER DR135	1	1	1	

Main Unit (DR-135)

Ref. No.	Parts No.	Description	Parts Name	Qty			Ver
				DR-135	DR-235	DR-435	
C101	CU3047	Chip C.	C1608JB1H103KT-N	1			
C102	CU3047	Chip C.	C1608JB1H103KT-N	1			
C103	CS0049	Chip tantalum	TMC8A1C105MTR	1			
C104	CU3047	Chip C.	C1608JB1H103KT-N	1			
C105	CS0394	Chip tantalum	TMCMB0J476MTR	1			
C106	CU3051	Chip C.	C1608JB1E223KT-NS	1			
C107	CU3111	Chip C.	C1608JB1C104KT-N	1			
C108	CU3047	Chip C.	C1608JB1H103KT-N	1			
C109	CS0216	Chip tantalum	TMCMB1A106MTR	1			
C110	CU3047	Chip C.	C1608JB1H103KT-N	1			
C111	CU3047	Chip C.	C1608JB1H103KT-N	1			
C112	CU3047	Chip C.	C1608JB1H103KT-N	1			
C113	CU3047	Chip C.	C1608JB1H103KT-N	1			
C114	CU3047	Chip C.	C1608JB1H103KT-N	1			
C115	CU3047	Chip C.	C1608JB1H103KT-N	1			
C116	CU3047	Chip C.	C1608JB1H103KT-N	1			
C117	CU3047	Chip C.	C1608JB1H103KT-N	1			
C118	CU3049	Chip C.	C1608JB1E153KT-NS	1			
C119	CU3051	Chip C.	C1608JB1E223KT-NS	1			
C120	CU3021	Chip C.	C1608CH1H680JT-AS	1			
C121	CU3005	Chip C.	C1608CH1H040CT-AS	1			
C122	CU3002	Chip C.	C1608CH1H010CT-AS	1			
C123	CU3015	Chip C.	C1608CH1H220JT-AS	1			
C124	CU3040	Chip C.	C1608JB1H272KT-NS	1			
C125	CU3044	Chip C.	C1608JB1H562KT-NS	1			
C126	CU3038	Chip C.	C1608JB1H182KT-AS	1			
C127	CU3041	Chip C.	C1608JB1H332KT-NS	1			
C129	CU3111	Chip C.	C1608JB1C104KT-N	1			
C130	CS0049	Chip tantalum	TMC8A1C105MTR	1			
C132	CU3035	Chip C.	C1608JB1H102KT-AS	1			
C133	CU3005	Chip C.	C1608CH1H040CT-AS	1			
C134	CU3042	Chip C.	C1608JB1H392KT-NS	1			
C135	CU3044	Chip C.	C1608JB1H562KT-NS	1			
C137	CU3017	Chip C.	C1608CH1H330JT-AS	1			
C138	CS0049	Chip tantalum	TMC8A1C105MTR	1			
C139	CU3017	Chip C.	C1608CH1H330JT-AS	1			
C140	CU3017	Chip C.	C1608CH1H330JT-AS	1			
C141	CU3111	Chip C.	C1608JB1C104KT-N	1			
C142	CU3111	Chip C.	C1608JB1C104KT-N	1			
C143	CU3111	Chip C.	C1608JB1C104KT-N	1			
C144	CU3047	Chip C.	C1608JB1H103KT-N	1			
C145	CU3003	Chip C.	C1608CH1H020CT-AS	1			
C146	CE0339	Electrolytic C.	16MV 10SWB+TS	1			
C148	CU3017	Chip C.	C1608CH1H330JT-AS	1			
C149	CU3017	Chip C.	C1608CH1H330JT-AS	1			
C150	CU3005	Chip C.	C1608CH1H040CT-AS	1			
C151	CU3047	Chip C.	C1608JB1H103KT-N	1			
C152	CE0339	Electrolytic C.	16MV 10SWB+TS	1			
C153	CU3035	Chip C.	C1608JB1H102KT-AS	1			
C154	CU3035	Chip C.	C1608JB1H102KT-AS	1			
C155	CU3007	Chip C.	C1608CH1H060CT-A	1			
C156	CU3047	Chip C.	C1608JB1H103KT-N	1			
C157	CU3035	Chip C.	C1608JB1H102KT-AS	1			
C158	CU3013	Chip C.	C1608CH1H150JT-AS	1			
C159	CU3035	Chip C.	C1608JB1H102KT-AS	1			
C160	CE0339	Electrolytic C.	16MV 10SWB+TS	1			
C161	CU3111	Chip C.	C1608JB1C104KT-N	1			
C162	CU3035	Chip C.	C1608JB1H102KT-AS	1			
C165	CU3111	Chip C.	C1608JB1C104KT-N	1			
C167	CU3047	Chip C.	C1608JB1H103KT-N	1			
C168	CU3111	Chip C.	C1608JB1C104KT-N	1			
C169	CU3027	Chip C.	C1608CH1H221JT-AS	1			
C171	CU3111	Chip C.	C1608JB1C104KT-N	1			
C172	CU3035	Chip C.	C1608JB1H102KT-AS	1			

Ref. No.	Parts No.	Description	Parts Name	Qty			Ver
				DR-135	DR-235	DR-435	
ST0065	SP Holder	DR135		1	1	1	
ST0066	SP FITTING	DR135		1	1	1	
TG0034	SP Himelon	DR135		1	1	1	
UE0258	ANT Connector	FM-M.D.R-(4)		1	1	1	
YZ0131	Tape	#9110 12X1mm		60	60	60	
DS0388A		Model Name Plate		1	-	1	E,EG
DS0429		Model Name Plate		1	1	1	T,TG
PR0309	Label	CE-MARKLABEL DJG5E		2.2	-	2.2	E,EG
PR0451	Label	FCC Part 15 Seal		1	1	1	T,TG
PR0452	Label	FCC Home Use Seal		1	1	1	T,TG

Packing Parts

Ref. No.	Parts No.	Description	Parts Name	Qty			Ver
				DR-135	DR-235	DR-435	
HK0486	Package	Item Carton DR135		1		-	
HK0507	Package	Item Carton DR235T		-	1	-	T,TG
HK0508	Package	Item Carton DR435T		-	-	1	
HM0203	Carton Box	5PCS		0.2	0.2	0.2	
HU0099	P.MTL/Carton	FRONT DR605		1	1	1	
HU0159	P.MTL/Carton	Fixture		1	1	1	
HU0161	P.MTL/Carton	Fixture 5PCS		0.4	0.4	0.4	
PR0345	Label	T		3	3	3	T,TG
PT0004A	Label	SERIAL NO.FOR CARTON		2	2	2	

ACCESSORIES

Ref. No.	Parts No.	Description	Parts Name	Qty			Ver
				DR-135	DR-235	DR-435	
ADFM78	Bracket	DR130		1	1	1	
ADUA38	Power cable	R-B2.0X3M RECEPTE.15A		1	1	1	
EMSS53	Microphone			1	1	1	E,EG
EMSS56	Microphone			1	-	-	
EMSS57	Microphone	Remote control		-	1	1	T,TG
HP0009	Plastic bag	5X125X250(ADUA38)		1	1	1	
HP0035	Plastic bag	5X200X250(DR135)		1	1	1	
PH0009A		Registration Card		1	1	1	T,TG
PK0078		Schematic Diagram DR135		1	-	-	
PK0083		Schematic Diagram DR235		-	1	-	T,TG
PK0085		Schematic Diagram DR435		-	-	1	
PR0454	Label	Security Seal T		2	2	2	
PS0370	Manual	INSTRUCTION DR235T		1	1	1	
UX1259	Wire	SCR1		1	1	1	
UX1260	Wire	SCR2		1	1	1	

ACCESSORIES (SCREW SET)

Ref. No.	Parts No.	Description	Parts Name	Qty			Ver
				DR-135	DR-235	DR-435	
AA0013	Screw	M5+20 Fe/Zn		4	4	4	
AE0012	Screw	HEXHD M4+8 Fe/B.Zn		4	4	4	
AJ0003	Screw	T5+20 Fe/Zn		4	4	4	
AJ0003	Nut	N5x0.8 Fe/Zn		4	4	4	
AZ0009	Washer	5x9.2x1.3 Fe/Zn		4	4	4	
AZ0010	Washer	5x12x0.8 Fe/Zn		4	4	4	
EF0005	Fuse	FGBO 125V 15A		2	2	2	
FM0079Z	SPANNER	DR130		1	1	1	
HP0006	Plastic bag	5X90X170		1	1	1	
YZ0121	Tape	Tape 10mm		2	2	2	

TNC (EJ41U) Packing Parts

Ref.No.	Parts No.	Description	Parts Name	Qty
FD0001	Floppy-Disc	(WIN2HD)		1
FF0034	VELCRO	B		1
FG0040	Cushion			1
HK0487	Package	Item Carton EJ41U		1
HP0029	Plastic bag	5X100X100		1
HP0040	Plastic bag	8X130X200		1
PF0061	SHEET	EJ41U		1
PR0449	Label	EJ41U		1
PS0354	Manual	INSTRUCTION EJ41U		1
PS0355	Manual	INST-DISC EJ41U		1
UZ0030	Plug	MP-013LC 3.5mm Plug		1

DR-135 ADJUSTMENT

1) Adjustment Spot

Power Supply Voltage 13.8 V

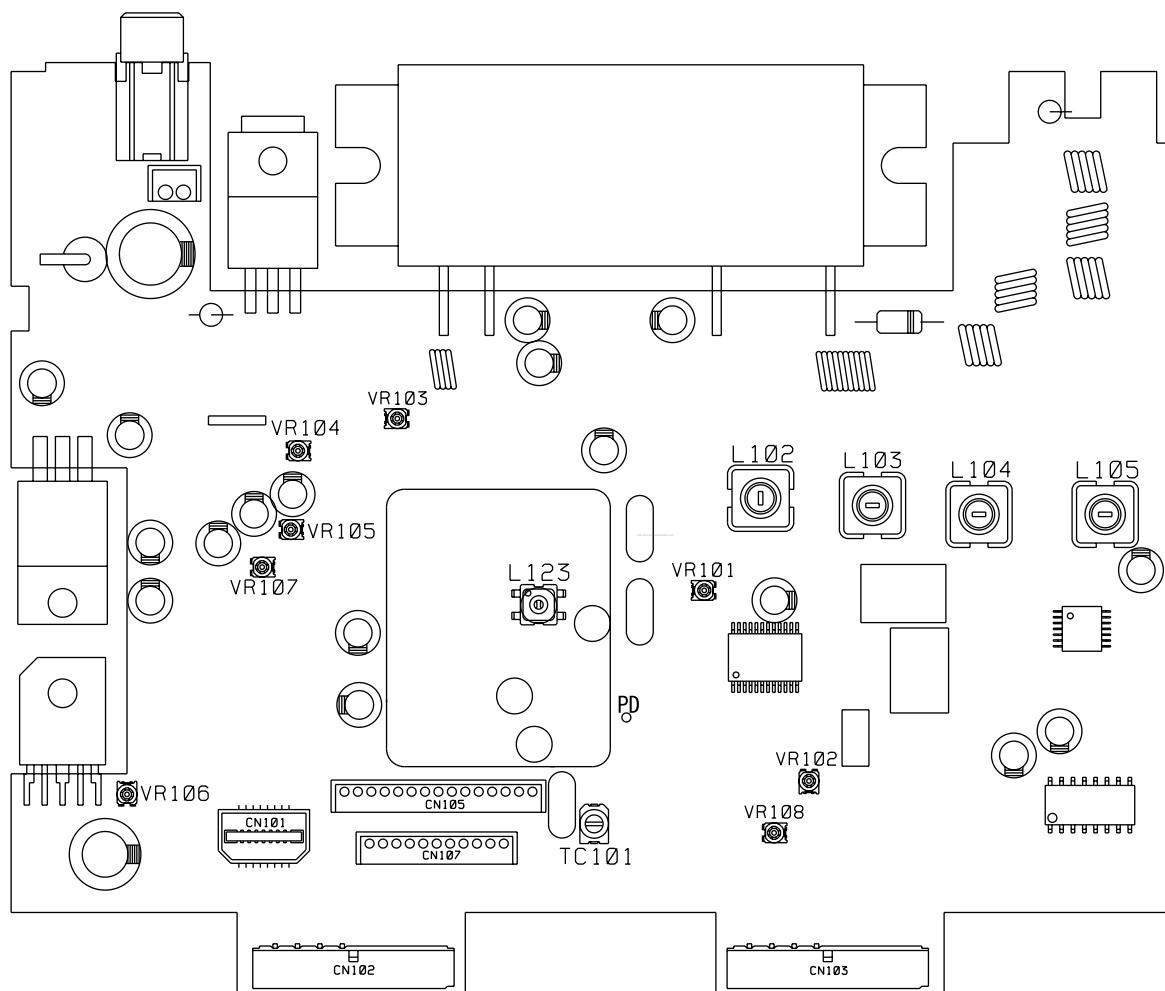
Output of SSG is all EMF indication

If without instruction, WIDE mode

If without instruction, SSG output is MOD 1KHz WIDE DEV 3.5KHz/DEV, NARROW DEV 1.75KHz/DEV

Standard Modulation is also based above.

Speaker load is 8Ω and Output is 50~100 mV.



Attention: Don't set the variable resistor into its open position.

2) VCO and RX Adjustment Specification

ITEM	CONDITION	UNIT	ADJ.SPOT	ADJUSTING METHOD
Adjustment Frequency	145.90MHz TX	MAIN	TC101	Adjust so that Tx Frequency becomes within 145.90MHz±100Hz
VCO Adjustment	136.00MHz RX	MAIN	L123	Adjust so that PD voltage becomes 1.5V
VCO Confirmation	173.99MHz RX	MAIN		Confirm if PD voltage becomes less than 7.3 V
Rx Signal Sensitivity Adjustment	146.05MHz 136.05MHz 146.05MHz 173.95MHz	MAIN	L105, L104 L103, L102	Repeatedly adjust so that the Rx sensitivity becomes in maximum. Confirm: At -7dBu SINAD more than 12dB At -8dBu SINAD more than 12dB At -6dBu SINAD more than 12dB
Squelch Adjustment	146.05MHz SSG OFF Indication 01	MAIN	VR101	Adjust so that the squelch stops at perfectly close location
S Meter Adjustment	146.05MHz SSG20dBu 1KHz 3.5KHz/DEV	MAIN	VR102	Adjust so that all the indicator appears

3) Tx Adjustment Specification

ITEM	CONDITION	UNIT	ADJ.SPOT	ADJUSTING METHOD
HI POWER Adjustment	146.00MHz HI POWER	MAIN	VR103	Adjust to 50.0±1.0W
MID POWER Adjustment	146.00MHz MID POWER	MAIN	VR104	Adjust to 10.0±1.0W
LOW POWER Confirmation	146.00MHz LOW POWER	MAIN		Confirm if it becomes 4.0 ±1.0W
Maximum Deviation Adjustment	146.00MHz MOD 1KHz40mVemf WIDE	MAIN	VR107	4.5±0.1KHz/DEV
Maximum Deviation Adjustment	146.00MHz MOD 1KHz40mVemf NARROW	MAIN	VR105	2.2±0.1KHz/DEV
Mic Gain Adjustment	146.00MHz MOD 1KHz4mVemf WIDE	MAIN	VR106	3.0±0.1KHz/DEV
CTCSS Modulation Level Confirmation	146.00MHz 88.5Hz	MAIN		800±200Hz/DEV 3KHz LPF ON
DCS Modulation Level Adjustment	146.00MHz 255 Code	MAIN	VR108	800±50Hz/DEV 3KHz LPF ON
1750Hz Modulation Level Confirmation	146.00MHz 1750Hz	MAIN		3.0±0.5KHz/DEV
DTMF Modulation Level Confirmation	146.00MHz DTMF① Press the V/M key during TX	MAIN		3.0±0.5KHz/DEV

4) Rx Test Specification

TEST ITEM	CONDITION	ADJ STANDARD	TEST STANDARD	NOTE
RX Sensitivity	136.05MHz	Less than -7dBu	Less than -6dBu	12dBSINAD
	146.05MHz	Less than -8dBu	Less than -7dBu	
	173.95MHz	Less than -6dBu	Less than -5dBu	
	146.05MHz NARROW	Less than -8dBu	Less than -7dBu	
	135.05MHz	Less than 9dBu	Less than 10dBu	AM 10dB S/N
RX Distortion	WIDE	Less than 4%	Less than 5%	SSG OUT PUT 30dBu
	NARROW			
RX S/N	WIDE	More than 40dB	More than 38dB	SSG OUT PUT 30dBu 0.3~3KHzBPF OFF
	NARROW	More than 34dB	More than 32dB	
Squelch Sensitivity	146.05MHz	Squelch Open	Squelch Open	SSG Output -10dBu SSG Output OFF
	Indication 02	Squelch Close	Squelch Close	
S Meter	146.05MHz 1KHz 3.5KHz/DEV	All appears at 20dBu	All appears at 25dBu	Decrease SSG level and decrease S Meter level
AF Output	146.05MHz	More than 2W	More than 2W	SSG Output 30dBu
CTCSS Sensitivity	WIDE	Open at 500Hz/DEV	Open at 500Hz/DEV	SSG Output 0dBu 88.5Hz
	NARROW	Open at 250Hz/DEV	Open at 250Hz/DEV	
DCS Sensitivity	WIDE	Opens when Test Equipment is in Tx	Opens when Test Equipment is in Tx	255 code
	NARROW	Opens when Test Equipment is in Tx	Opens when Test Equipment is in Tx	255 code
Drain Current	146.05MHz	Less than 0.65A	Less than 0.65A	MAX VR
Power Off Current	146.05MHz	Less than 10mA	Less than 10mA	Power Off
Howling	146.05MHz	Don't occur	Don't occur	SSG Output 60dBu MOD OFF MAX VR

5) Tx Test Specification

TEST ITEM	CONDITION	ADJ STANDARD	TEST STANDARD	NOTE
TX Output HI POWER	136.00MHz 144.00MHz 146.00MHz 148.00MHz 173.99MHz	More than 33W 50±1W More than 33W	More than 33W 50±3W 50±3W 50±3W More than 33W	← TA,TAG ONLY ← T,TG ONLY ← TA,TAG ONLY
TX Output MID POWER	146.00MHz	10±1W	10 ±2W	
TX Output LOW POWER	146.00MHz	4±1W	3~6W	
Drain Current	146.00MHz	Less than 10A	Less than 11A	
Frequency Deviation	146.00MHz	Within ±0.3KHz	Within±0.5KHz	
Spurious	136.00MHz 144.00MHz 146.00MHz 148.00MHz 173.99MHz	More than 60dB More than 65dB More than 65dB More than 65dB More than 60dB	More than 55dB More than 60dB More than 60dB More than 60dB More than 55dB TA,TAG ONLY	M and L standard power is also the same as of H power level
Modulation Level	WIDE 146.00MHz	3.0±0.1KHz/DEV 4.5±0.1KHz/DEV	3.0±0.2KHz/DEV 4.5±0.2KHz/DEV	MIC IN 4mVemf MIC IN 40mVemf
	NARROW 146.00MHz	2.2±0.1KHz/DEV	2.2±0.2KHz/DEV	MIC IN 40mVemf
CTCSS Modulation Level	WIDE 146.00MHz	800±200Hz/DEV	800±200Hz/DEV	88.5Hz 3KHz LPF ON
DCS Modulation Level	WIDE 146.00MHz	800±200Hz/DEV	800±200Hz/DEV	Code 255 3KHz LPF ON
	NARROW 146.00MHz	450±100Hz/DEV	450±100Hz/DEV	Code 255 3KHz LPF ON
1750Hz Modulation Level	WIDE 146.00MHz	3.0±0.5KHz/DEV	3.0±0.5KHz/DEV	
DTMF Modulation Level	WIDE 146.00MHz	3.0±0.5KHz/DEV	3.0±0.5KHz/DEV	Press the V/M key during TX
Modulation Distortion	146.00MHz	Less than 3%	Less than 4%	
TX S/N	WIDE	More than 40dB	More than 38dB	0.3 ~ 3KHz BPF ON
	NARROW	More than 34dB	More than 32dB	

DR-235 ADJUSTMENT

1) Adjustment Spot

Power Supply Voltage 13.8 V

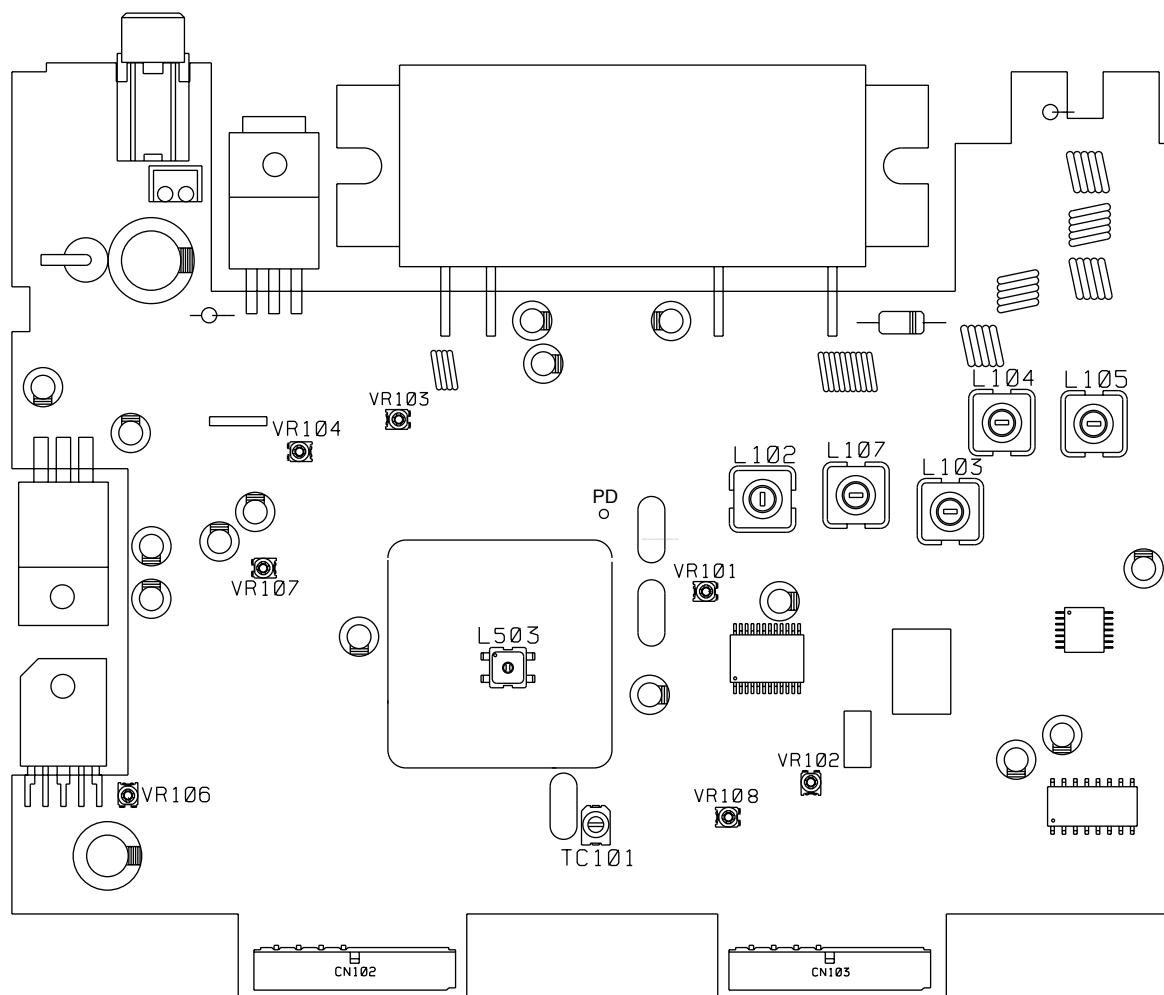
Output of SSG is all EMF indication

If without instruction, WIDE mode

If without instruction, SSG output is MOD 1KHz WIDE DEV 3.5KHz/DEV, NARROW DEV 1.75KHz/DEV

Standard Modulation is also based above.

Speaker load is 8Ω and Output is 50~100 mV.



Attention: Don't set the variable resistor into its open position.

2) VCO and RX Adjustment Specification

ITEM	CONDITION	UNIT	ADJ.SPOT	ADJUSTING METHOD
Adjustment Frequency	224.90MHz TX	MAIN	TC101	Adjust so that Tx Frequency becomes within 224.90MHz±100Hz
VCO Adjustment	225.00MHz RX	VCO	L503	Adjust so that PD voltage becomes 2.2V
VCO Confirmation	224.99MHz TX	VCO		Confirm if PD voltage becomes less than 6.2 V
Rx Signal Sensitivity Adjustment	223.50MHz 216.05MHz 223.50MHz 250.05MHz	MAIN	L105, L104 L103, L107 L102	Repeatedly adjust so that the Rx sensitivity becomes in maximum. Confirm: At -7dBu SINAD more than 12dB At -8dBu SINAD more than 12dB At -3dBu SINAD more than 12dB
Squelch Adjustment	223.50MHz SSG OFF Indication 01	MAIN	VR101	Adjust so that the squelch stops at perfectly close location
S Meter Adjustment	223.50MHz SSG20dBu 1KHz 3.5KHz/DEV	MAIN	VR102	Adjust so that all the indicator appears

3) Tx Adjustment Specification

ITEM	CONDITION	UNIT	ADJ.SPOT	ADJUSTING METHOD
HI POWER Adjustment	223.50MHz HI POWER	MAIN	VR103	Adjust to 25.0±1.0W
MID POWER Adjustment	223.50MHz MID POWER	MAIN	VR104	Adjust to 10.0±1.0W
LOW POWER Confirmation	223.50MHz LOW POWER	MAIN		Confirm if it becomes 4.5±1.0W
Maximum Deviation Adjustment	223.50MHz MOD 1KHz40mVemf WIDE	MAIN	VR107	4.5±0.1KHz/DEV
Maximum Deviation Adjustment	223.50MHz MOD 1KHz40mVemf NARROW	MAIN	VR105	2.2±0.1KHz/DEV
Mic Gain Adjustment	223.50MHz MOD 1KHz4mVemf WIDE	MAIN	VR106	3.0±0.1KHz/DEV
CTCSS Modulation Level Confirmation	223.50MHz 88.5Hz	MAIN		800±300Hz/DEV 3KHz LPF ON
DCS Modulation Level Adjustment	223.50MHz 255 Code	MAIN	VR108	800±100Hz/DEV 3KHz LPF ON
1750Hz Modulation Level Confirmation	223.50MHz 1750Hz	MAIN		3.0±0.5KHz/DEV
DTMF Modulation Level Confirmation	223.50MHz DTMF① Press the V/M key during TX	MAIN		3.0±0.5KHz/DEV

4) Rx Test Specification

TEST ITEM	CONDITION	ADJ STANDARD	TEST STANDARD	NOTE
RX Sensitivity	216.05MHz	Less than -7dBu	Less than -6dBu	12dBSINAD
	223.50MHz	Less than -8dBu	Less than -7dBu	
	250.05MHz	Less than -3dBu	Less than -2dBu	
	223.50MHz NARROW	Less than -8dBu	Less than -7dBu	
	223.50MHz	Less than +6dBu	Less than +7dBu	AM 10dB S/N
RX Distortion	WIDE	Less than 4%	Less than 5%	SSG OUT PUT 30dBu
	NARROW			
RX S/N	WIDE	More than 40dB	More than 38dB	SSG OUT PUT 30dBu 0.3~3KHzBPF OFF
	NARROW	More than 34dB	More than 32dB	
Squelch Sensitivity	223.50MHz	Squelch Open	Squelch Open	SSG Output -10dBu
	Indication 02	Squelch Close	Squelch Close	SSG Output OFF
S Meter	223.50MHz 1KHz 3.5KHz/DEV	All appears at 20dBu	All appears at 25dBu	Decrease SSG level and decrease S Meter level
AF Output	223.50MHz	More than 2W	More than 2W	SSG Output 30dBu
CTCSS Sensitivity	WIDE	Open at 500Hz/DEV	Open at 500Hz/DEV	SSG Output 0dBu 88.5Hz
	NARROW	Open at 250Hz/DEV	Open at 250Hz/DEV	
DCS Sensitivity	WIDE	Opens when Test Equipment is in Tx	Opens when Test Equipment is in Tx	255 code
	NARROW	Opens when Test Equipment is in Tx	Opens when Test Equipment is in Tx	255 code
Drain Current	223.50MHz	Less than 0.65A	Less than 0.65A	MAX VR
Power Off Current	223.50MHz	Less than 10mA	Less than 10mA	Power Off
Howling	223.50MHz	Don't occur	Don't occur	SSG Output 60dBu MOD OFF MAX VR

5) Tx Test Specification

TEST ITEM	CONDITION	ADJ STANDARD	TEST STANDARD	NOTE
TX Output HI POWER	222.00MHz	25±1W	25±3W	
	223.50MHz	25±1W	25±3W	
	224.99MHz	25±1W	25±3W	
TX Output MID POWER	223.50MHz	10±1W	10±2W	
TX Output LOW POWER	223.50MHz	4.5±1W	3~6W	
Drain Current	223.50MHz	Less than 7A	Less than 8A	
Frequency Deviation	223.50MHz	Within±0.5KHz	Within±0.7KHz	
Spurious	222.00MHz 223.50MHz 224.99MHz	More than 65dB More than 65dB More than 65dB	More than 60dB More than 60dB More than 60dB	M and L standard power is also the same as of H power level
Modulation Level	WIDE 223.50MHz	3.0±0.1KHz/DEV 4.5±0.1KHz/DEV	3.0±0.2KHz/DEV 4.5±0.2KHz/DEV	MIC IN 4mVemf MIC IN 40mVemf
	NARROW 223.50MHz	2.2±0.1KHz/DEV	2.2±0.2KHz/DEV	MIC IN 40mVemf
CTCSS Modulation Level	WIDE 223.50MHz	800±200Hz/DEV	800±200Hz/DEV	88.5Hz 3KHz LPF ON
DCS Modulation Level	WIDE 223.50MHz	800±100Hz/DEV	800±200Hz/DEV	Code 255 3KHz LPF ON
	NARROW 146.00MHz	500±100Hz/DEV	450±100Hz/DEV	Code 255 3KHz LPF ON
1750Hz Modulation Level	WIDE 146.00MHz	3.0±0.5KHz/DEV	3.0±0.5KHz/DEV	
DTMF Modulation Level	WIDE 146.00MHz	3.0±0.5KHz/DEV	3.0±0.5KHz/DEV	Press the V/M key during TX
Modulation Distortion	146.00MHz	Less than 3%	Less than 4%	
TX S/N	WIDE	More than 40dB	More than 38dB	0.3~3KHz BPF ON
	NARROW	More than 34dB	More than 32dB	

DR-435 ADJUSTMENT

1) Adjustment Spot

Power Supply Voltage 13.8 V

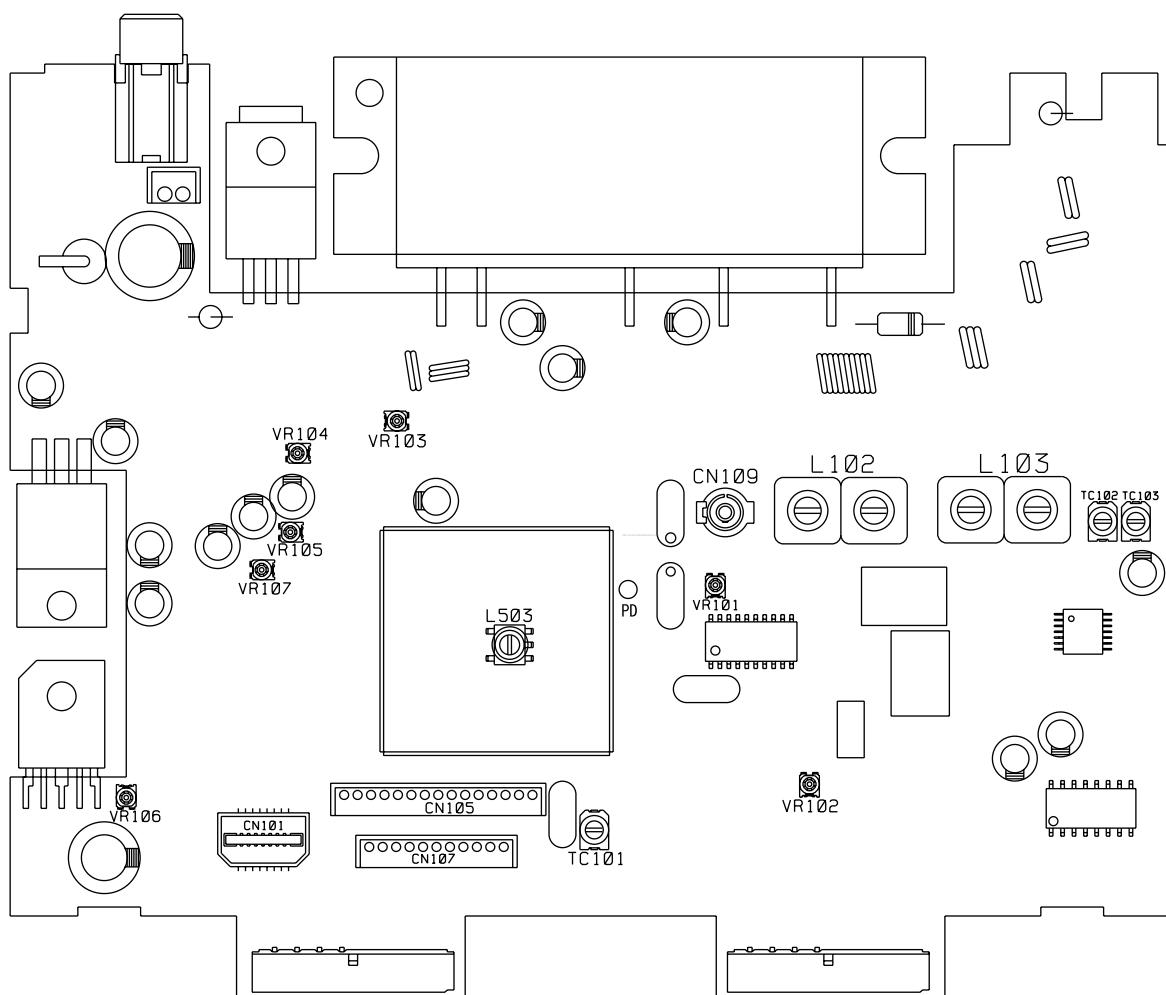
Output of SSG is all EMF indication

If without instruction, WIDE mode

If without instruction, SSG output is MOD 1KHz WIDE DEV 3.5KHz/DEV, NARROW DEV 1.75KHz/DEV

Standard Modulation is also based above.

Speaker load is 8Ω and Output is 50~100 mV.



Attention: Don't set the variable resistor into its open position.

2) VCO and RX Adjustment Specification

ITEM	CONDITION	UNIT	ADJ.SPOT	ADJUSTING METHOD
Adjustment Frequency	439.00MHz TX	MAIN	TC101	Adjust so that Tx Frequency becomes within 439.00MHz±100Hz
VCO Adjustment	425.00MHz RX	VCO	L503	Adjust so that PD voltage becomes 1.7V
VCO Confirmation	511.95MHz RX	VCO		Confirm if PD voltage becomes less than 9.0 V
Rx Signal Sensitivity Adjustment	440.05MHz 430.05MHz 440.05MHz 450.05MHz	MAIN	TC103 TC102 L103, L102	<p>It is a tracking generator from an antenna connector. -30dBm is inputted. And when CN109 is seen with a spectrum analyzer, by the maximum gain, it becomes as it is shown in the following figure, and appearance adjustment is carried out.</p> <p>At -7.5dB SINAD more than 12dB At -7.5dB SINAD more than 12dB At -7.5dB SINAD more than 12dB</p>
Squelch Adjustment	440.05MHz SSG OFF Indication 01	MAIN	VR101	Adjust so that the squelch stops at perfectly close location
S Meter Adjustment	440.05MHz SSG20dBu 1KHz 3.5KHz/DEV	MAIN	VR102	Adjust so that all the indicator appears

3) Tx Adjustment Specification

ITEM	CONDITION	UNIT	ADJ.SPOT	ADJUSTING METHOD
HI POWER Adjustment	440.00MHz HI POWER	MAIN	VR103	Adjust to $35.0 \pm 1.0\text{W}$
MID POWER Adjustment	440.00MHz MID POWER	MAIN	VR104	Adjust to $10.0 \pm 1.0\text{W}$
LOW POWER Confirmation	440.00MHz LOW POWER	MAIN		Confirm if it becomes $5.0 \pm 1.0\text{W}$
Maximum Deviation Adjustment	440.00MHz MOD 1KHz40mVemf WIDE	MAIN	VR107	$4.5 \pm 0.1\text{KHz/DEV}$
Maximum Deviation Adjustment	440.00MHz MOD 1KHz40mVemf NARROW	MAIN	VR105	$2.2 \pm 0.1\text{KHz/DEV}$
Mic Gain Adjustment	440.00MHz MOD 1KHz4mVemf WIDE	MAIN	VR106	$3.0 \pm 0.1\text{KHz/DEV}$
CTCSS Modulation Level Confirmation	440.00MHz 88.5Hz	MAIN		$800 \pm 200\text{Hz/DEV}$ 3Khz LPF ON
DCS Modulation Level Confirmation	440.00MHz 255 Code	MAIN		$800 \pm 200\text{Hz/DEV}$ 3Khz LPF ON
1750Hz Modulation Level Confirmation	440.00MHz 1750Hz	MAIN		$3.0 \pm 0.5\text{KHz/DEV}$
DTMF Modulation Level Confirmation	440.00MHz DTMF ① Press the V/M key during TX	MAIN		$3.0 \pm 0.5\text{KHz/DEV}$

4) Rx Test Specification

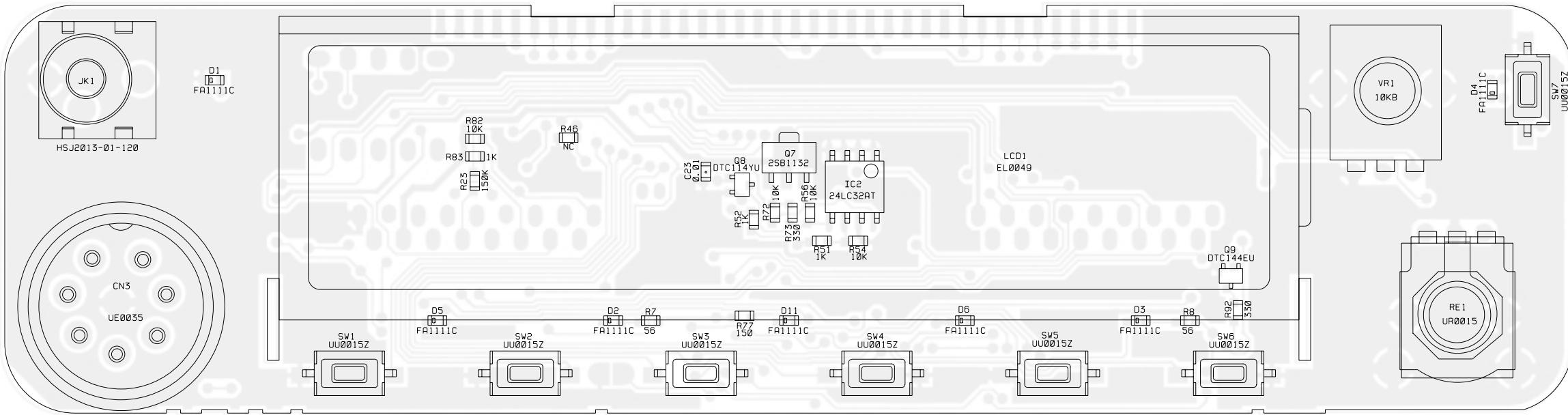
TEST ITEM	CONDITION	ADJ STANDARD	TEST STANDARD	NOTE
RX Sensitivity	350.05MHz	Less than -1dBu	Less than 0dBu	12dBSINAD
	430.05MHz	Less than -7.5dBu	Less than-6.5dBu	
	440.05MHz	Less than-7.5dBu	Less than-6.5dBu	
	450.05MHz	Less than-7.5dBu	Less than-6.5dBu	
	511.95MHz	Less than +1dBu	Less than +2dBu	
	440.05MHz NARROW	Less than-7.5dBu	Less than-6.5dBu	
RX Distortion	WIDE	Less than 4%	Less than 5%	SSG Output 40dBu
	NARROW			
RX S/N	WIDE	More than 40dB	More than 38dB	SSG Output 40dBu 0.3~3KHzBPF OFF
	NARROW	More than 34dB	More than 32dB	
Squelch Sensitivity	440.05MHz	Squelch Open	Squelch Open	SSG Output -10dBu SSG Output OFF
	Indication 02	Squelch Close	Squelch Close	
S Meter	440.05MHz 1KHz 3.5KHz/DEV	All appears at 20dBu	All appears at 25dBu	Decrease SSG level and decrease S Meter level
AF Output	440.05MHz	More than 2W	More than 2W	SSG Output 40dBu
CTCSS Sensitivity	WIDE	Open at 500Hz/DEV	Open at 500Hz/DEV	SSG Output 0dBu 88.5Hz
	NARROW	Open at 250Hz/DEV	Open at 250Hz/DEV	
DCS Sensitivity	WIDE	Opens when Test Equipment is in Tx	Opens when Test Equipment is in Tx	255 code
	NARROW	Opens when Test Equipment is in Tx	Opens when Test Equipment is in Tx	255 code
Drain Current	440.05MHz	Less than 0.7A	Less than 0.7A	MAX VR
Power Off Current	440.05MHz	Less than 10mA	Less than 10mA	Power Off
Howling	440.05MHz TP,TPG WIDE MODE OTHER NARROW MODE	Don't occur	Don't occur	SSG Output 60dBu MOD OFF MAX VR

5) Tx Test Specification

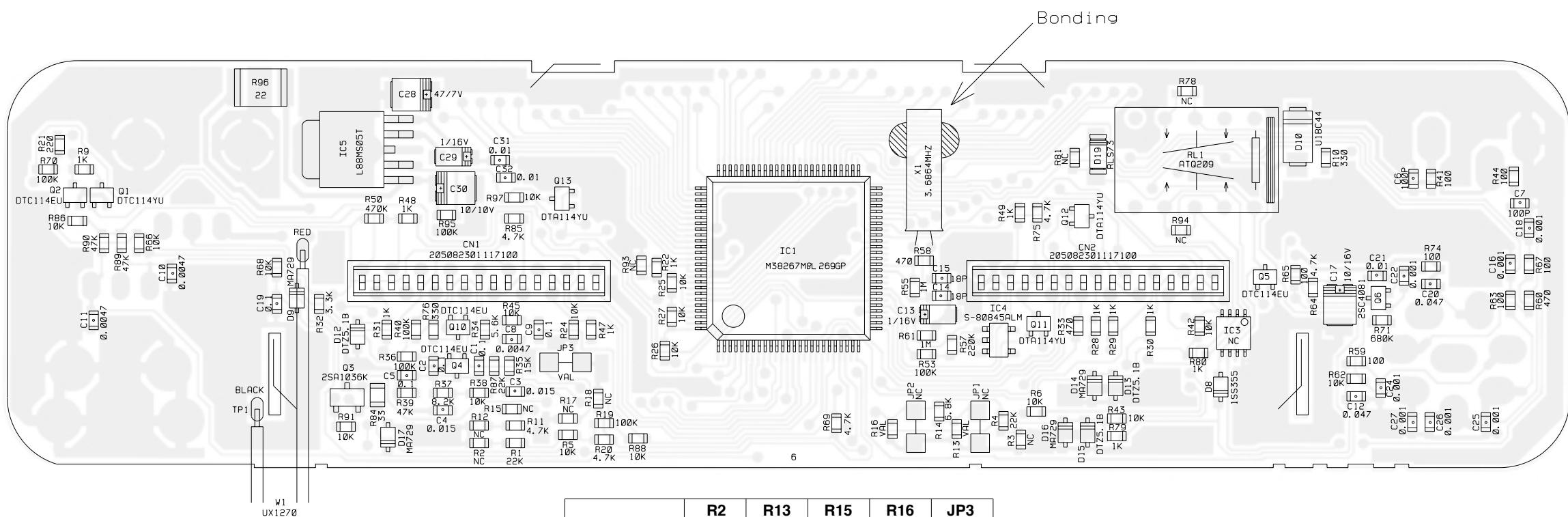
TEST ITEM	CONDITION	ADJ STANDARD	TEST STANDARD	NOTE
TX Output HI POWER	430.00MHz 440.00MHz 450.00MHz	35±1W	35±3W 35±3W 35±3W	← T,TG ONLY
TX Output MID POWER	440.00MHz	10±1W	10±2W	
TX Output LOW POWER	440.00MHz	5±1W	5±2W	
Drain Current	440.00MHz	Less than 9A	Less than 10A	
Frequency Deviation	440.00MHz	Within ±0.5KHz	Within ±1.0KHz	
Spurious	430.00MHz 440.00MHz 450.00MHz	More than 62dB More than 62dB More than 62dB	More than 60dB More than 60dB More than 60dB 450MHz T,TG ONLY	M and L standard power is also the same as of H power level
Modulation Level	WIDE 440.00MHz	3.0±0.1KHz/DEV 4.5±0.1KHz/DEV	3.0±0.2KHz/DEV 4.5±0.2KHz/DEV	MIC IN 4mVemf MIC IN 40mVemf
	NARROW 440.00MHz	2.2±0.1KHz/DEV	2.2±0.2KHz/DEV	MIC IN 40mVemf
CTCSS Modulation Level	WIDE 440.00MHz	800±200Hz/DEV	800±200Hz/DEV	88.5Hz 3KHz LPF ON
DCS Modulation Level	WIDE 440.00MHz	800±200Hz/DEV	800±200Hz/DEV	Code 255 3KHz LPF ON
	NARROW 440.00MHz	450±100Hz/DEV	450±100Hz/DEV	Code 255 3KHz LPF ON
1750Hz Modulation Level	WIDE 440.00MHz	3.0±0.5 KHz/DEV	3.0±0.5 KHz/DEV	
DTMF Modulation Level	WIDE 440.00MHz	3.0±0.5 KHz/DEV	3.0±0.5 KHz/DEV	Press the V/M key during TX
Modulation Distortion	440.00MHz	Less than 3%	Less than 4%	
TX S/N	WIDE	More than 40dB	More than 38dB	0.3~3KHz BPF ON
	NARROW	More than 34dB	More than 32dB	

PC BOARD VIEW

1) CPU Unit Side A DR-135 (UP 0400B) DR-235 (UP 0414) DR-435 (UP 0415)

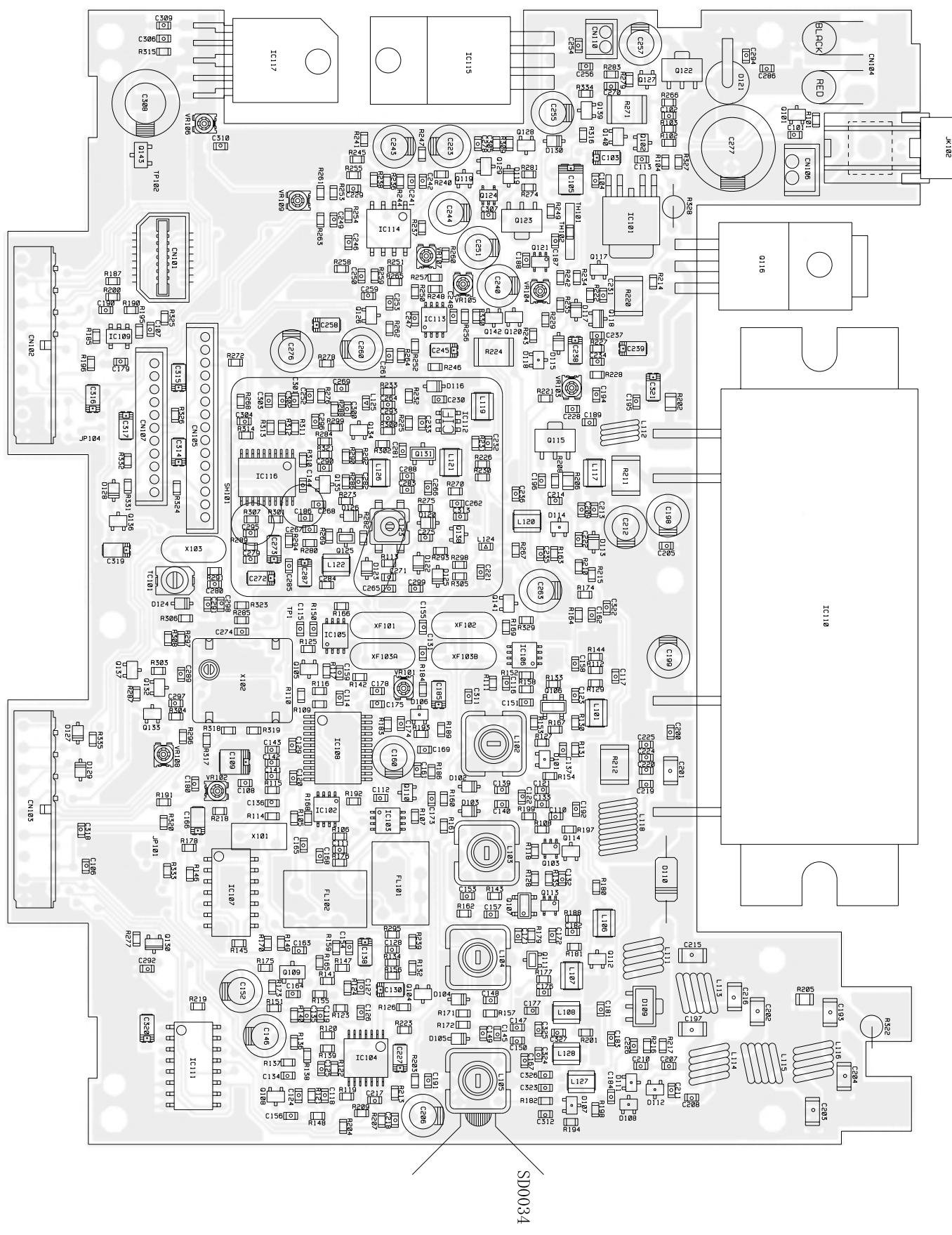


2) CPU Unit Side B DR-135 (UP 0400B) DR-235 (UP 0414) DR-435 (UP 0415)

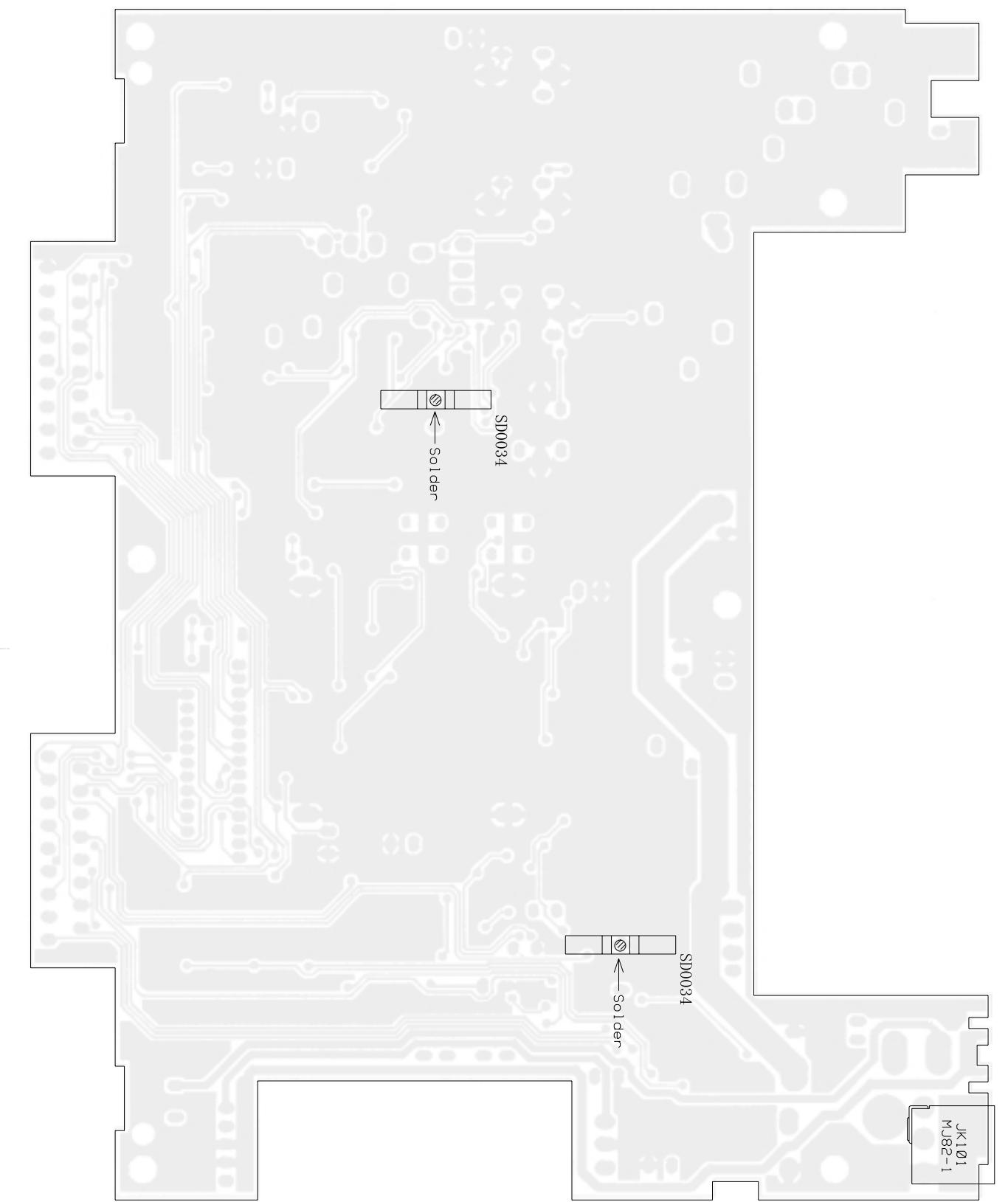


	R2	R13	R15	R16	JP3
DR135 T, TG	NC	NC	NC	0	JUMPER
DR135 E, EG	NC	0	NC	NC	JUMPER
DR135 TA, TAG	NC	NC	NC	0	NC
DR235 T, TG	0	NC	NC	0	JUMPER
DR435 T, TG	NC	NC	0	0	JUMPER
DR435 E, EG	NC	0	0	NC	JUMPER

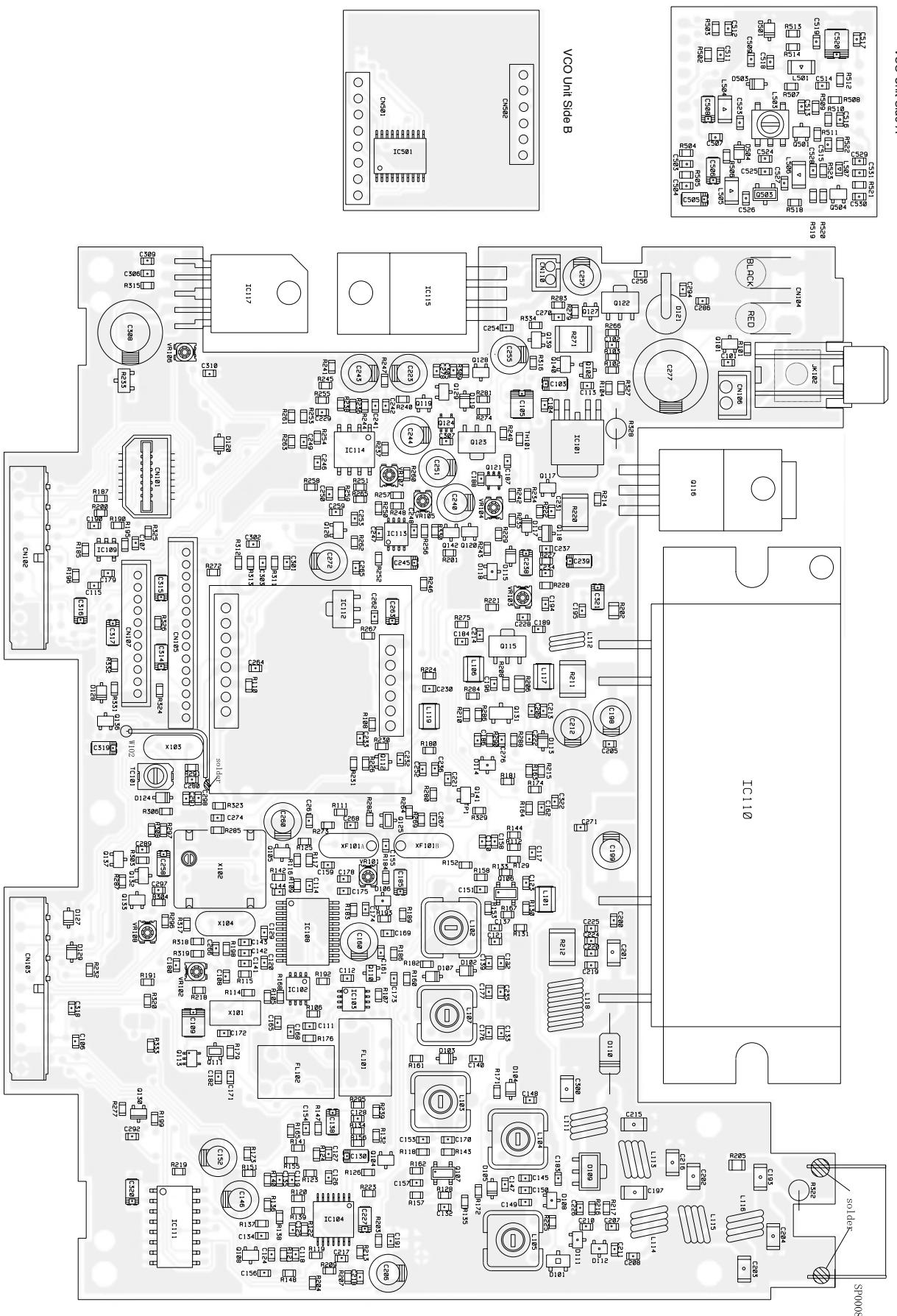
3) MAIN Unit Side A DR-135 (UP 0400B)



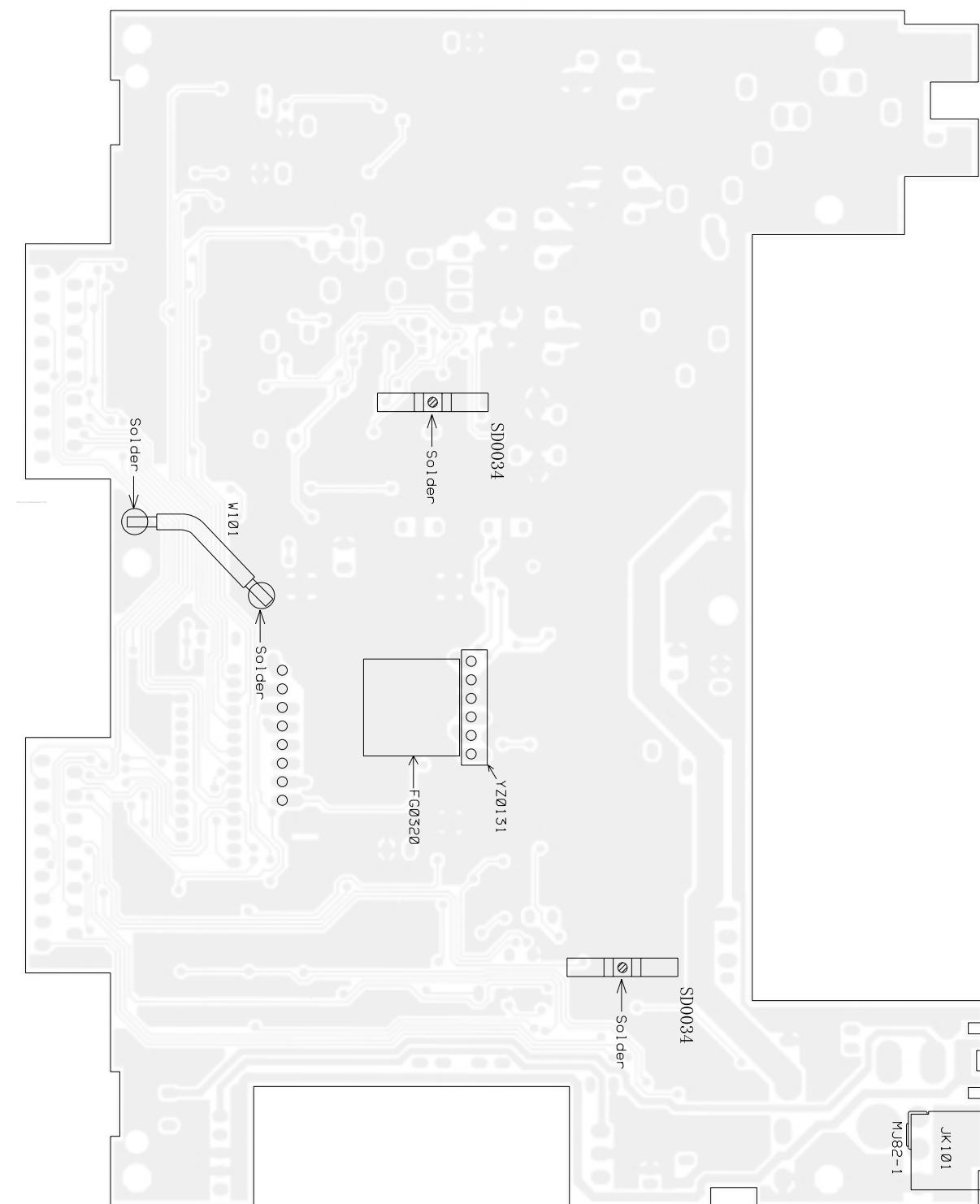
4) MAIN Unit Side B DR-135 (UP 0400B)



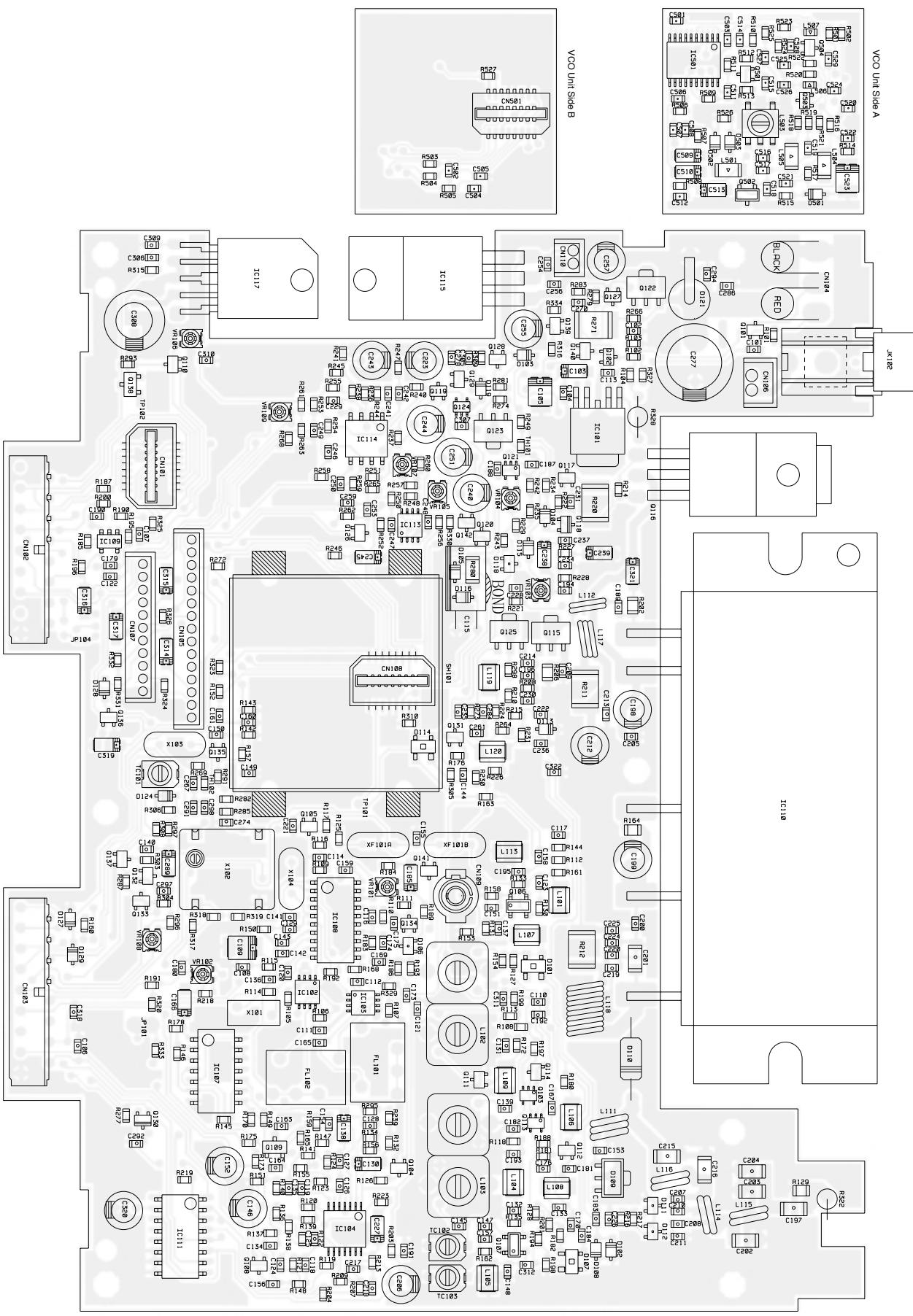
5) MAIN Unit Side A DR-235 (UP 0414)



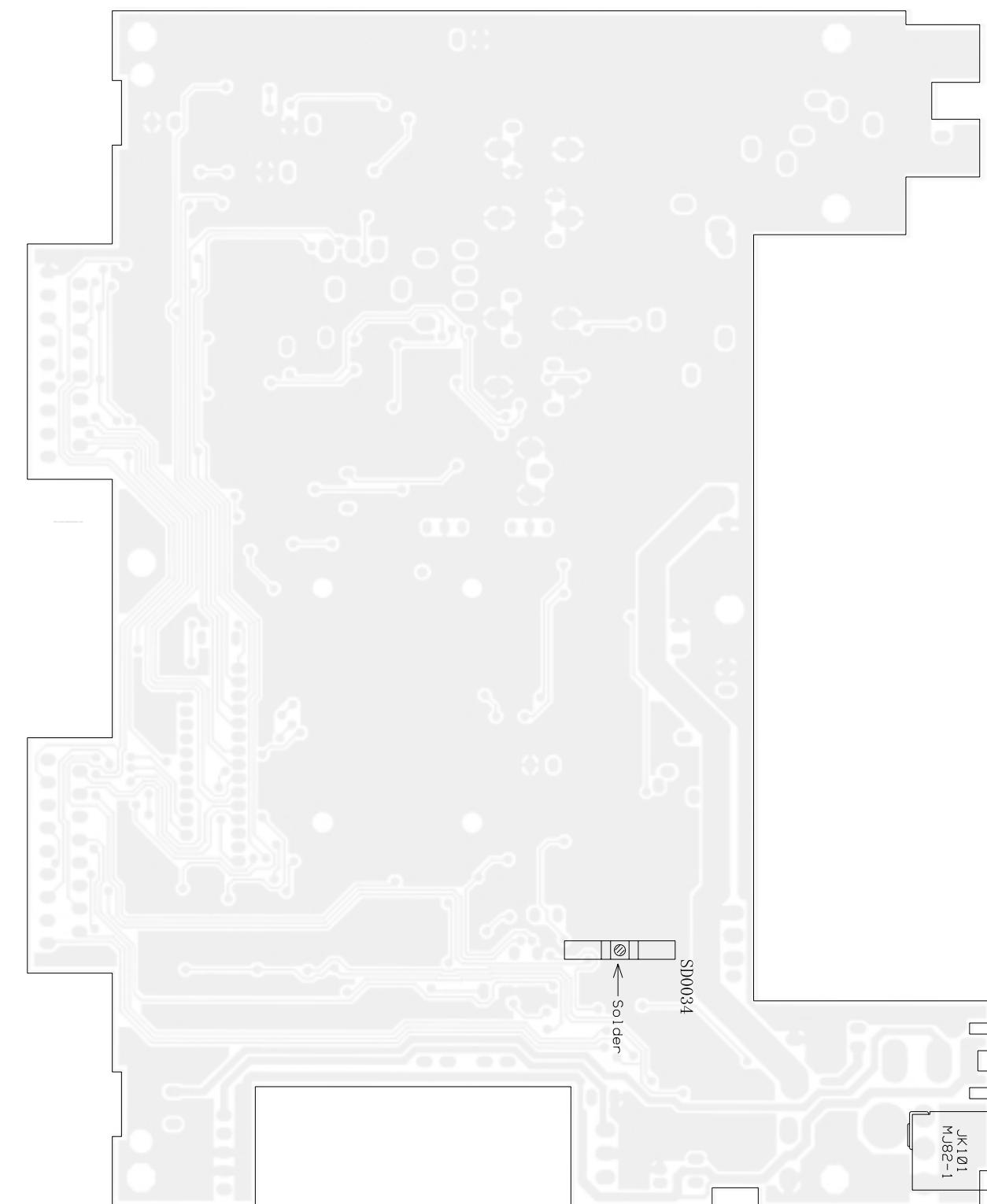
6) MAIN Unit Side B DR-235 (UP 0414)



7) MAIN Unit Side A DR-435 (UP 0415)

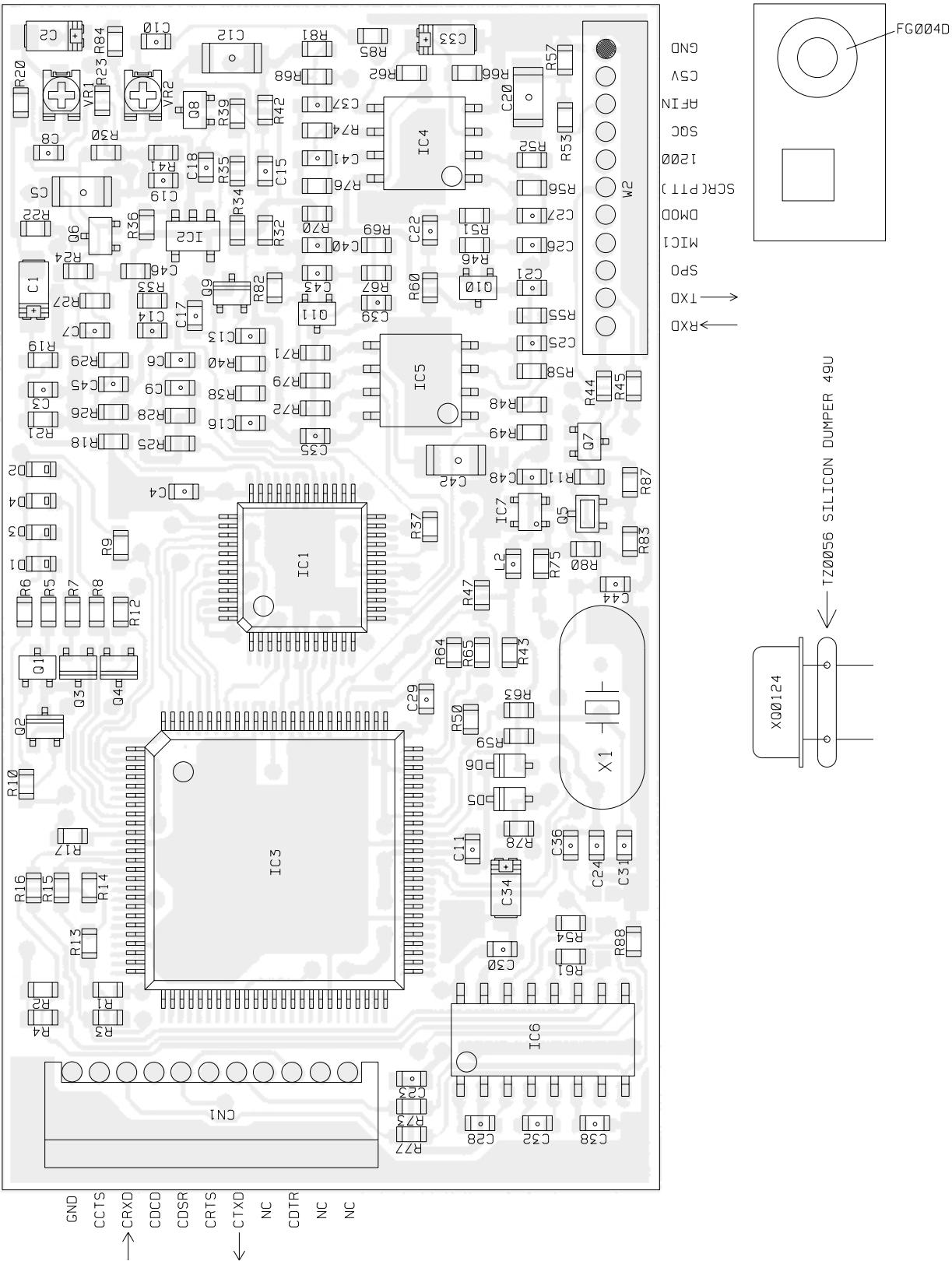


8) MAIN Unit Side B DR-435 (UP 0415)

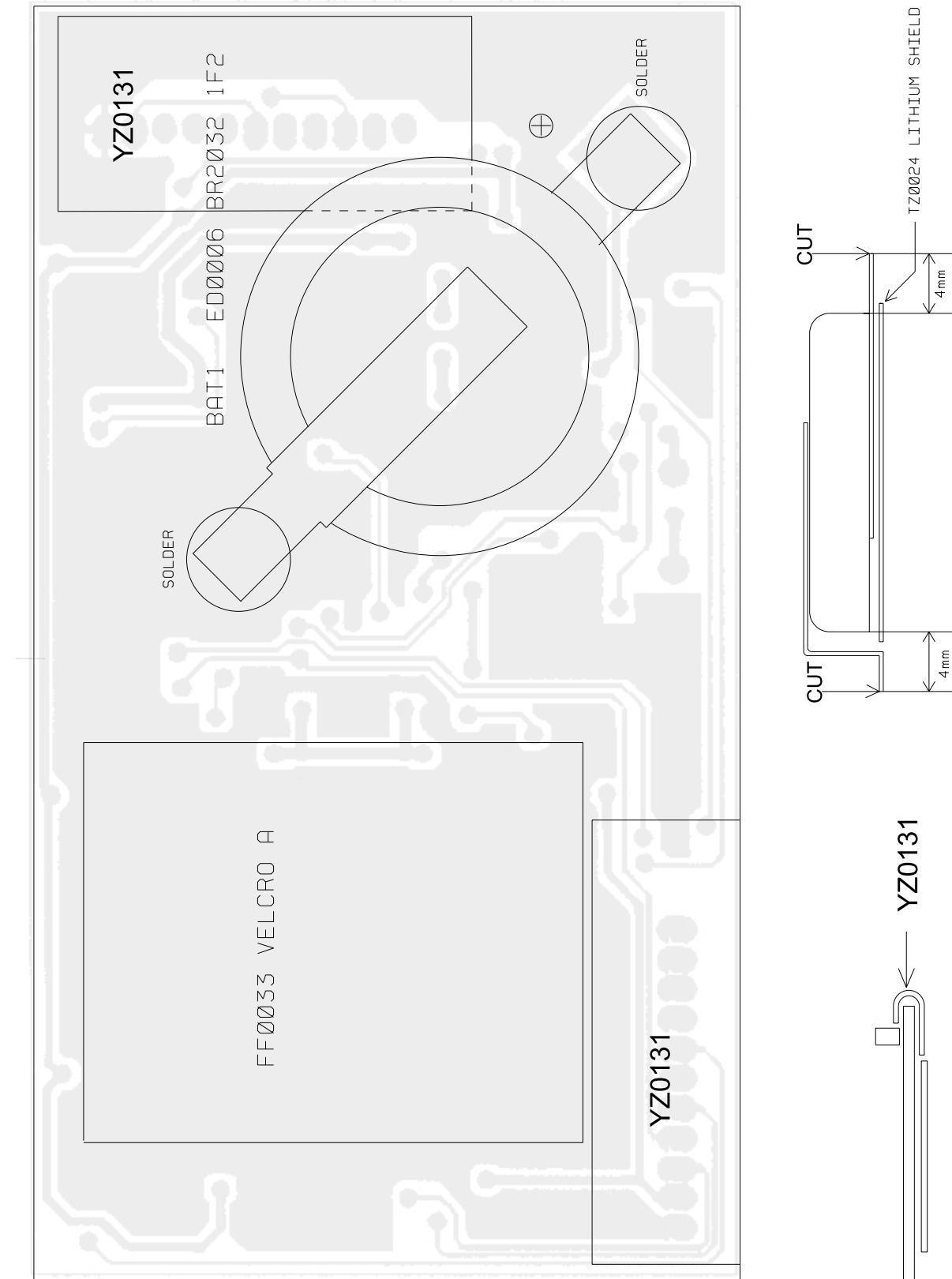


9) TNC Unit Side A (UP 0402) (DR-135TP only)

OPTION unit (EJ41U)

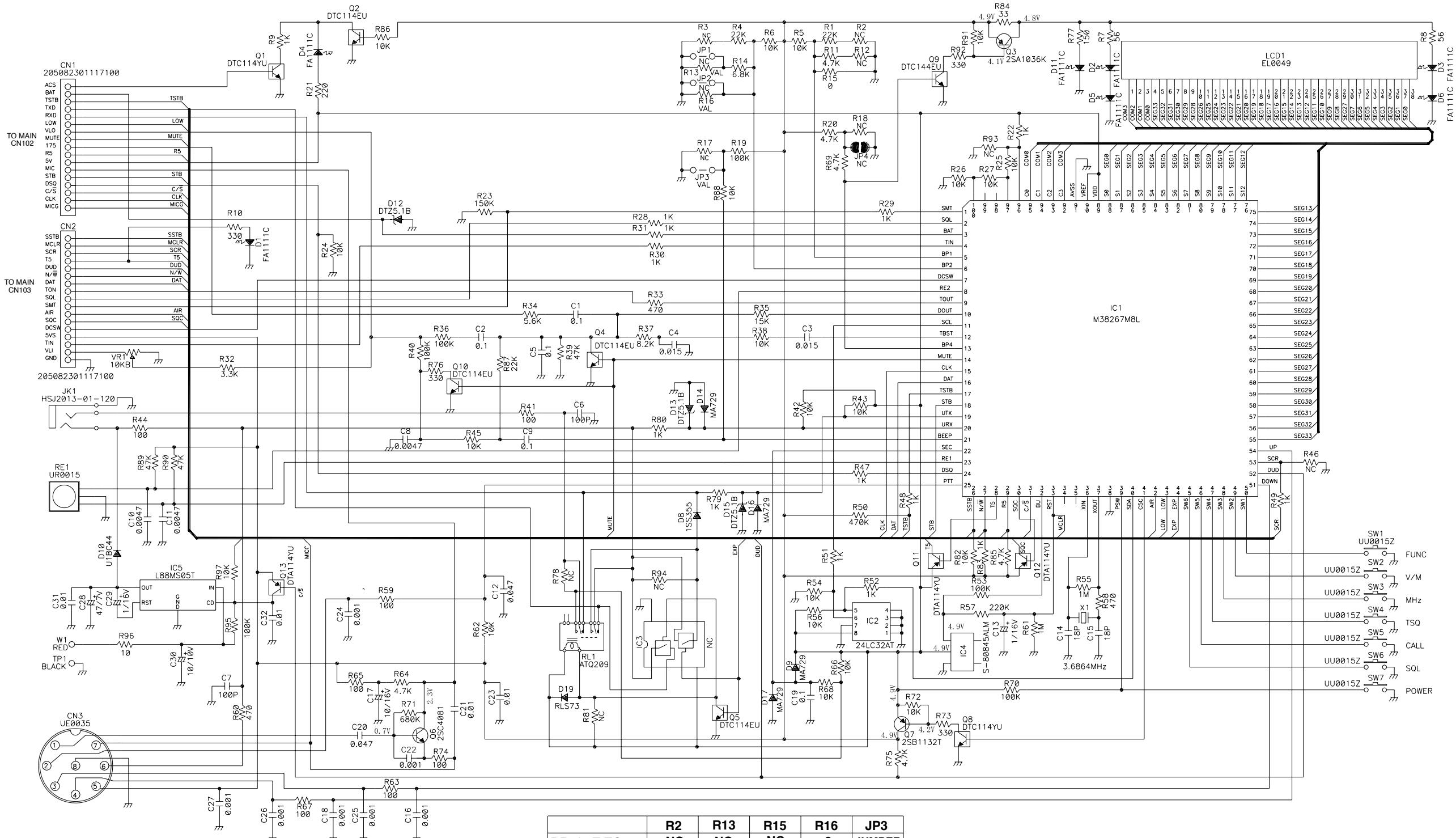


10) TNC Unit Side B (UP 0402) (DR-135TP only)

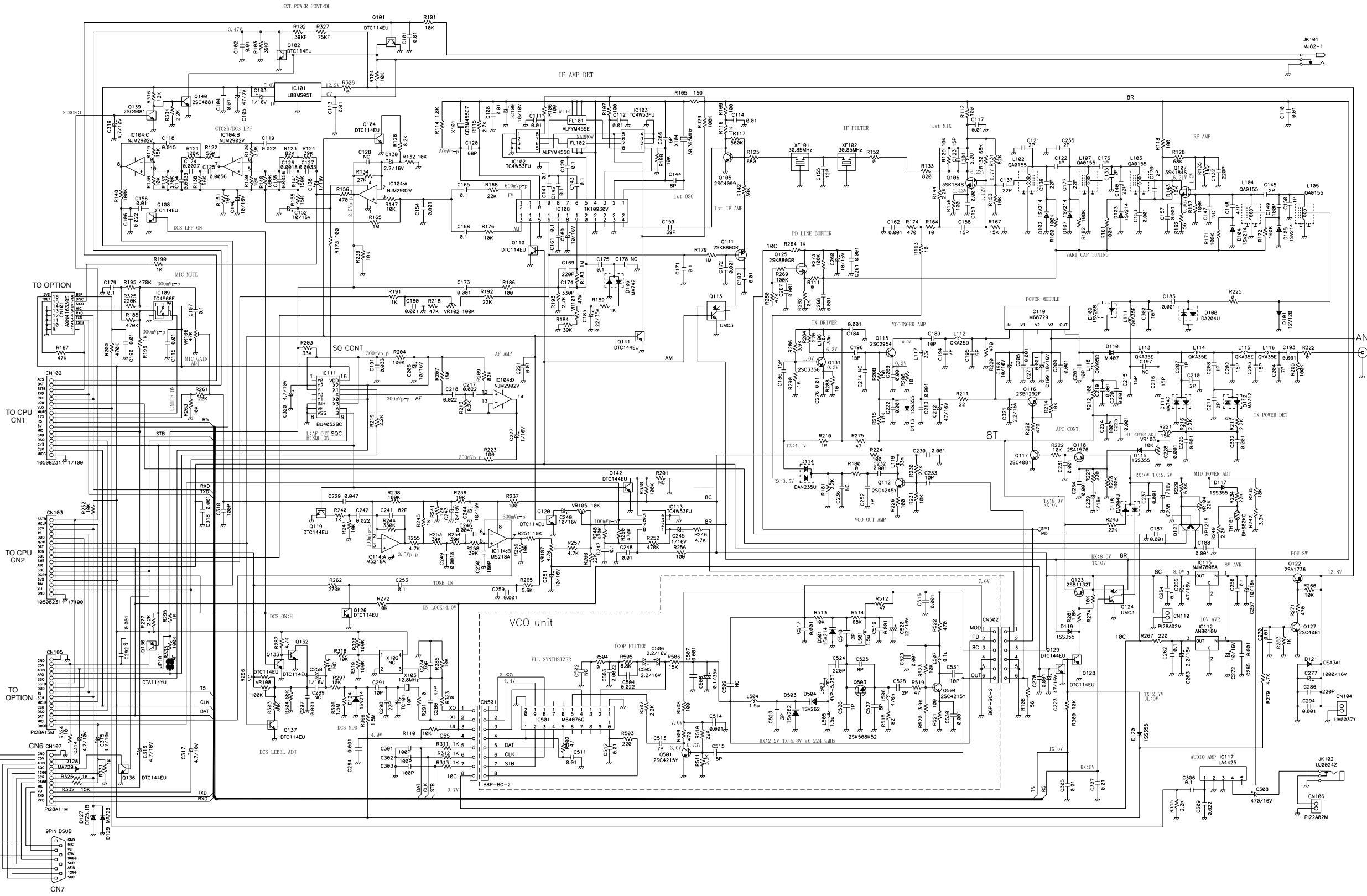


SCHMATIC DIAGRAM

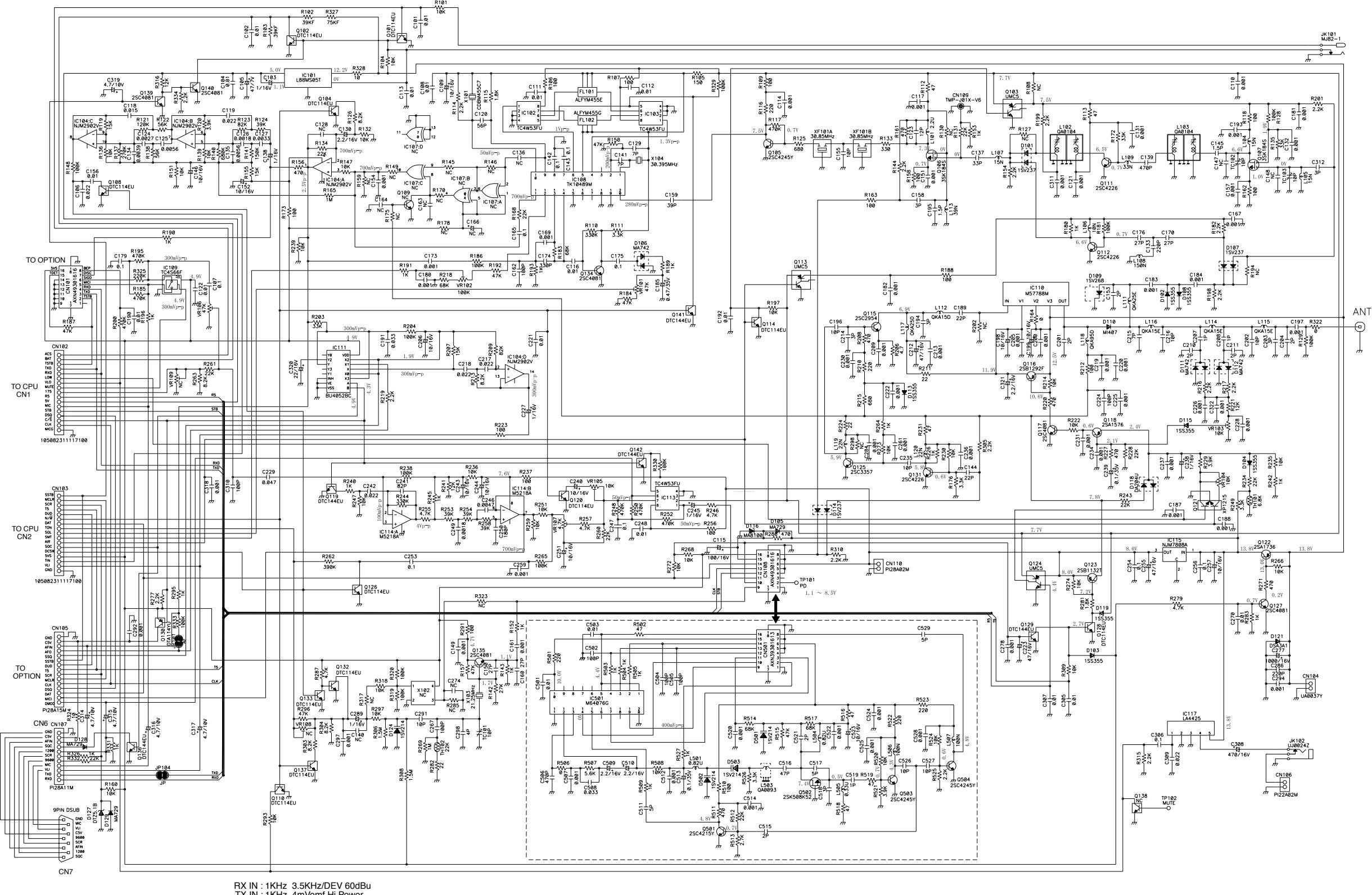
1) CPU Unit DR-135 / DR-235 / DR-435



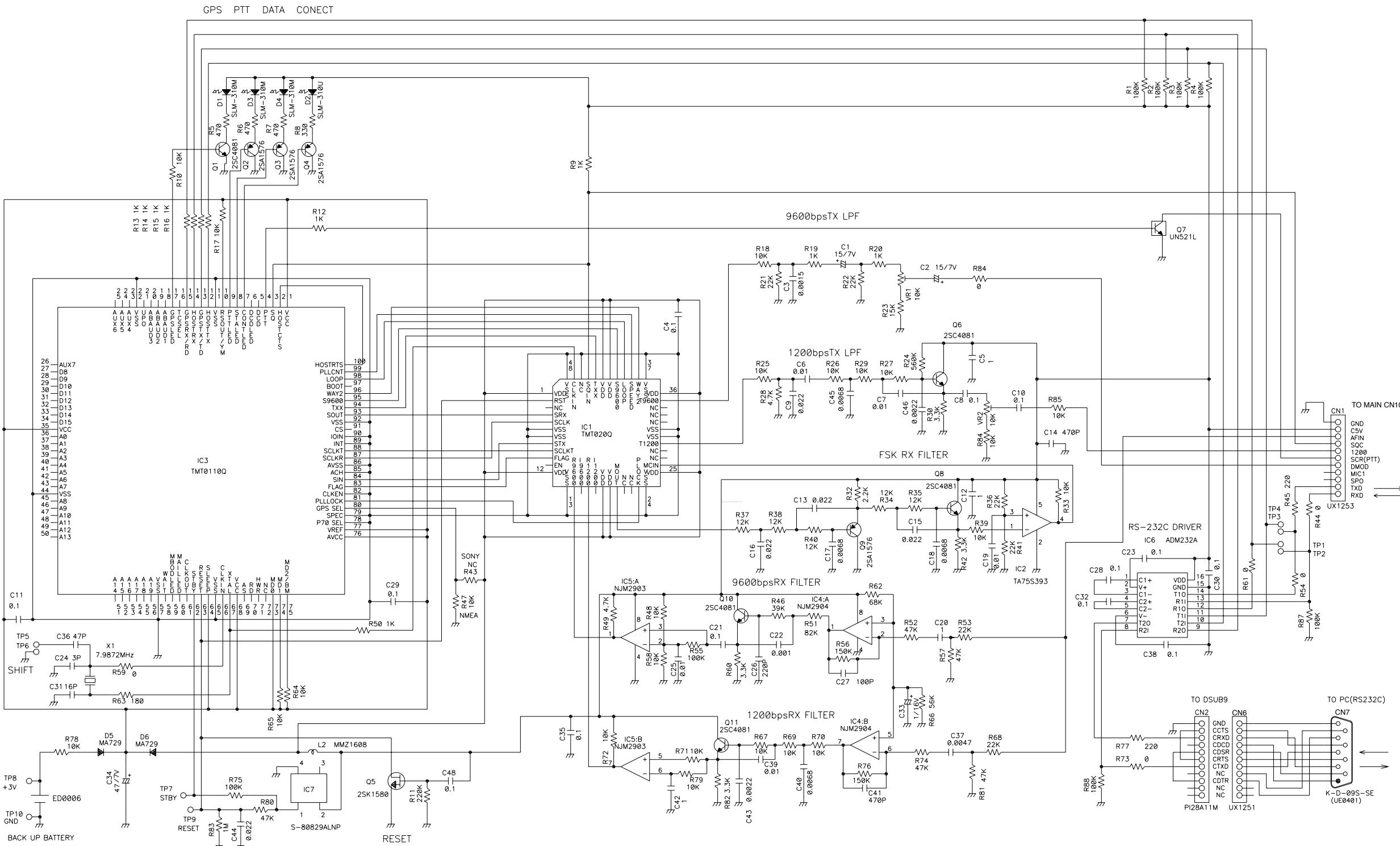
3) MAIN Unit DR-235



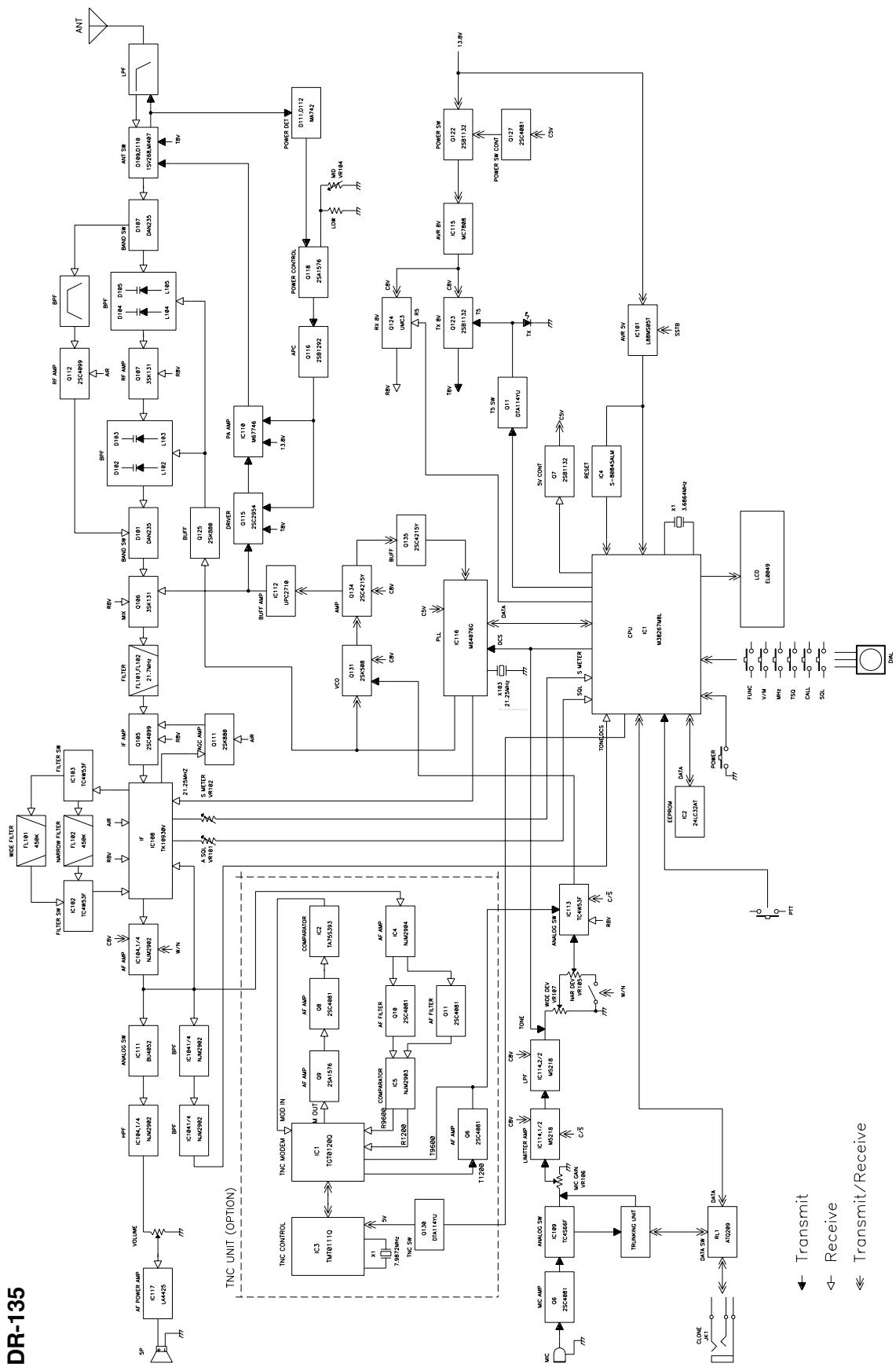
4) MAIN Unit DR-435



5) TNC Unit (DR-135TP only) or option

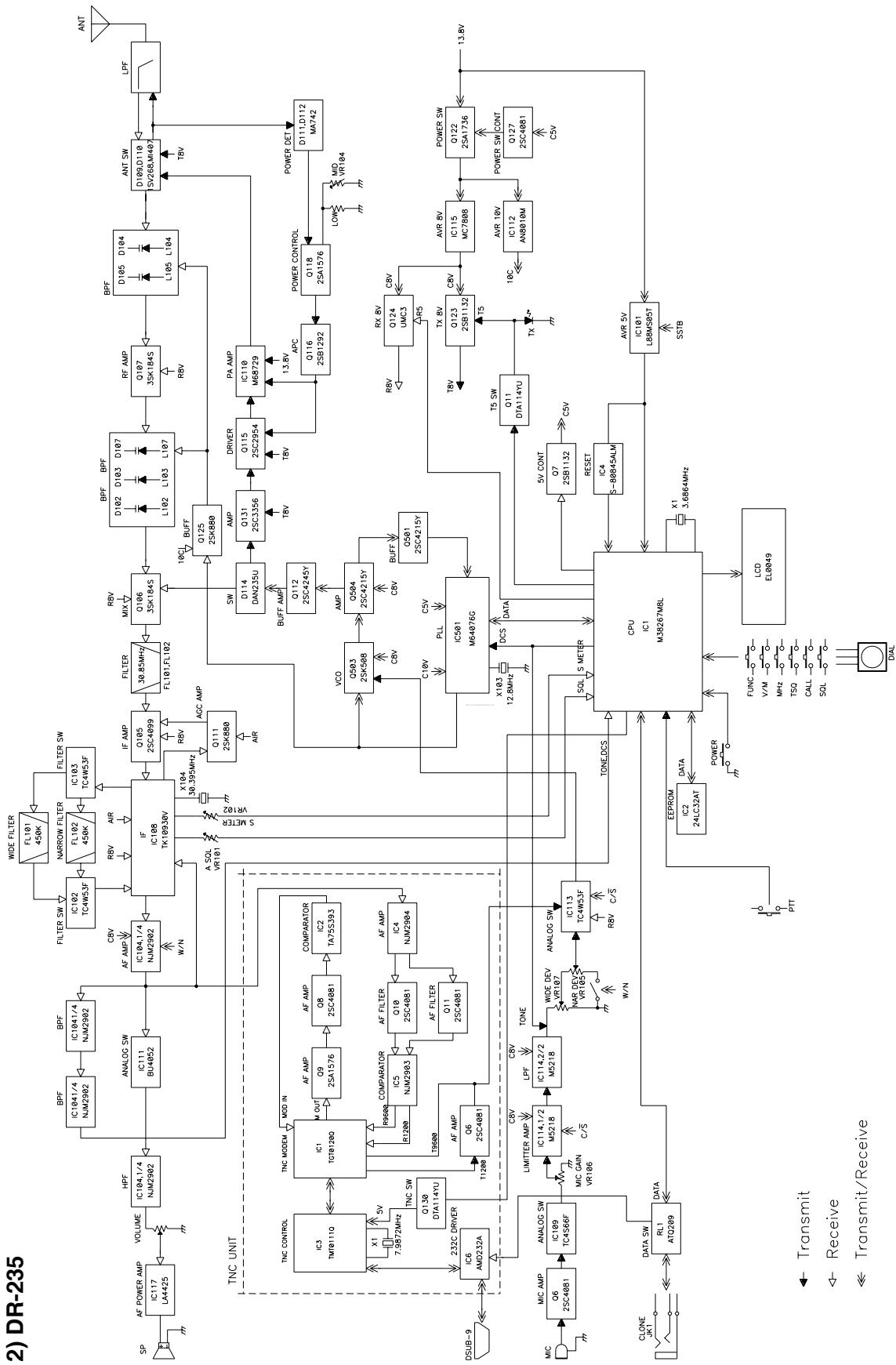


BLOCK DIAGRAM

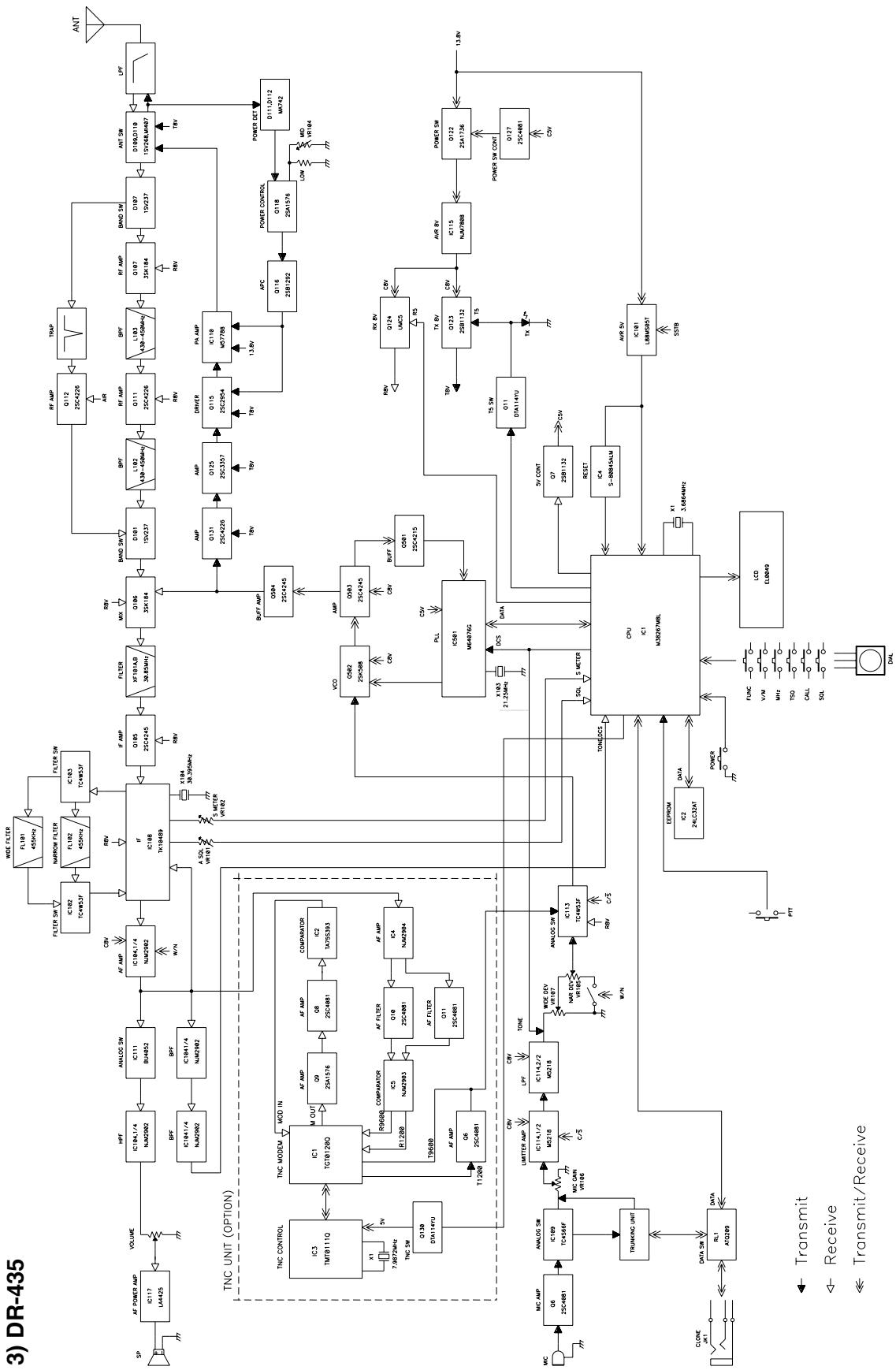


1) DR-135

2) DR-235



3) DR-435



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