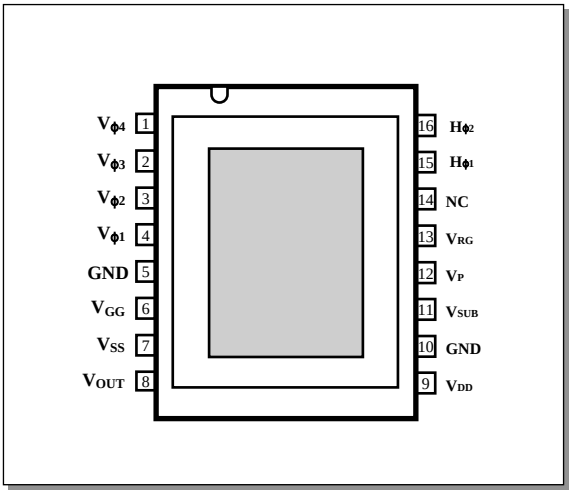
Description

The *Ai329* is a 290K pixels CCD area sensor for CCIR 1/3inch video cameras. Buried photodiode and micro lens are adopted for low noise, low smear and high sensitivity. This chip also features a strong anti-blooming and electronic shutter with variable charge-storage time.

Pin Configuration



16 Pin Plastic - DIP
(Top View)

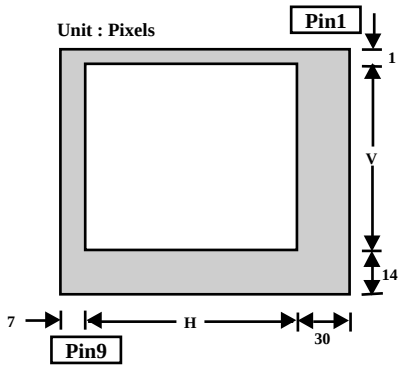
Feature

-. Micro Lens for high sensitivity
-. Image-lag is negligible and excellent blooming suppression is performed.
-. TTL level(5V) operation on HCCD & RG electrodes.
-. 16 pin plastic-DIP.
-. Variable electronic shutter of 1/50 to 1/100,000 sec.
-. High sensitivity and low smear.

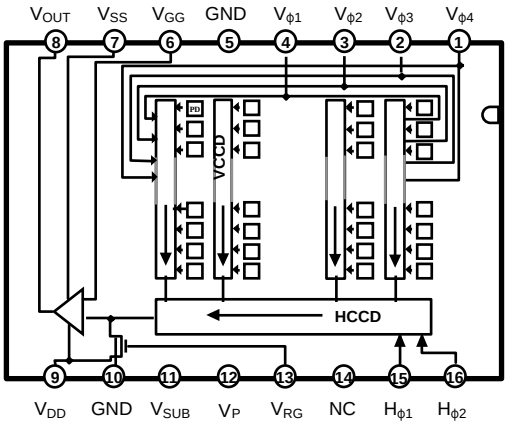
Structure

-. Architecture : IT - CCD
-. Optical size : 1/3 inch format
-. Chip size : 6.0(H) x 5.2(V) ㎟
-. Number of effective pixels :
500 (H) x 582 (V) about 290K pixels
-. Number of total pixels :
537 (H) x 597 (V) about 320K pixels
-. Pixel size : 9.8 (H) x 6.3 (V) ㎛²
-. Optical black area
Horizontal direction : Front 7 pixels Rear 30 pixels
Vertical direction : Front 14 pixels Rear 1 pixels
-. Number of dummy bits
Horizontal : 16
Vertical : 1 (Even field only)

Optical black position(Top View)



Block Diagram



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	$V_{\phi4}$	Vertical register transfer clock 4	9	V_{DD}	Output amplifier drain bias
2	$V_{\phi3}$	Vertical register transfer clock 3	10	GND	Ground
3	$V_{\phi2}$	Vertical register transfer clock 2	11	V_{SUB}	Substrate(Overflow drain)bias
4	$V_{\phi1}$	Vertical register transfer clock 1	12	V_P	Protection bias
5	GND	Ground	13	V_{RG}	Reset gate clock
6	V_{GG}	Output amplifier gate bias	14	NC	No connection
7	V_{SS}	Output amplifier source bias	15	$H_{\phi1}$	Horizontal register transfer clock 1
8	V_{OUT}	CCD Output signal	16	$H_{\phi2}$	Horizontal register transfer clock 2

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Substrate voltage	V_{SUB} - GND	-0.3 to +55	V
Supply voltage	V_{DD}, V_{OUT}, V_{SS} - GND V_{DD}, V_{OUT}, V_{SS} - V_{SUB}	-0.3 to +18 -55 to +10	V V
Vertical clock input voltage	$V_{\phi1,\ 2,\ 3,\ 4}$ - GND $V_{\phi1,\ 2,\ 3,\ 4}$ - V_P $V_{\phi1,\ 2,\ 3,\ 4}$ - V_{SUB}	-10 to +20 -0.3 to +27 -55 to +10	V V V
Horizontal clock input voltage	$H_{\phi1}$, $H_{\phi2}$ - GND	-10 to +15	V
Between vertical clock input pins	$V_{\phi x}$ - $V_{\phi y}$	-10 to +15	V
Between horizontal clock and vertical clock input pins	$H_{\phi1}$, $H_{\phi2}$ - $V_{\phi4}$	-17 to +17	V
Output pin voltage	$_{\phi}$RG, V_{GG} - GND $_{\phi}$RG, V_{GG} - V_{SUB}	-10 to +15 -55 to +10	V V
Protective circuit voltage	Vp - V_{SUB}	-65 to 0.3	V
Storage temperature	T_{STG}	-30 to 80	℃
Operation temperature	T_{OPR}	-10 to 60	℃

Bias Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Output amplifier drain voltage	V_{dd}	14.5	15.0	15.5	V	
Output amplifier gate voltage	V_{gg}	1.5	2.0	2.5	V	
Output amplifier source voltage	V_{ss}	Ground through 680Ω Resistor, ±5%				
Substrate voltage adjustment range	V_{sub}	5		15	V	
Fluctuation range after substrate voltage adjustment	$\triangle V_{sub}$	-1		1	V	
Reset gate clock voltage adjustment range	V_{rgl}	0		4	V	
Fluctuation range after reset gate voltage adjustment	$\triangle V_{rgl}$	-3		3	%	
Protection bias	V_p	Set to low level of vertical transfer clock				

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output amplifier drain current	I_{DD}	-	3	-	mA

Driving Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit
Vertical clock high voltage	$\Phi V_{H1,}\ V_{H3}$	14.5	15.0	15.5	V
Vertical clock middle voltage	$\Phi V_{M1, 2, 3, 4}$	-0.2	0.0	0.2	V
Vertical clock low voltage	$\Phi V_{L1, 2, 3, 4}$	-9.0	-8.5	-8.0	V
Horizontal clock high voltage	$\Phi H_{H1, 2}$	4.5	5.0	5.5	V
Horizontal clock low voltage	$\Phi H_{L1, 2}$	-0.5	0.0	0.5	V
RG clock voltage difference	ΦRG_{HL}	4.7	5.0	5.3	V
Substrate clock voltage	ΦV_{SUB}	23	24	25	V

Electro-optical Performance

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement Method	Remark
Sensitivity	SENS	55	70		mV/Lux	1	
Saturation signal	V_{SAT}	800			mV	2	Temp=60℃
Smear	S_{MR}			0.015	%	3	
Blooming	BL			1	%	4	
Video signal shading	OSNU			15	%	5	
Dark signal level	V_{DARK}			2	mV	6	Temp=60℃
Dark signal shading	DSNU			2	mV	7	Temp=60℃

Measurement Method

1. Sensitivity

① Set to SILC (Standard Illumination Conditions*)
② Measure the average value of signal output (Vout)
③ Calculate the efficiency of Vout to light intensity

2. Vsat

① Adjust light intensity to 200 times of SILC
② Measure the average value of signal output

3. Smear

① Adjust light intensity to 200 times of SILC & readout clock
② Measure the signal output at horizontal optical black (Vhopb)
③ Measure the signal output at vertical blanking dummy (Vvbd)
④ Smear = { (Vvbd - Vhopb) / Vsat } × 100 (%)

4. Blooming

① Adjust light intensity to 200 times of SILC & readout clock
② Measure the signal output at horizontal optical black (Vhopb)
③ Measure the signal output at blooming dummy area (Vbd)
④ Blooming = { (Vbd - Vhopb) / Vsat } × 100 (%)

5. OSNU

① Set to SILC
② Measure the average value of signal output (Vout)
③ Measure the maximum value and the minimum value of signal output
④ OSNU = (Vmax - Vmin) / Vout 100 (%)

6. Vdark

① Measure the average value of signal output at dark condition

7. DSNU

① Measure the voltage difference between minimum and maximum of dark signal

* Standard Illumination Conditions

① Measure the average value of output of linear region
② At this time, measure the light intensity of illumination at CCD face plate
③ Define SILC with above
④ Light source: Tungsten lamp(3100K)
⑤ Use a standard test lens at F8

Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensor.

e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering

a) Make sure the package temperature does not exceed 80°C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and Dirt protection

a) Perform all assembly operations in a clean room (class 1000 or less).

b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)

c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.

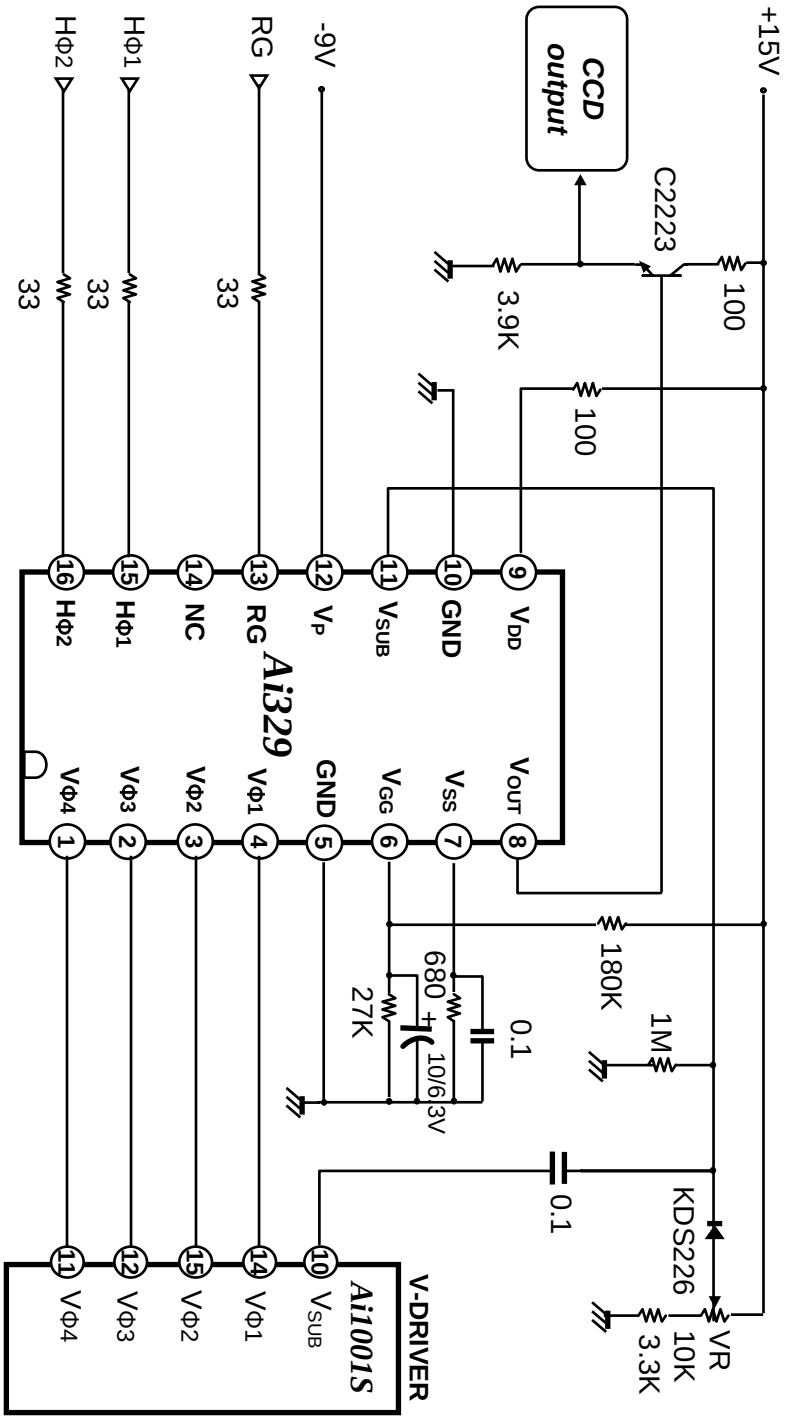
d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

4) Others

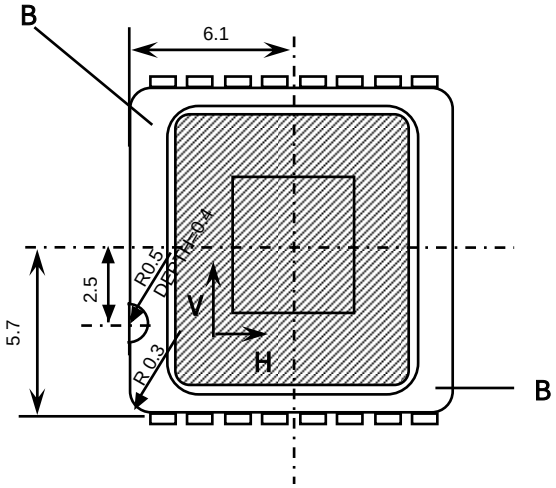
a) Do not expose to strong light (sun rays) for long periods.

b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

Application Circuit



Package Dimension (16 Pin Plastic-DIP)



UNIT = mm

1.The center of the effective image area relative to " B " and " B' "is (H, V) = (6.1, 5.7)±0.15mm.

2. The rotation angle of the effective image area relative to H and V is ±1.5°

: GLASS LID