



VNQ500PEP-E

QUAD CHANNEL HIGH SIDE DRIVER

Table 1. General Features

Type	R _{DS(on)}	I _{OUT}	V _{CC}
VNQ500PEP-E	500 mΩ	0.4 A	36V

- CMOS COMPATIBLE I/O's
- CHIP ENABLE
- JUNCTION OVERTEMPERATURE PROTECTION AND DIAGNOSTIC
- CURRENT LIMITATION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

DESCRIPTION

The VNQ500PEP-E is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground.

Active current limitation combined with latched thermal shutdown, protect the device against overload.

Figure 1. Package



In case of overtemperature of one channel the relative I/O pin is pulled down.

Device automatically turns off in case of ground pin disconnection.

Table 2. Order Codes

Package	Tube	Tape and Reel
PowerSSO-12	VNQ500PEP-E	VNQ500PEPTR-E

Figure 2. Block Diagram

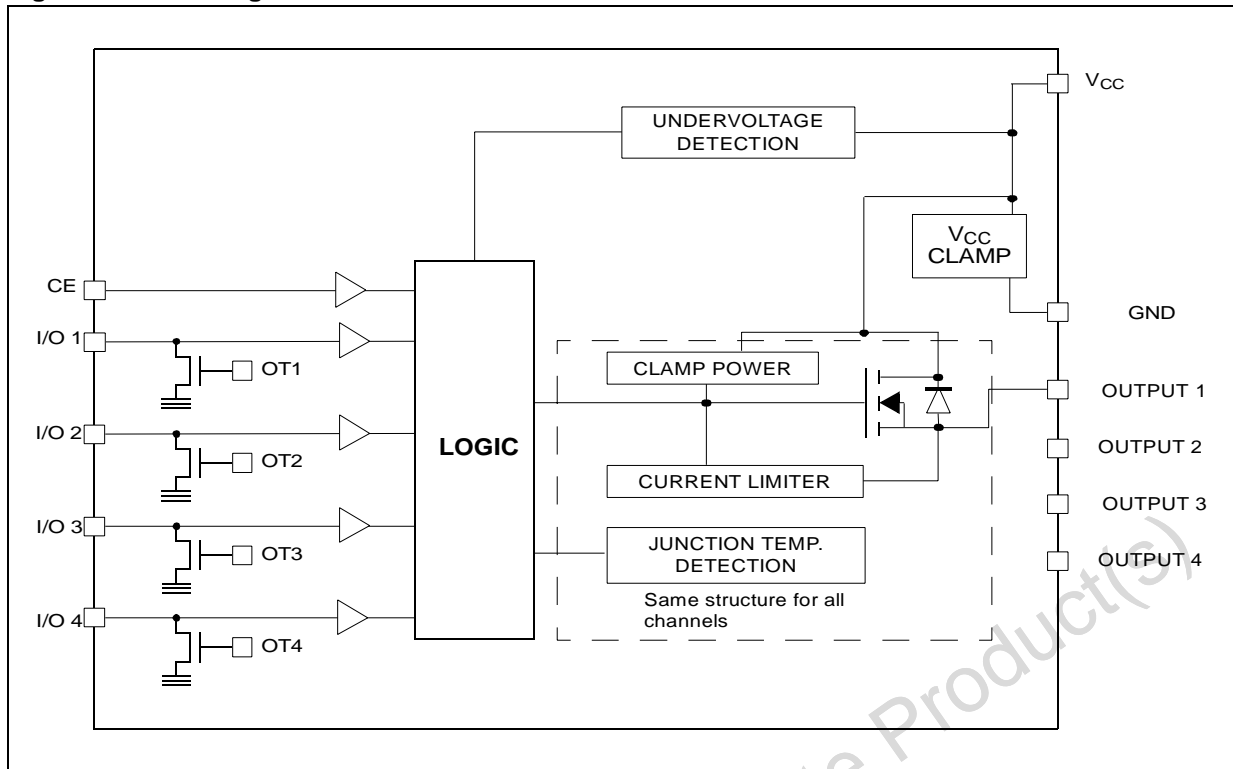


Table 3. Pin Definitions And Functions

Pin No	Symbol	Function
TAB	V _{CC}	Positive power supply voltage
7,12	V _{CC}	Positive power supply voltage
1	GND	Logic ground
2	CE	Chip Enable
3	I/O 1	Input/Output of channel 1
4	I/O 2	Input/Output of channel 2
5	I/O 3	Input/Output of channel 3
6	I/O 4	Input/Output of channel 4
8	OUTPUT 4	High-Side output of channel 4
9	OUTPUT 3	High-Side output of channel 3
10	OUTPUT 2	High-Side output of channel 2
11	OUTPUT 1	High-Side output of channel 1

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply voltage	41	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
$-I_{GND}$	DC Ground pin reverse current	- 250	mA
I_{OUT}	DC Output current	Internally Limited	A
$-I_{OUT}$	Reverse DC output current	-1	A
I_{IN}	DC Input current	+/- 10	mA
V_{ESD}	Electrostatic discharge (R=1.5K Ω ; C=100pF)	4000	V
	- I/On - OUTn & Vcc	5000	V
P_{tot}	Power dissipation at $T_c=25^\circ\text{C}$	73	W
T_j	Junction operating temperature	Internally Limited	$^\circ\text{C}$
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$

Figure 3. Configuration Diagram (Top View)

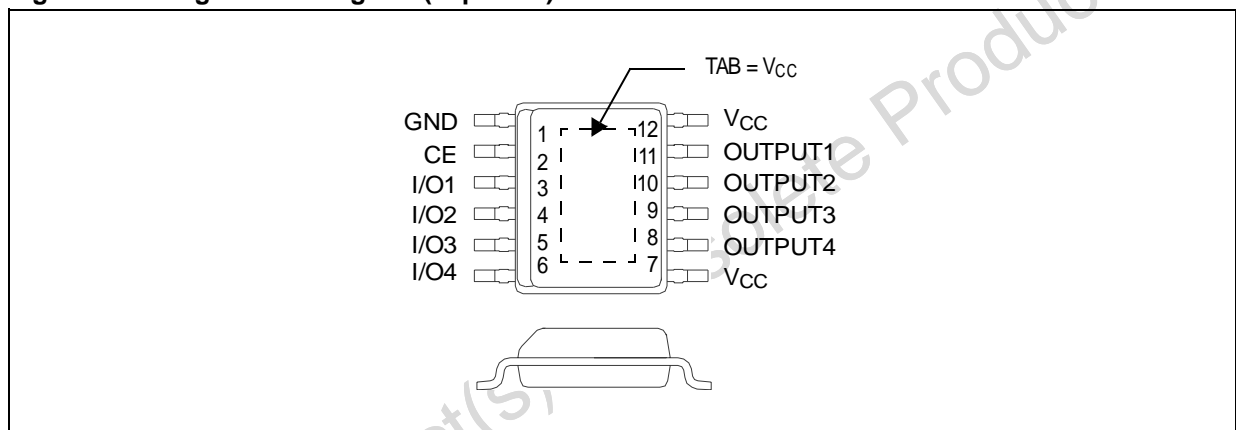


Figure 4. Current and Voltage Conventions

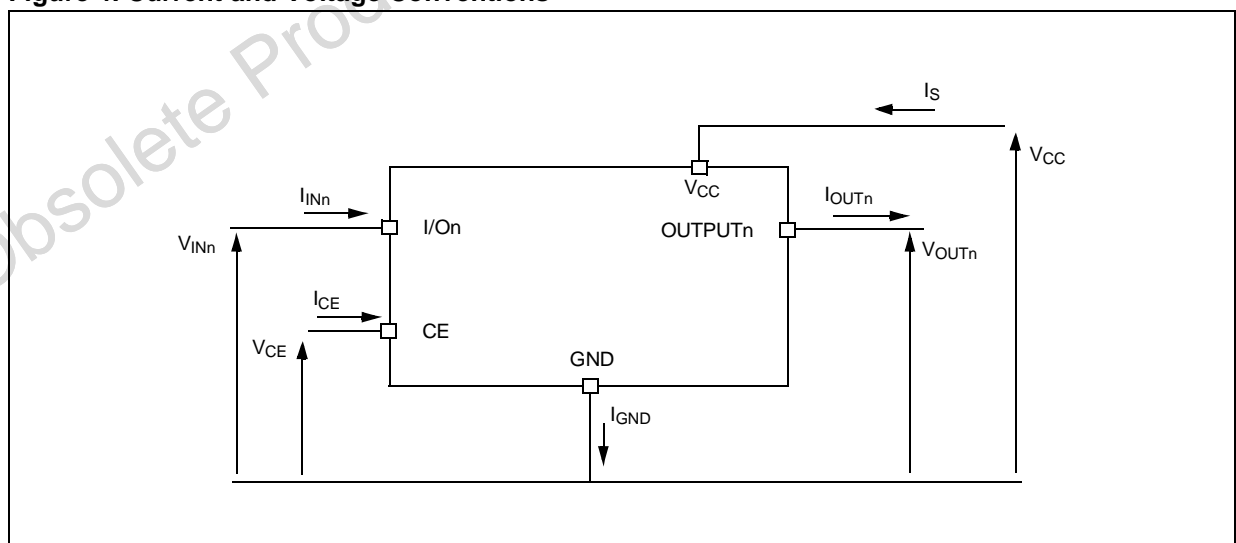


Table 5. Thermal Data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal Resistance Junction-case	Max 1.7	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max 61 ⁽¹⁾ 50 ⁽²⁾	°C/W

Note: 1. When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35µm thick) connected to all V_{CC} pins.
 Note: 2. When mounted on a standard single-sided FR-4 board with 8cm² of Cu (at least 35µm thick) connected to all V_{CC} pins.

ELECTRICAL CHARACTERISTICS (8V < V_{CC} < 36V; -40°C < T_j < 150°C unless otherwise specified)

Table 6. Power

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{CC} (**)	Operating supply voltage		5.5	13	36	V
V _{USD} (**)	Undervoltage shut-down		3	4	5.5	V
V _{OV} (**)	Overvoltage shutdown		36			V
R _{ON}	On state resistance	I _{OUTn} =0.25A; T _j =25°C I _{OUTn} =0.25A			500 1000	mΩ mΩ
I _S	Supply current	V _{CE} =V _{I/On} =0V; V _{CC} =13V; T _{case} =25°C On state (all channels ON); V _{CC} =13V			20 8	µA mA
I _{LGND} (**)	Output current at turn-off	V _{CC} =V _{CE} =V _{I/On} =V _{GND} =13V V _{OUTn} =0V			1	mA
I _{L(off)} (**)	Off state output current	V _{I/On} =V _{OUTn} =0V	0		5	µA
I _{Loff2} (**)	Off state output current	V _{I/On} =0V, V _{OUTn} =0V, V _{CC} =13V; T _{case} =25°C			1	µA

Note: (**) Per channel

Table 7. Switching (V_{CC} =13V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{on}	Turn-on time	R _L =52Ω from 80% V _{OUT} ⁽¹⁾		50		µs
t _{off}	Turn-off time	R _L =52Ω to 10% V _{OUT} ⁽¹⁾		75		µs
dV _{OUT} /dt _(on)	Turn-on voltage slope	R _L =52Ω from V _{OUT} =1.3V to V _{OUT} =10.4V ⁽¹⁾		0.3		V/µs
dV _{OUT} /dt _(off)	Turn-off voltage slope	R _L =52Ω from V _{OUT} =11.7V to V _{OUT} =1.3V ⁽¹⁾		0.3		V/µs

Note: (1) see figure 5 :switching time waveforms

Table 8. Input & CE Pin

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{INL}	I/O low level				1.25	V
I _{INL}	Low level I/O current	V _{IN} =1.25V	1			µA
V _{INH}	I/O high level		3.25			V
I _{INH}	High level I/O current	V _{IN} =3.25V			10	µA
V _{I(hyst)}	I/O hysteresis voltage		0.5			V
V _{ICL}	Input Clamp Voltage	I _{IN} =1mA I _{IN} =-1mA	6	6.8 -0.7	8	V V



ELECTRICAL CHARACTERISTICS (continued)

Table 9. Protections (see note 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OL}	I/O low level default detection	$I_{IN}=1mA$, latched thermal shutdown			0.5	V
T_{TSD}	Junction shut-down temperature		150	175	200	°C
I_{lim}	DC Short circuit current	$V_{CC}=13V$; $R_{LOAD}=10m\Omega$	0.4		0.9	A
V_{demag}	Turn-off output clamp voltage	$I_{OUT}=0.25 A$; $L=50mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V
t_{reset}	Thermal latch reset time	$T_J < T_{TSD}$ (see figure 3 in waveforms)			10	μs

Note: 1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

Figure 5. Switching Time Waveforms: Turn-on & Turn-off

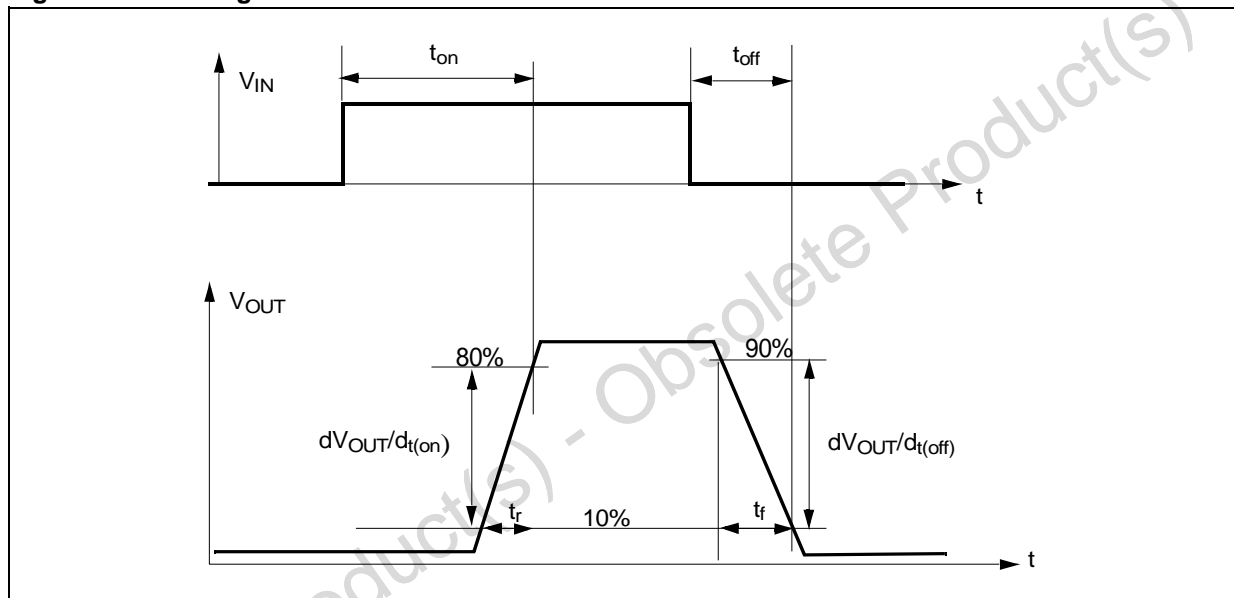


Figure 6. Driving Circuit

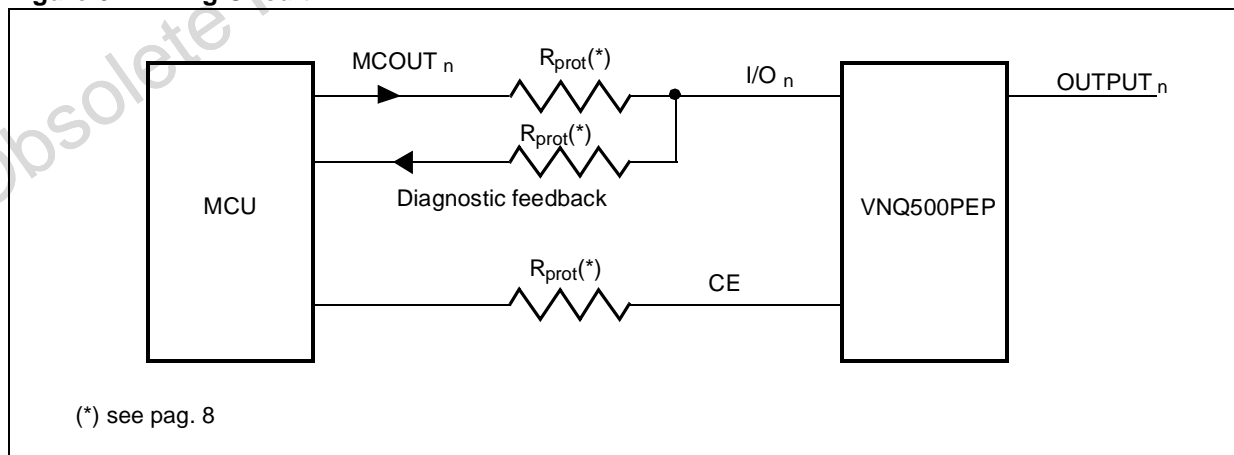


Table 10. Truth Table

CONDITIONS	MCOUTn	CE	I/On	OUTPUTn
Normal operation	L	H	L	L
	H	H	H	H
Current limitation	L	H	L	L
	H	H	H	H
Overtemperature	L	H	L	L
	H	H	L (latched)	L
Undervoltage	L	H	L	L
	H	H	H	L
Stand-by	X	L	X	L

Table 11. Electrical Transient Requirements On V_{CC} Pin

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Waveforms

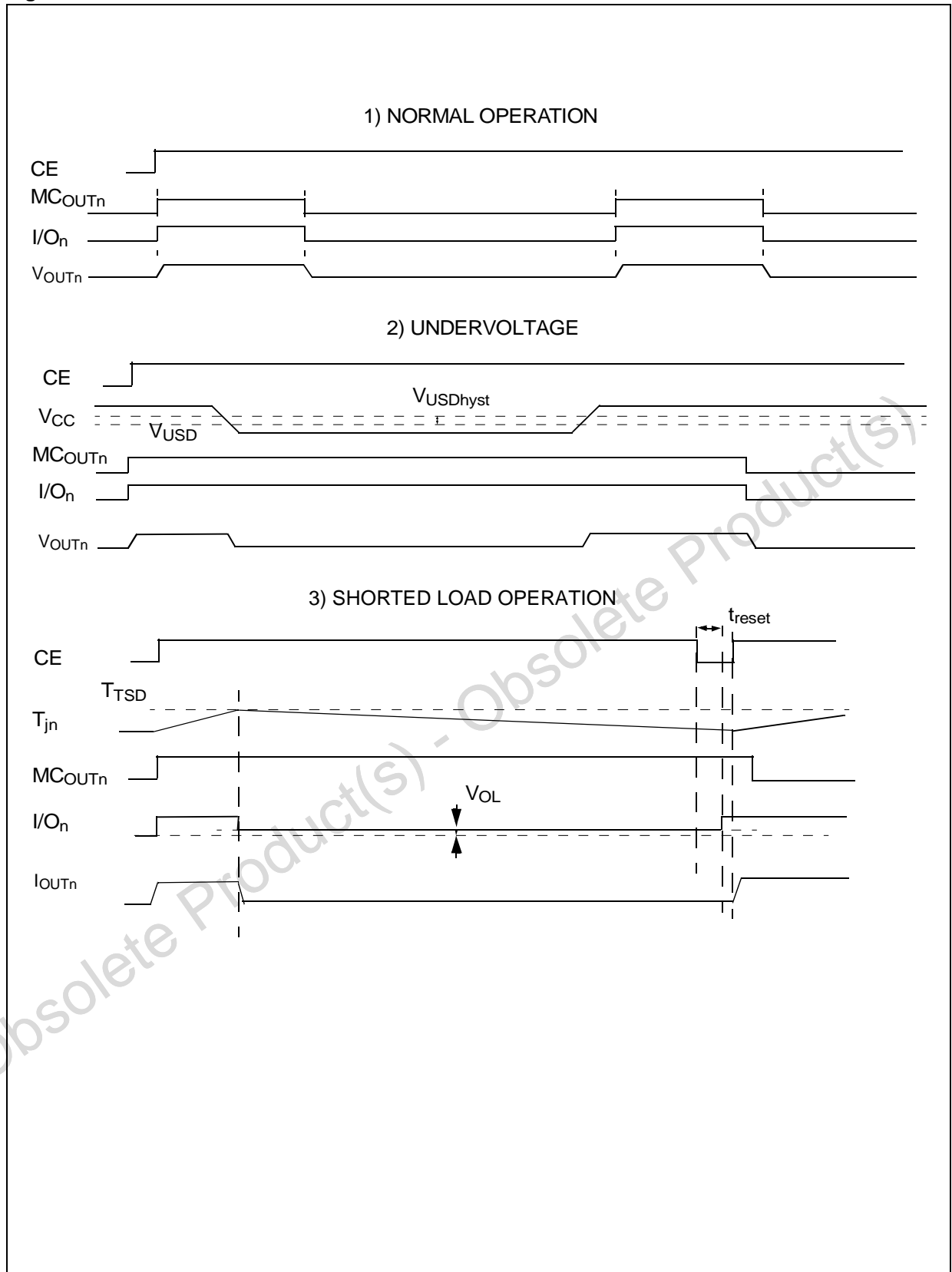
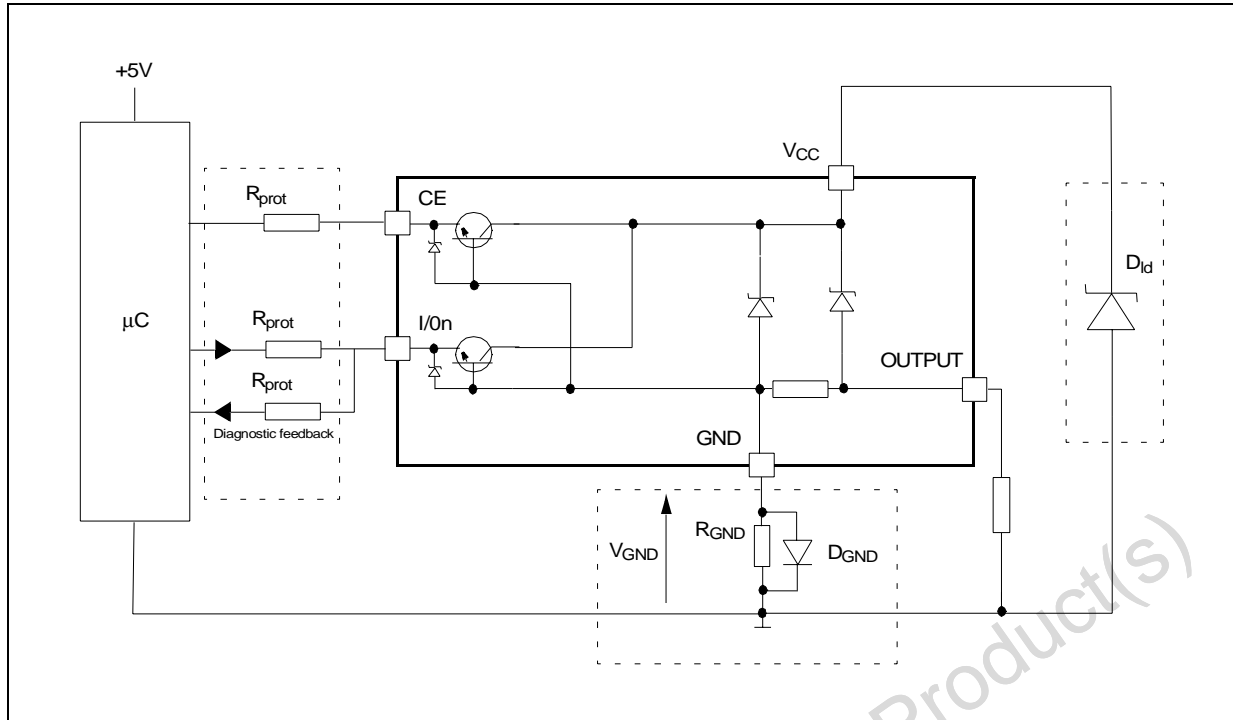


Figure 8. Application Schematic



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600mV / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where -I_{GND} is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where I_{S(on)max} becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift (I_{S(on)max} * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of

the ground network will produce a shift (≈600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OHµC} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = -100V and I_{latchup} ≥ 20mA; V_{OHµC} ≥ 4.5V

$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended R_{prot} value is 10kΩ.

Figure 9. Off State Output Current

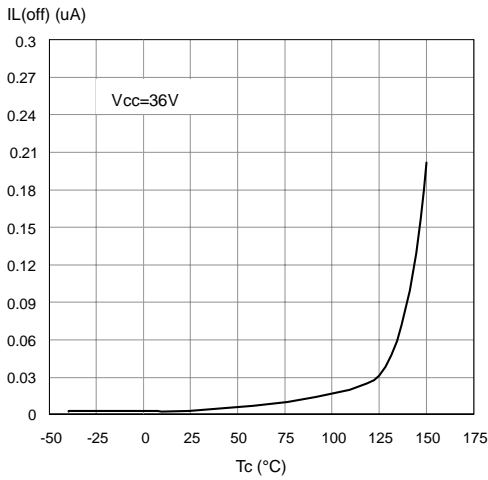


Figure 10. High Level Input Current

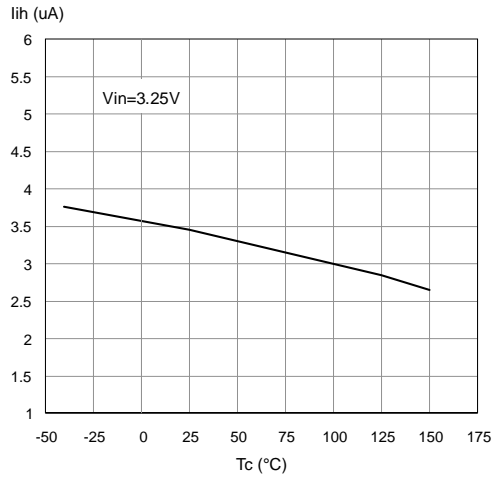


Figure 11. Input Clamp Voltage

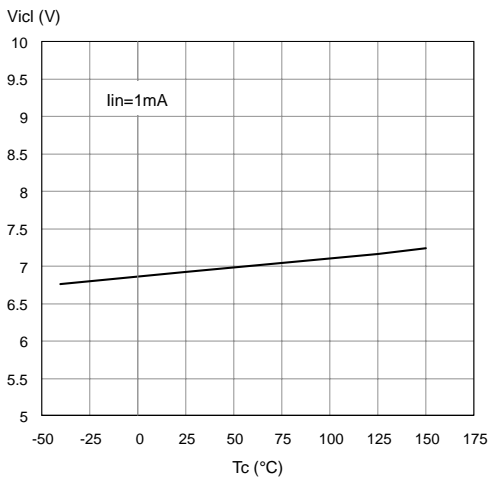


Figure 13. Overvoltage Shutdown

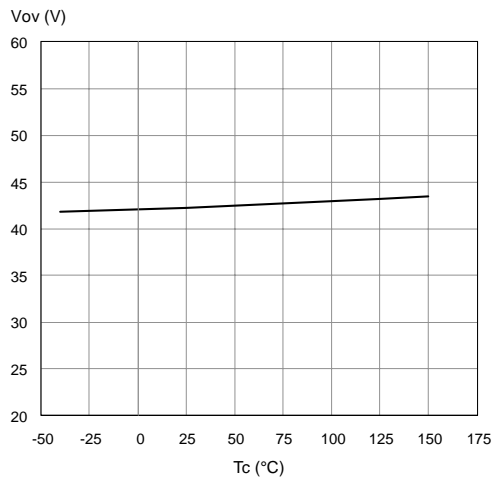


Figure 12. Turn-on Voltage Slope

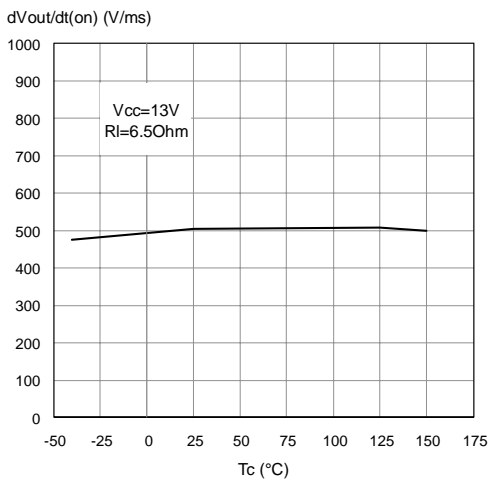


Figure 14. Turn-off Voltage Slope

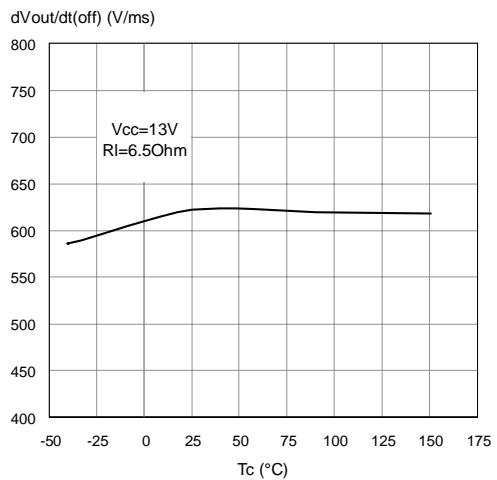


Figure 15. I_{LIM} Vs T_{case}

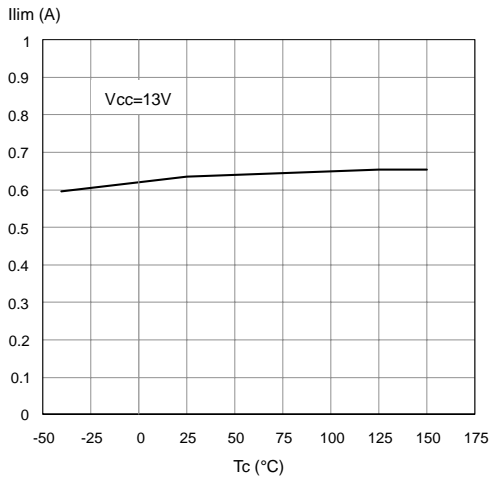


Figure 18. Input Hysteresis Voltage

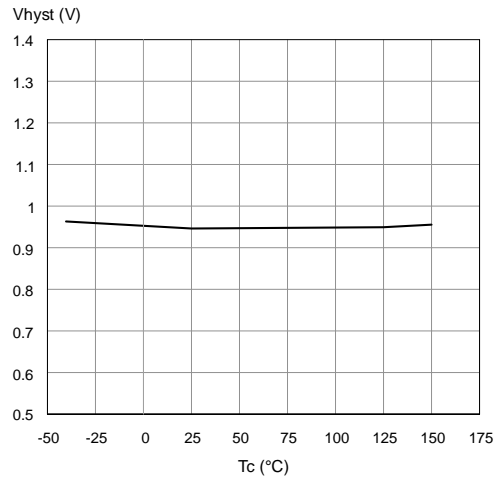


Figure 16. On State Resistance Vs V_{CC}

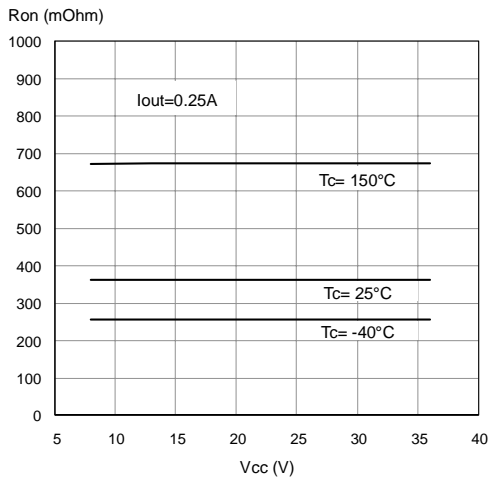


Figure 19. On State Resistance Vs T_{case}

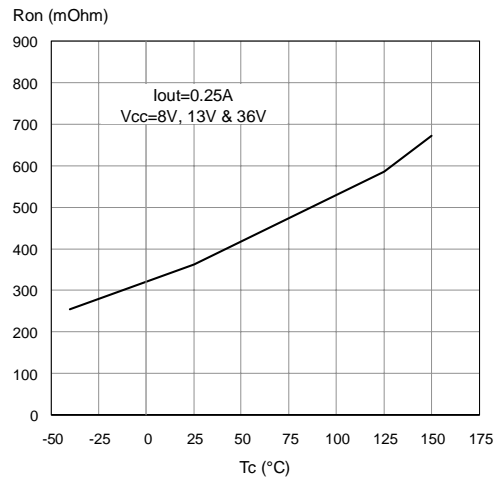


Figure 17. Input High Level

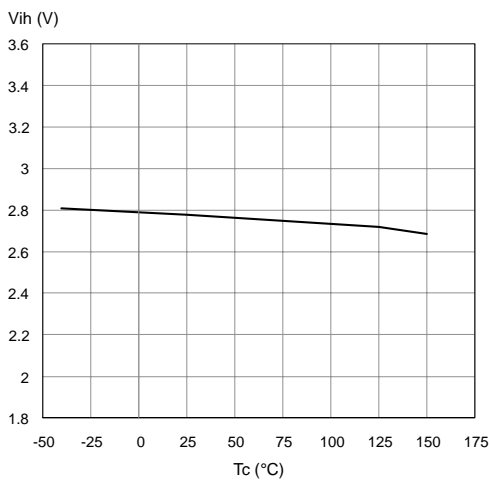


Figure 20. Input Low Level

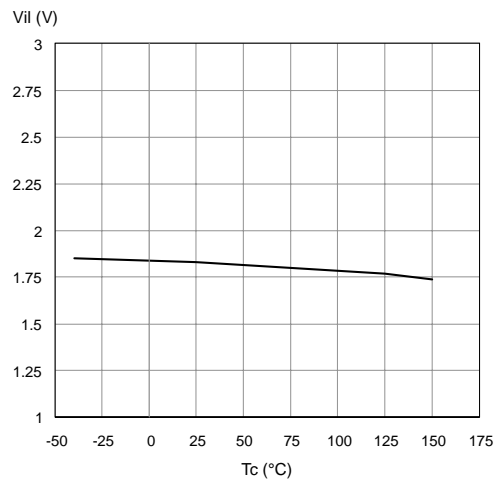
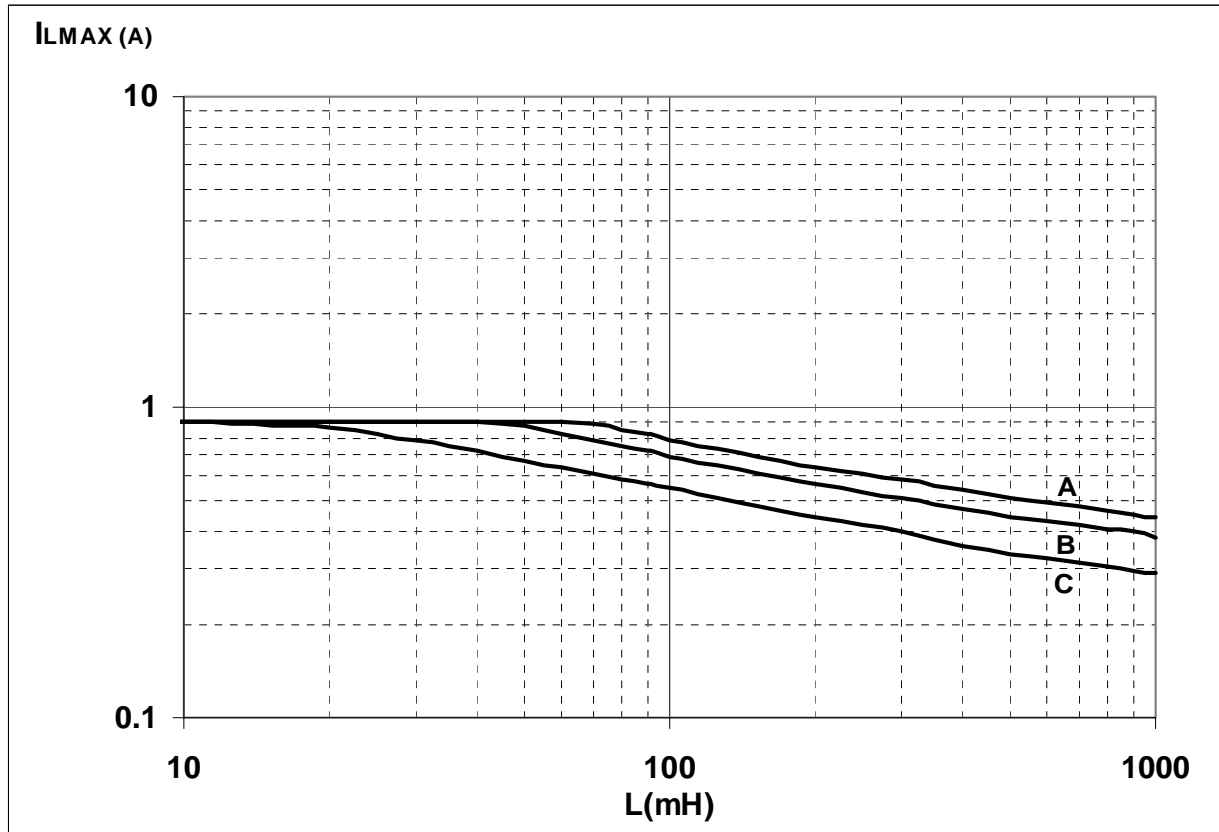


Figure 21. Maximum Turn Off Current Versus Load Inductance



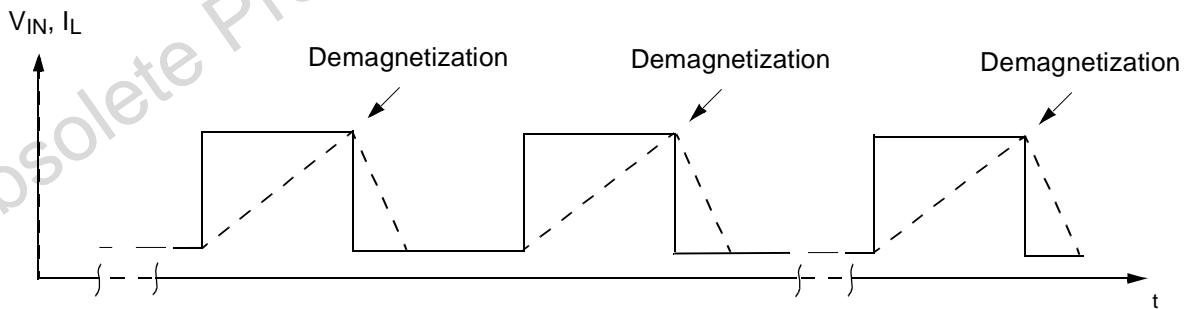
- A = Single Pulse at $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at $T_{Jstart}=100^{\circ}C$
- C= Repetitive Pulse at $T_{Jstart}=125^{\circ}C$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Conditions:

$V_{CC}=13.5V$



PowerSSO-12 Thermal Data

Figure 22. PowerSSO-12 PC Board

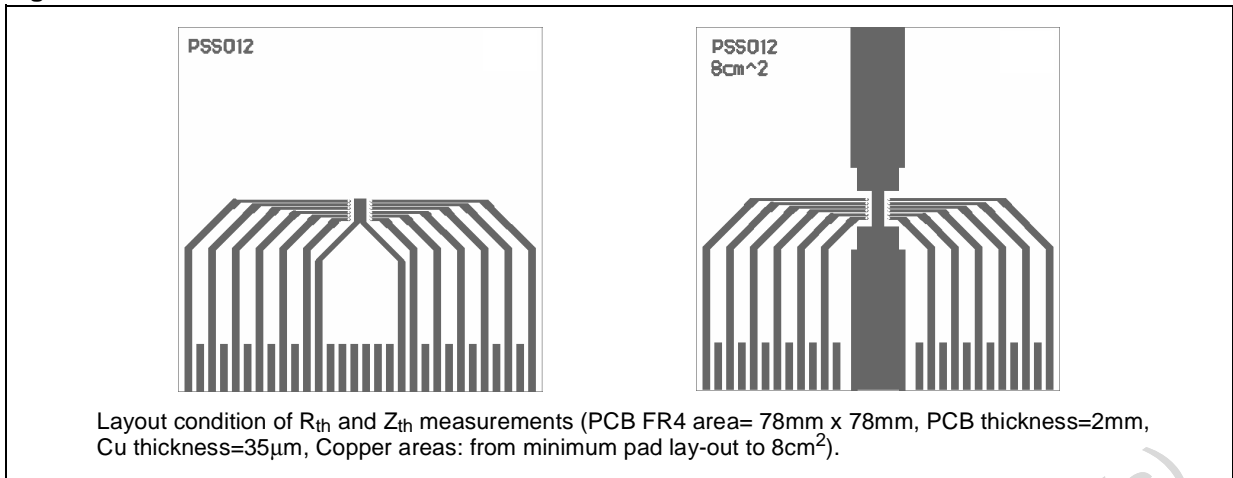


Figure 23. $R_{thj-amb}$ Vs PCB copper area in open box free air condition

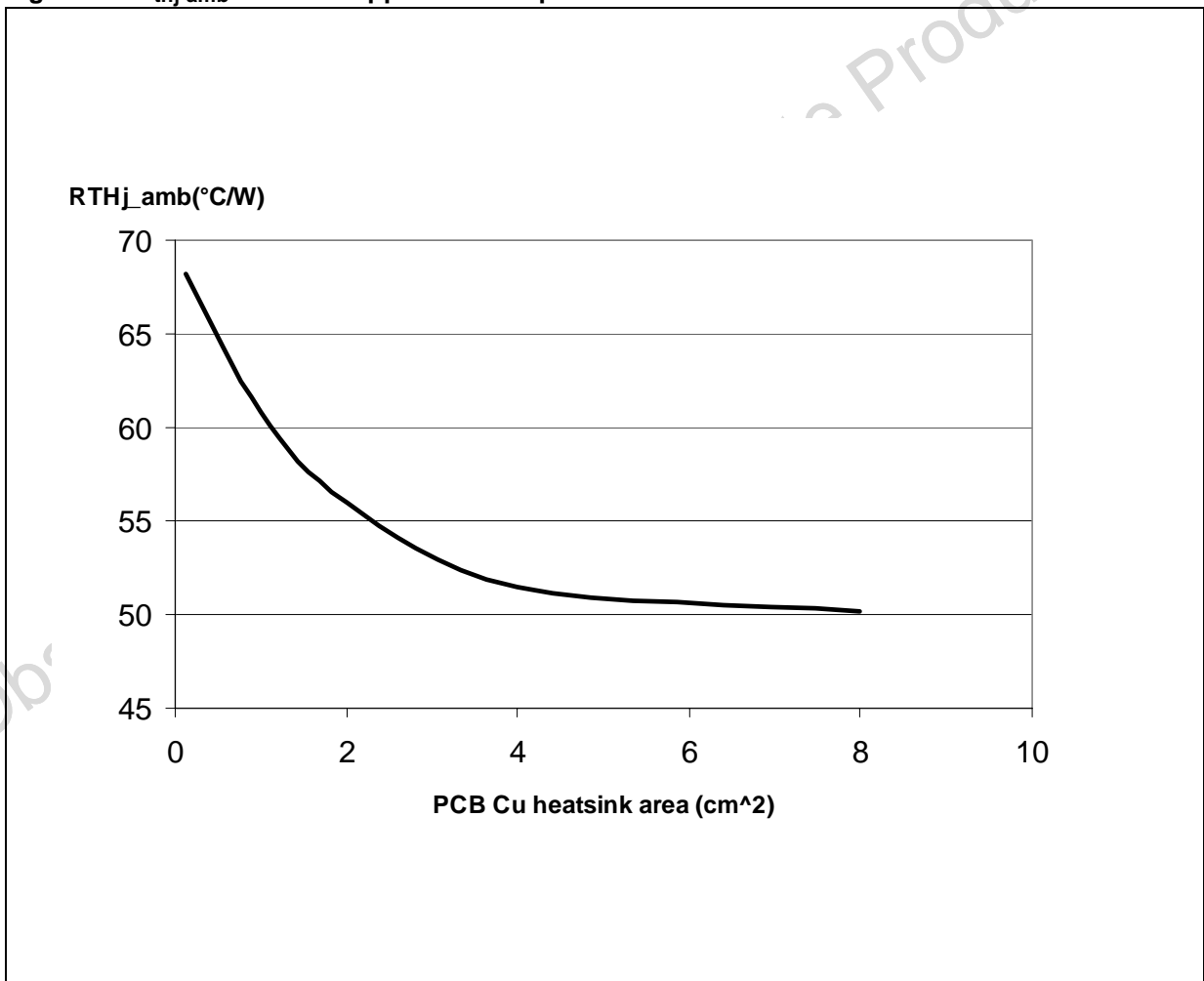


Figure 24. Thermal Impedance Junction Ambient Single Pulse

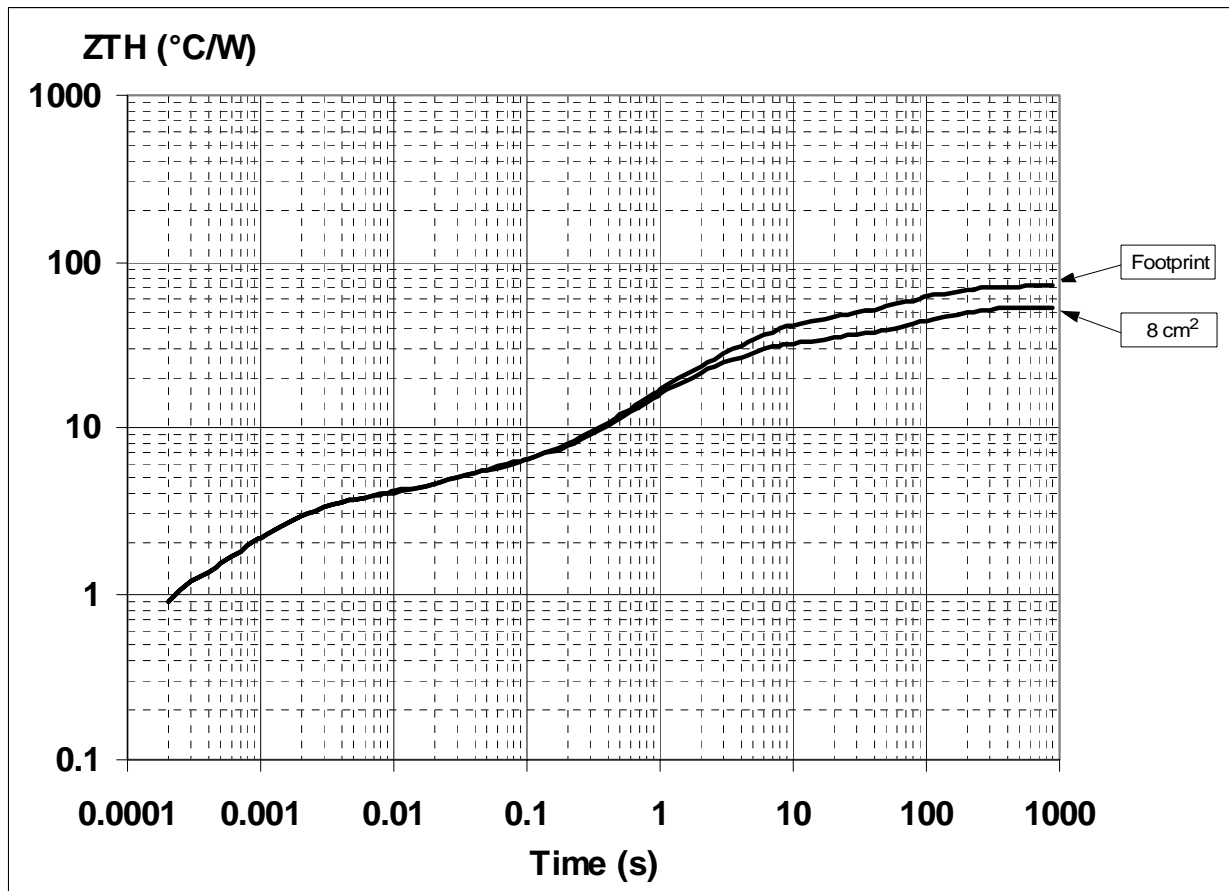
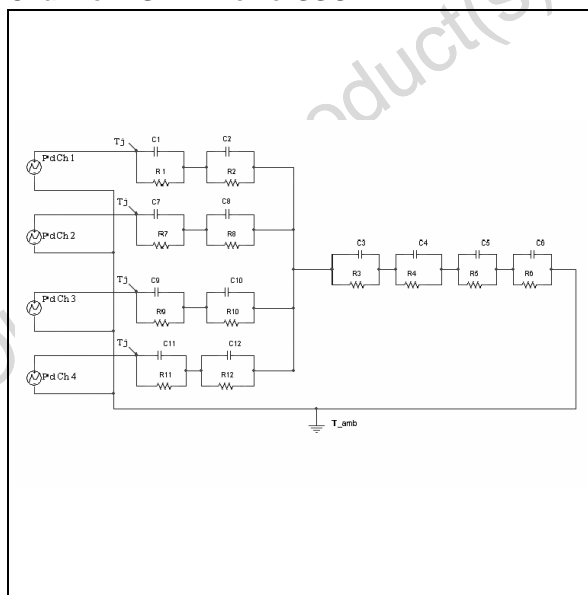


Figure 25. Thermal Fitting Model of a Quad Channel HSD in PowerSSO-12



Pulse Calculation Formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 12. Thermal Parameter

Area/island (cm ²)	Footprint	8
R1=R7=R9=R11 (°C/W)	0.8	
R2=R8=R10=R12 (°C/W)	2.6	
R3 (°C/W)	1.5	
R4 (°C/W)	8	
R5 (°C/W)	28	18
R6 (°C/W)	30	22
C1=C7=C9=C11 (W.s/°C)	0.00006	
C2=C8=C10=C12 (W.s/°C)	0.0005	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.1	
C5 (W.s/°C)	0.15	0.17
C6 (W.s/°C)	3	5

PACKAGE MECHANICAL

Table 13. PowerSSO-12™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
DIM.	mm.		
	MIN.	TYP	MAX.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

Figure 26. PowerSSO-12™ Package Dimensions

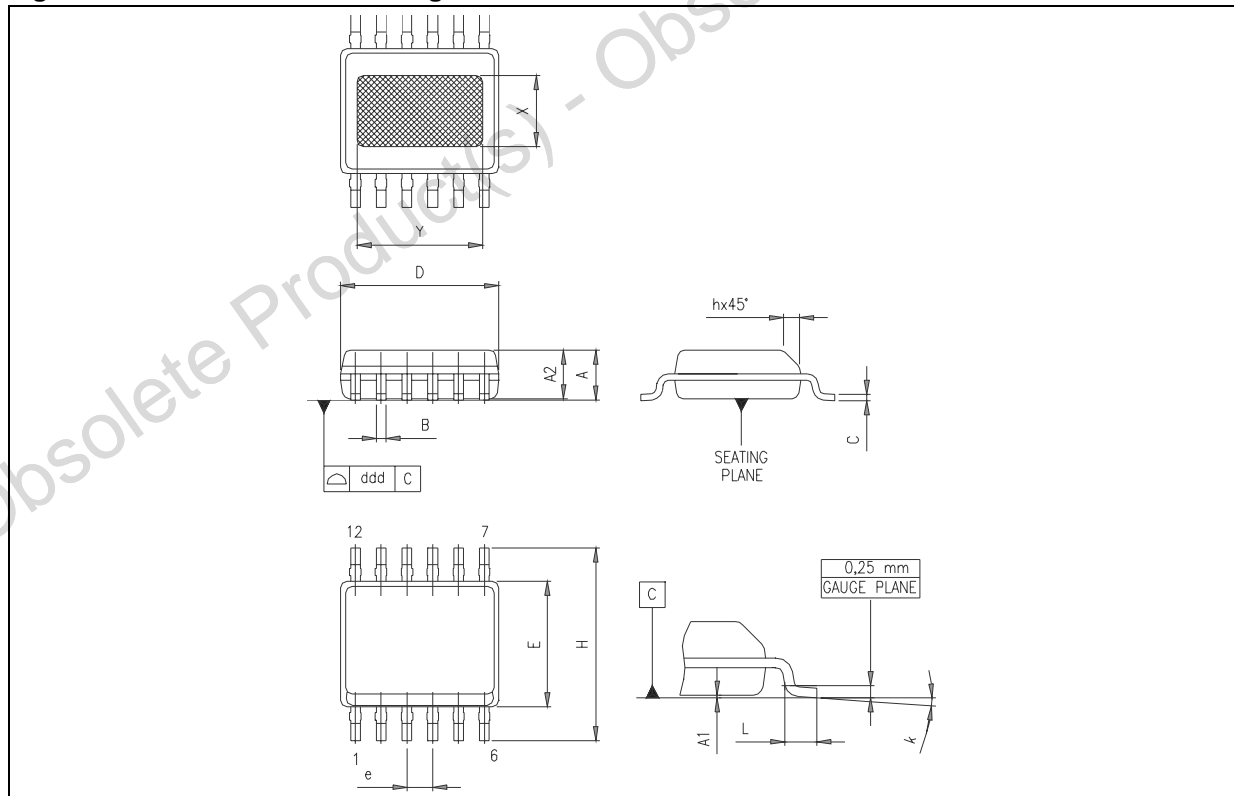


Figure 27. PowerSSO-12 Tube Shipment (No Suffix)

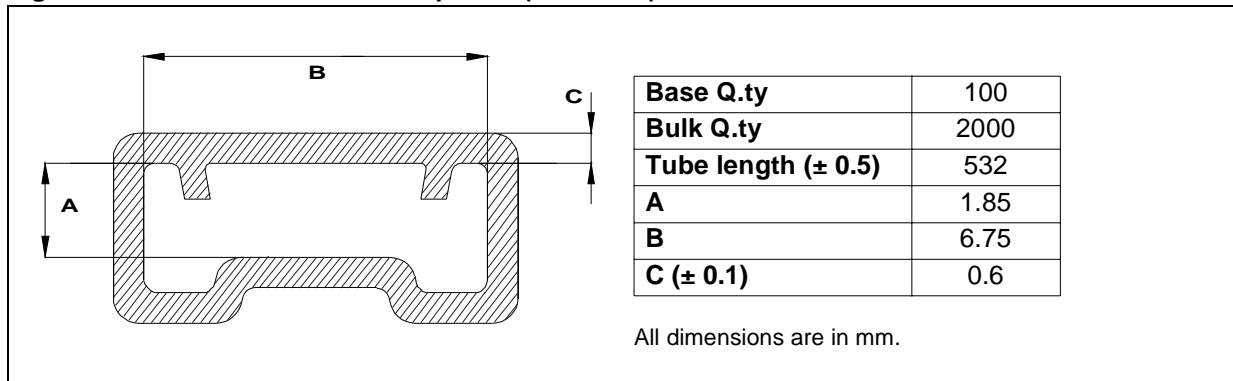
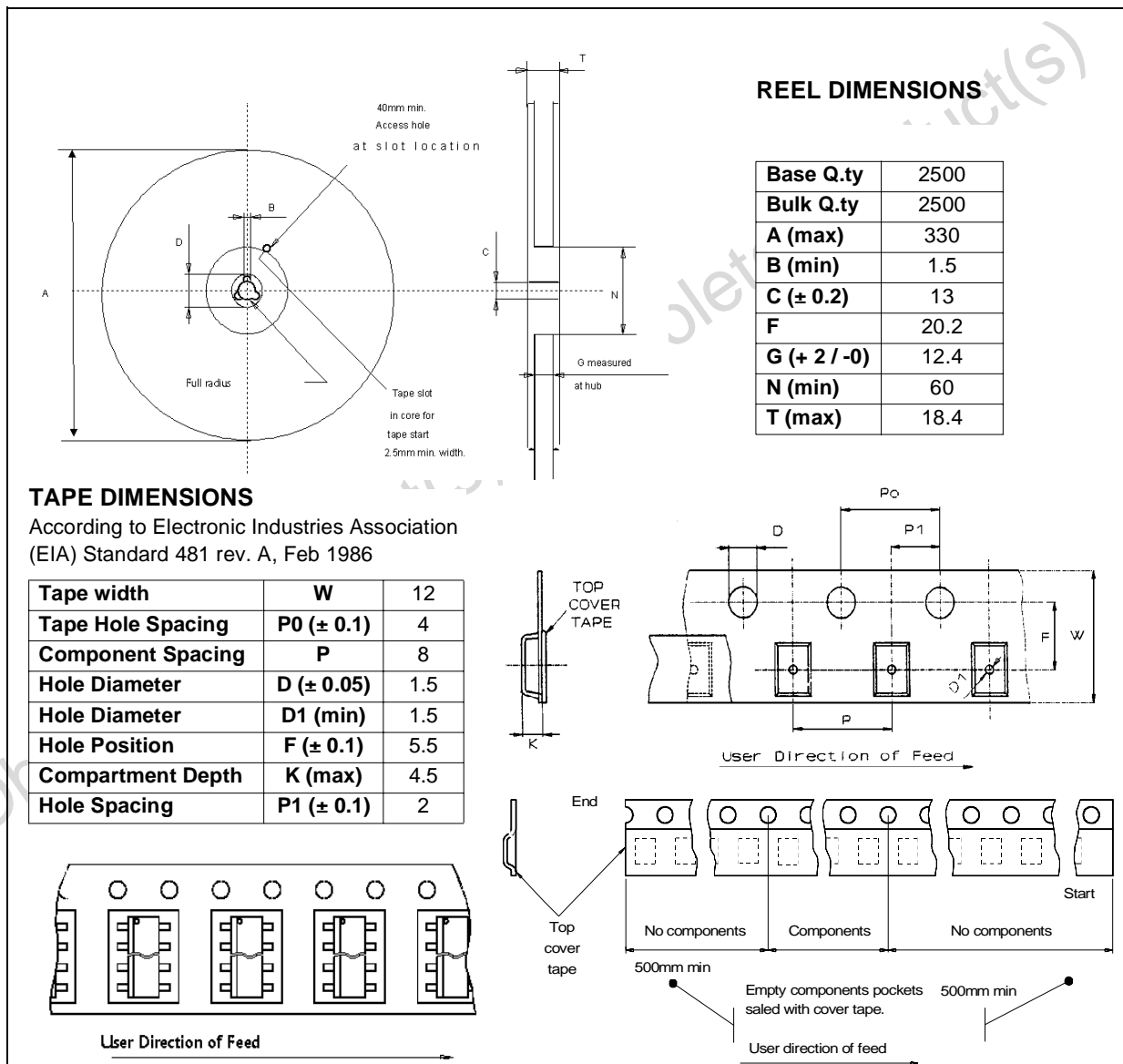


Figure 28. Tape And Reel Shipment (Suffix "TR")



REVISION HISTORY**Table 14. Revision History**

Date	Revision	Description of Changes
Dec. 2004	1	- First Issue.
Jun. 2005	2	- Electrical characterization insertion; - Configuration diagram drawing change; - Thermal data insertion; - Shipment data insertion; - Minor changes.
Jun. 2005	3	- Maximum Turn Off Current Versus Load Inductance curve insertion; - Thermal Impedance Junction Ambient Single Pulse curve insertion.
Jun. 2005	4	- Maximum Turn Off Current Versus Load Inductance curve review.

Obsolete Product(s) - Obsolete Product(s)

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